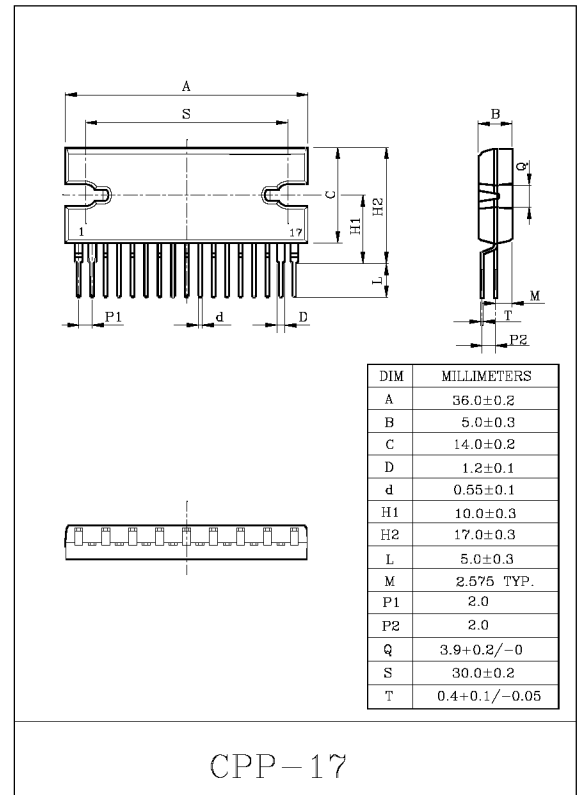


22W BTL DUAL AUDIO POWER AMPLIFIER

The thermal resistance θ_{j-T} KIA6210AH package CPP-17(Compact Power Package 17pin), designed for low thermal resistance, has high efficiency of heat radiation. The temperature rise of chip can be reduced, and the influence from the degradation of the features due to the temperature rise at the high output can also be reduced. This stereo audio power IC, designed for car audio use, has two built-in channels to reduce the characteristic difference between L and R channels. In addition, the functions of stand-by and muting, and a variety of protection circuits are involved.

FEATURES:

- Low Thermal Resistance.
 - : $\theta_{j-T}=1.5^{\circ}\text{C}/\text{W}$ (Infinite heat sink)
- High Power.
 - : $P_{OUT(1)}=22\text{W(Typ.)}/\text{channel}$
($V_{CC}=14.4\text{V}$, $f=1\text{kHz}$, $\text{THD}=10\%$, $R_L=4\Omega$)
 - : $P_{OUT(2)}=19\text{W(Typ.)}/\text{channel}$
($V_{CC}=13.2\text{V}$, $f=1\text{kHz}$, $\text{THD}=10\%$, $R_L=4\Omega$)
- Low Distortion.
 - : $\text{THD}=0.04\%$ (Typ.)
($V_{CC}=13.2\text{V}$, $f=1\text{kHz}$, $P_{OUT}=1\text{W}$, $R_L=4\Omega$, $G_V=50\text{dB}$)
- Low Noise.
 - : $V_{NO}=0.30\text{mV}_{\text{rms}}$ (Typ.)
($V_{CC}=13.2\text{V}$, $R_L=4\Omega$, $G_V=50\text{dB}$, $R_g=0\Omega$, $\text{BW}=20\text{Hz}\sim 20\text{kHz}$)
- Built-in stand-by function.
(With ④ pin set at low, power is turned OFF.)
- Built-in muting function.
(With ① pin set at low, $I_{SB}=1\mu\text{A(Typ.)}$ power is turned OFF.)
: $V(\text{Mute})=1\text{V(Typ.)}$
- Built-in various protection circuits
Protection circuits : Thermal shut down, over voltage, $\text{OUT}\rightarrow V_{CC}$ short, OUT-GND short and OUT-OUT short.
- Operating supply voltage : $V_{CC}=9\sim 18\text{V}$.



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MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Peak Supply Voltage (0.2sec)	V _{CC} surge	50	V
DC Supply Voltage	V _{CC} DC	25	V
Operating Supply Voltage	V _{CC} opr	18	V
Output Current (Peak)	I _o (Peak)	9	A
Power Dissipation	P _D	50	W
Operating Temperature	T _{opr}	-30~85	°C
Storage Temperature	T _{stg}	-55~150	°C

ELECTRICAL CHARACTERISTICS

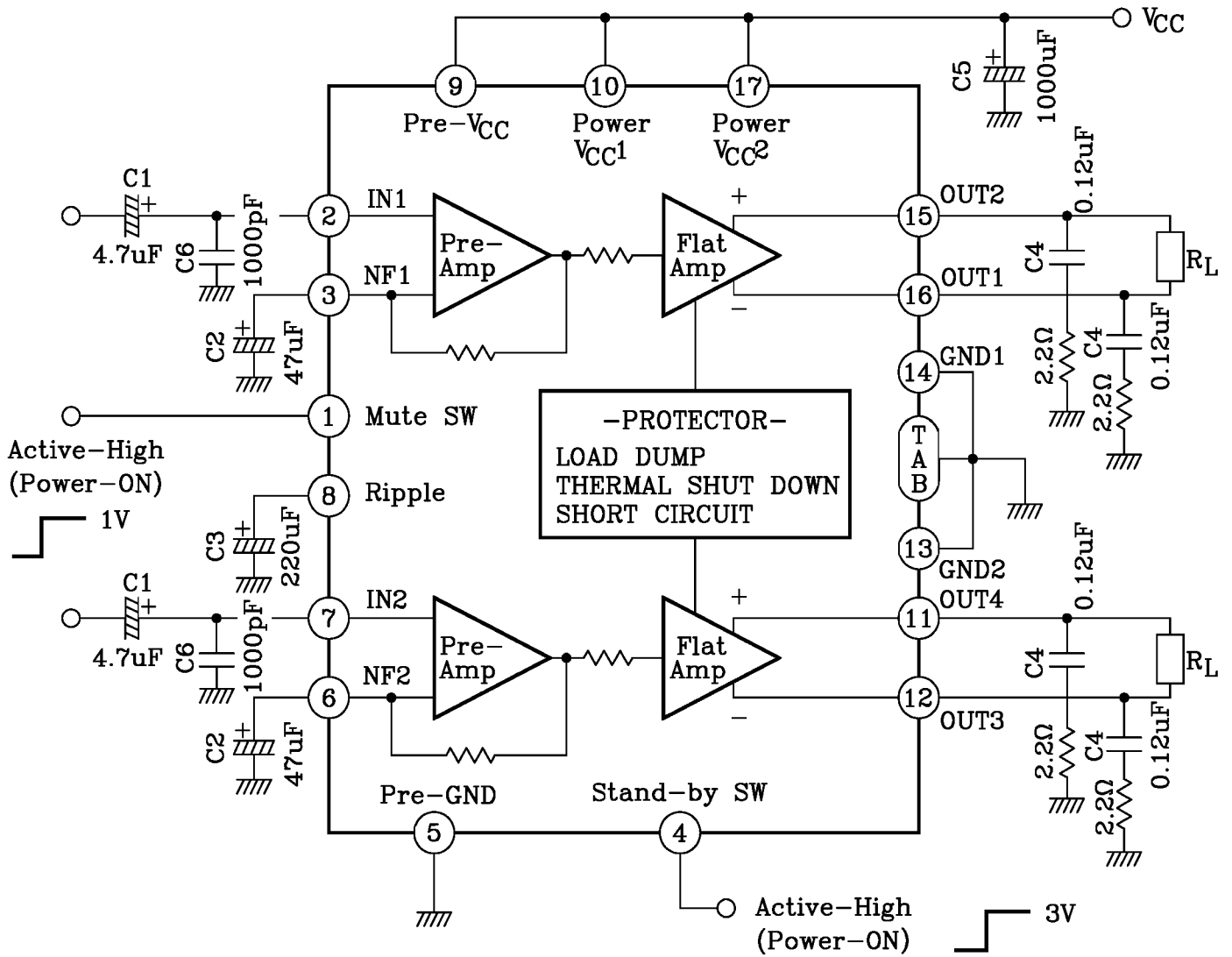
(Unless otherwise specified, V_{CC}=13.2V, R_L=4Ω, f=1kHz, Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Supply Current	I _{CCQ}	-	V _{IN} =0	-	120	250	mA
Output Power	P _{OUT(1)}	-	V _{CC} =14.4V, THD=10%	-	22	-	W
	P _{OUT(2)}	-	THD=10%	16	19	-	
Total Harmonic Distortion	THD	-	P _{OUT} =1W	-	0.04	0.4	%
Voltage Gain	G _V	-	-	48	50	52	dB
Output Noise Voltage	V _{NO}	-	R _g =0Ω, BW=20Hz~20kHz	-	0.30	0.70	mV _{rms}
Ripple Rejection Ratio	R.R	-	f _{ripple} =100Hz, R _g =600Ω	40	54	-	dB
Input Resistance	R _{IN}	-	-	-	30	-	kΩ
Output Offset Voltage	V _{offset}	-	V _{IN} =0	-300	0	300	mV
Current at Stand-by State	I _{SB}	-	-	-	1	10	μA
Cross Talk	C.T	-	R _g =600Ω, V _{OUT} =0dBm	-	60	-	dB
④ Pin Control Voltage	V _{SB}	-	Stand-by→OFF(Power→ON)	2.5	-	V _{CC}	V
① Pin Control Voltage	V _(MUTE)	-	Mute→ON (Power→OFF)	-	1.0	2.0	V

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BLOCK DIAGRAM AND TEST CIRCUIT

KIA6210AH ($G_V=50\text{dB}$)



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CAUTIONS AND APPLICATION METHOD
(Description is made only on the single channel.)

1. Voltage Gain Adjustment

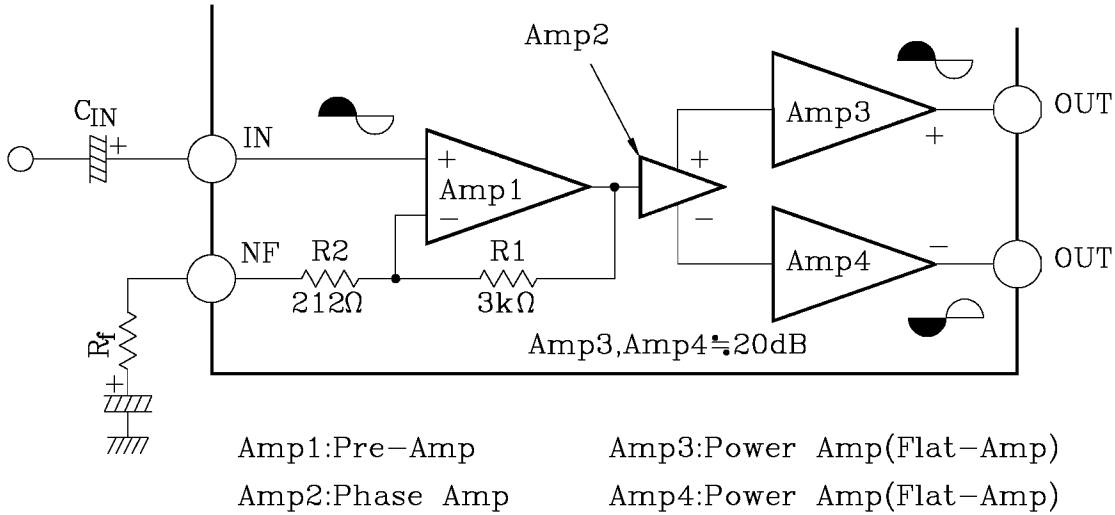


Fig.1

This IC has the amplifier construction as shown in Fig.1. The Pre-Amp (Amp 1) is provided to the primary stage, and the input voltage is amplified by the Flat Amps, Amp 3 and Amp 4 of each channel through the phase Amp (Amp 2). Since the input offset is prevented by Pre-Amp Vcc is set to ON, this circuit can remarkably reduce the pop noise. The total closed loop gain G_v of this IC can be obtained by expression below when the closed loop voltage gain of Amp 1 is G_{v1} .

$$G_{v1} = 20 \log \frac{R1 + (Rf + R2)}{Rf + R2} \text{ (dB)} \dots \dots \dots (1)$$

The closed loop voltage gain of POWER Amp (Amp 3 and 4) is fixed at

$$G_{v3} \cong G_{v4} = 20 \text{ dB}$$

Therefore, the total closed circuit voltage gain G_v is obtained through BTL connection by the expression below.

$$G_v = G_{v1} + G_{v3} + 6 \text{ (dB)} \dots \dots \dots (2)$$

For example, when $R_f = 0 \Omega$, G_v is obtained by the expression (1) and (2) as shown below.

$$G_v \cong 24 + 20 + 6 = 50 \text{ dB}$$

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The voltage gain is reduced when R_f is increased. (Fig.2)

With the voltage gain reduced, since (1) the oscillation stability is reduced, and (2) the pop noise changes when V_{cc} is set to ON, refer to the items 3 and 4.

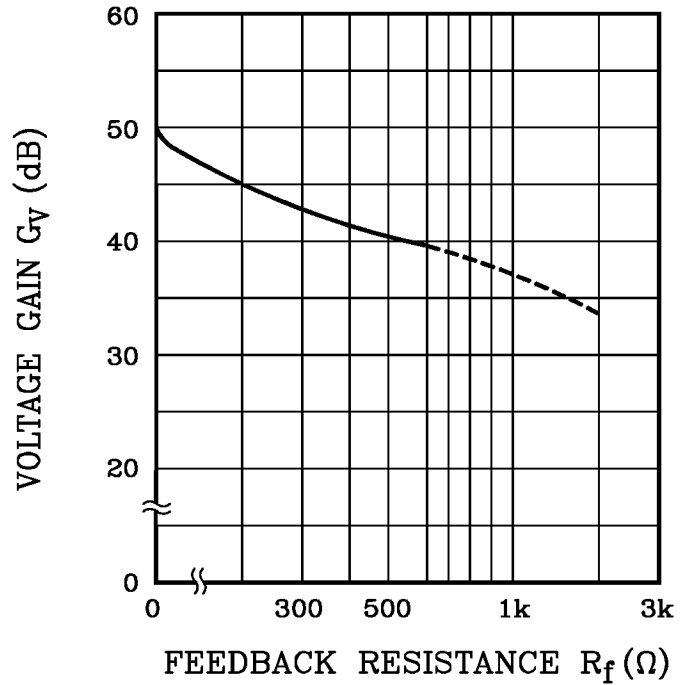
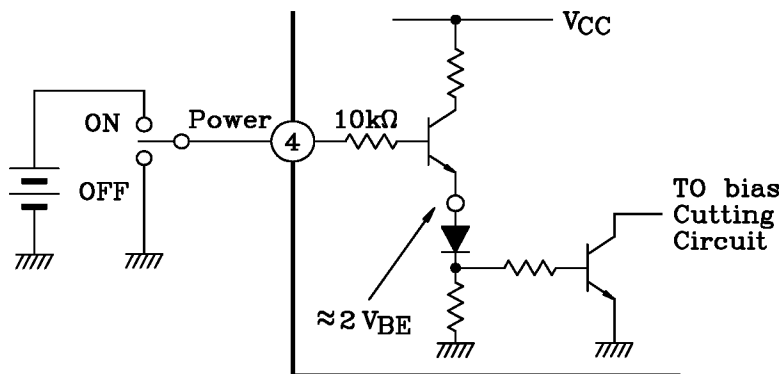


Fig. 2

2. Stand-by SW Function

By means of controlling ④ pin (Stand-by terminal) to High and Low, the power supply can be set to ON and OFF.

The threshold voltage of ④ pin is set at about 3V (Typ.), and the power supply current is about $1\mu A$ (Typ.) at the stand-by state.



(Fig.-3) With ④ Pin set to High, Power is turned ON.

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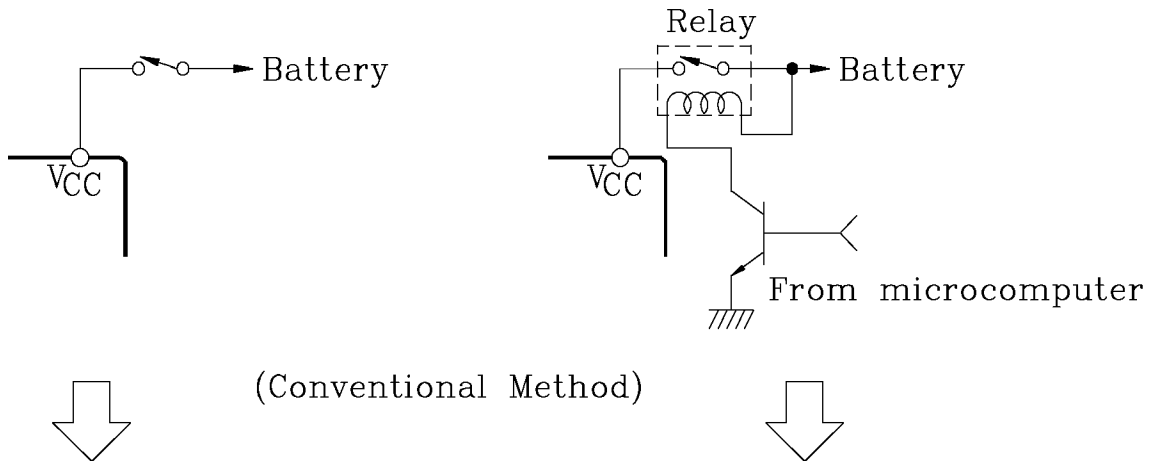
④ pin control voltage : $V(SB)$

Stand-By	Power	$V_{SB(V)}$
ON	OFF	0~2
OFF	ON	3~ V_{CC}

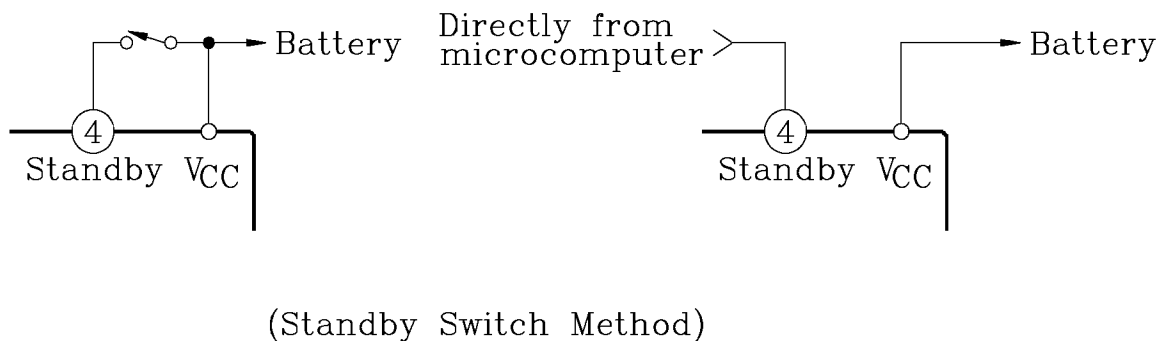
Advantage of Stand-by SW

- (1) Since V_{CC} can directly be controlled to ON/OFF by the microcomputer, the switching relay can be omitted.
- (2) Since the control current is microscopic, the switching relay of small current capacity is satisfactory for switching.

Large current capacity switch



Small current capacity switch



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3. Preventive Measure Against Oscillation

For preventing the oscillation, it is advisable to use C4, the condenser of polyester film having small characteristic fluctuation of the temperature and the frequency.

The resistance R to be series applied to C4 is effective for phase correction of high frequency, and improves the oscillation allowance.

Since the oscillation allowance is varied according to the causes described below, perform the temperature test to check the oscillation allowance.

- (1) Voltage gain to be used (Gv Setting)
- (2) Capacity value of condenser
- (3) Kind of condenser
- (4) Layout of printed board

In case of its use with the voltage gain Gv reduced or with the feedback amount increased, care must be taken because the phase-inversion is caused by the high frequency resulting in making the oscillation liable generated.

4. Input Offset Prevention Circuit At Vcc→ON

Having Pre-Amp (Amp 1) mounted on the primary stage, this IC contains the circuit for making the Amp1 input voltage and the NF terminal voltage equipotential.

Therefore, the offset voltage produced at the input stage is suppressed to prevent the pop noise at Vcc→ON. The capacity values of the input and NF condenser (C1 and C2) shall be set according to the gain to be used.

- (Reference)
- | | |
|-----|----------------------|
| (A) | At Gv=50dB (Rf=0Ω) |
| | C1=4.7μF, C2=47μF |
| (B) | At Gv=40dB (Rf=470Ω) |
| | C1=3.3μF, C2=33μF |

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5. Muting Function

Through setting ① pin (mute terminal) at about 1V or less, muting becomes possible. The interval circuit of IC is shown in Fig. 4.

When ① pin is set to Low, Q1 and Q2 are turned to ON, the charge of the ripple condenser is discharged and the bias is cut. The mute amount of 60dB or over can be obtained.

Since this muting function rapidly discharges the charge of the ripple filter capacitor of ⑧ pin, the pop noise is generated by the DC fluctuation of the bias section. Therefore, this muting function is not appropriate to the audio muting but is effective in muting at $V_{cc} \rightarrow ON$.

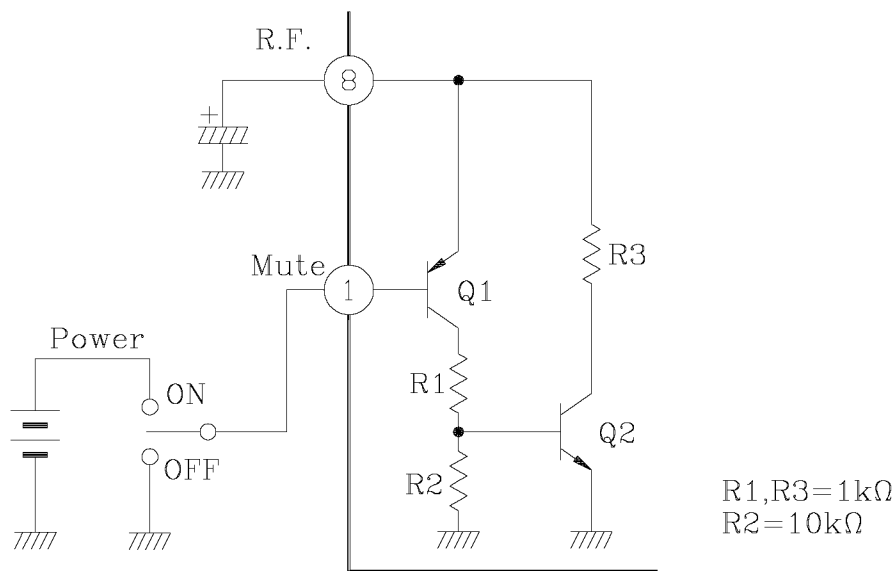


Fig.4 Mute Circuit

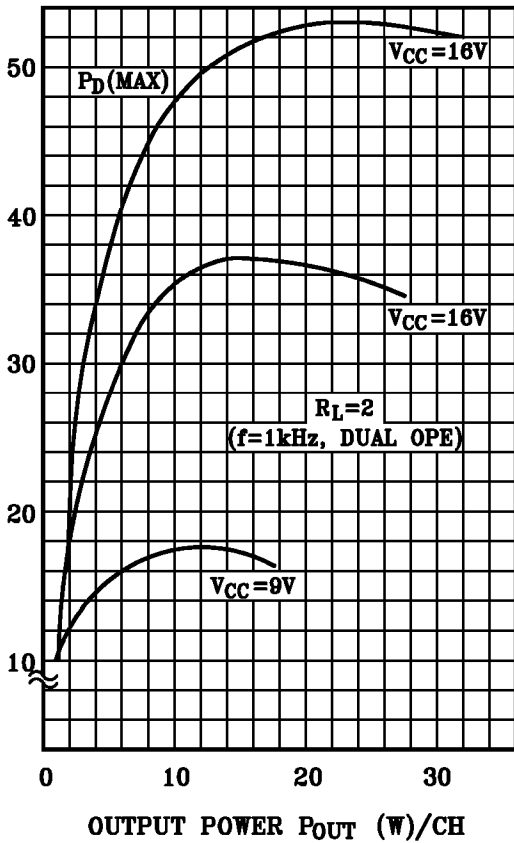
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6. External Part List And Description.

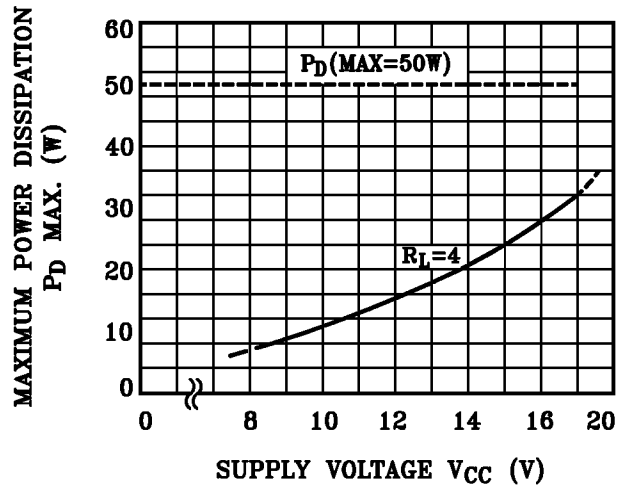
NAME OF PART	RECOMMENDED VALUE	OBJECT	INFLUENCE		REMARKS
			SMALLER THAN RECOMMENDED VALUE	LARGER THAN RECOMMENDED VALUE	
C ₁	4.7 μ F	DC blocking	Related to pop noise at Vcc→ON.		Related to gain. Refer to item 4.
C ₂	47 μ F	Feedback condenser	Related to pop noise at Vcc→ON.		
			Determination of low cut-off frequency. $C2 = \frac{1}{2\pi f_L \cdot R_f}$		
C ₃	220 μ F	Ripple reduction	Time constant is small at Vcc→ON or OFF.	Time constant is large at Vcc→ON or OFF.	
C ₄	0.12 μ F	Oscillation Prevention	Made liable to oscillate.	Oscillation allowance improved.	Refer to item 3.
C ₅	1000 μ F	Ripple Filter	For filtering power supply hum and ripple. Large at using AC rectified power supply. Small at using DC power supply.		

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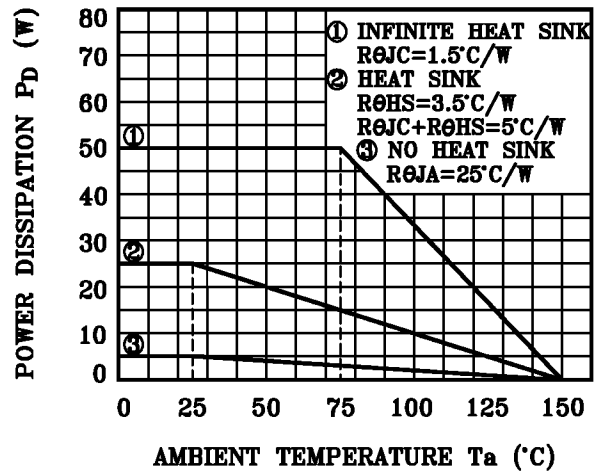
$P_{OUT} - P_D$



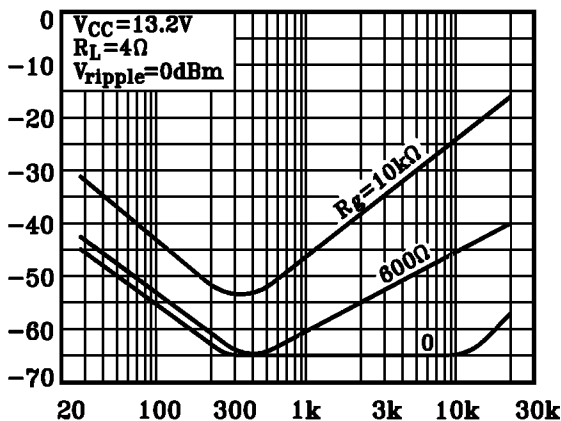
$P_D MAX - V_{CC}$



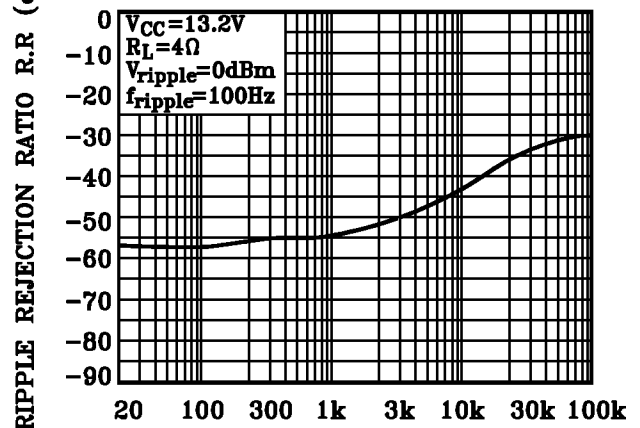
$P_D - T_a$



R.R - f



R.R - R_g



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