NEW

CRYSTAL OSCILLATOR
LOW-JITTER SPXO

SG - 210 S*H

- Frequency range : 80.000 MHz to 170.000 MHz
  Fundamental mode oscillator
- Supply voltage : 1.8 V / 2.5 V / 3.3 V
- Output : CMOS
- Function : Standby($\overline{ST}$)
- External dimensions : 2.5 × 2.0 × 0.8 mm

Pb Free RoHS Compliant

Product Number (please contact us)
SG-210SCH: X1G003931xxxx00
SG-210SDH: X1G003941xxxx00
SG-210SEH: X1G003951xxxx00

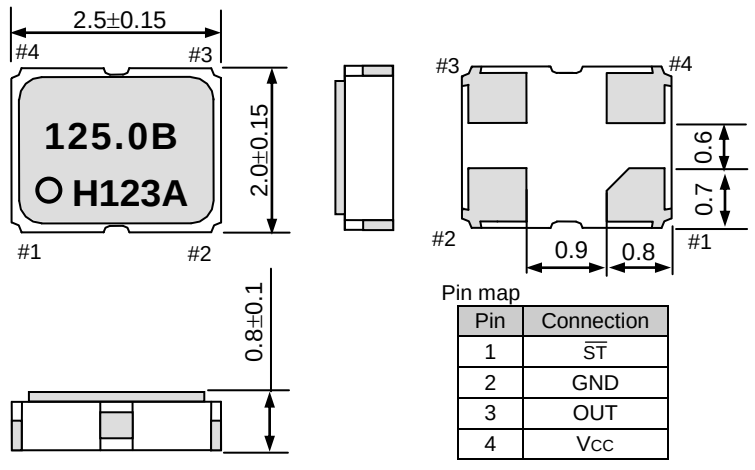
Actual size

Specifications (characteristics)

Item	Symbol	Specifications			Conditions / Remarks
		SG-210SEH	SG-210SDH	SG-210SCH	
Output frequency range	fo	80.000 MHz to 170.000 MHz			
		100MHz, 106.25MHz, 125MHz, 133.33MHz, 150MHz, 156.25MHz			Standard frequency. *1
Supply voltage	Vcc	1.8 V ± 10%	2.5 V ± 10%	3.3 V ± 10%	*2
Storage temperature	T_stg	-40 °C to +125 °C			Storage as single product.
Operating temperature	T_use	-40 °C to +85 °C			
Frequency tolerance	f_tol	B: ±50 × 10^{-6}, C: ±100 × 10^{-6}			-20 °C to +70 °C
		L: ±50 × 10^{-6}, M: ±100 × 10^{-6}			-40 °C to +85 °C
Current consumption	Icc	6.0 mA Max.	7.0 mA Max.	9.0 mA Max.	No load condition,80 MHz≤f0≤125 MHz
		8.0 mA Max.	9.0 mA Max.	11.0 mA Max.	No load condition,125 MHz<f0≤170 MHz
Stand-by current	I_std	10.0 µA Max.			$\overline{ST}$ =GND
Symmetry	SYM	45 % to 55 %			50 % Vcc level, L_CMOS ≤ 15 pF
Output voltage	VOH	90 % Vcc Min.			IOH = -4mA
	VOL	10 % Vcc Max.			IOL = 4mA
Output load condition (CMOS)	L_CMOS	15 pF Max.			
Input voltage	VIH	80 % Vcc Min.			$\overline{ST}$ terminal
	VIL	20 % Vcc Max.			
Rise time / Fall time	tr/ tf	3 ns Max.	2 ns Max.		20 % Vcc to 80 % Vcc level, L_CMOS ≤15 pF
Start-up time	t_str	5 ms Max.			T=0 at 90 % Vcc
Jitter *3	tp-p	22 ps Typ.	20 ps Typ.		Peak to Peak / L_CMOS ≤ 15 pF
Phase Jitter	tPJ	0.7 ps Max.	0.6 ps Max.		Offset frequency: 12kHz to 20MHz / L_CMOS ≤ 15 pF
Frequency aging	f_aging	±5 × 10^{-6} / year Max.			+25 °C, First year

*1 Please contact us for requirements not listed in the specification.
*2 fo ≥ 157MHz: Vcc ± 5%
*3 Based on SIA-3100C signal integrity analyzer made from WAVECREST.

External dimensions (Unit:mm)

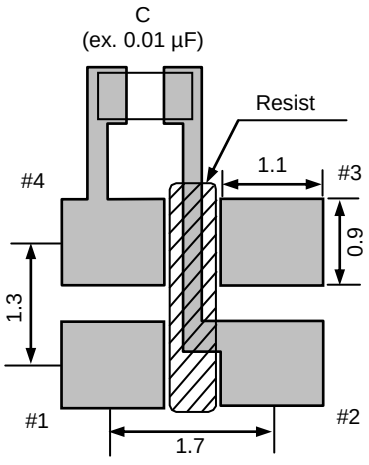


Pin map

Pin	Connection
1	$\overline{ST}$
2	GND
3	OUT
4	Vcc

Note.
$\overline{ST}$ pin = HIGH or "open": Specified frequency output.
$\overline{ST}$ pin = LOW : Output is high impedance, oscillation stops.

Footprint (Recommended) (Unit:mm)



To maintain stable operation, provide a 0.01uF to 0.1uF by-pass capacitor at a location as near as possible to the power source terminal of the crystal product (between Vcc - GND).