

# DATA SHEET

**TDA8708A**

Video analog input interface

Product specification  
Supersedes data of April 1993  
File under Integrated Circuits, IC02

June 1994

**Philips Semiconductors**



**PHILIPS**

## Video analog input interface

## TDA8708A

### FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- Binary or two's complement 3-state TTL outputs
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Power dissipation of 365 mW (typical)
- Input selector circuit (one out of three video inputs)
- Clamp and Automatic Gain Control (AGC) functions for CVBS and Y signals
- No sample-and-hold circuit required.
- The TDA8708A has white peak control in modes 1 and 2 whereas the TDA8708B has control in mode 1 only.

### APPLICATIONS

- Video signal decoding
- Scrambled TV (encoding and decoding)
- Digital picture processing
- Frame grabbing.

### GENERAL DESCRIPTION

The TDA8708A is an analog input interface for video signal processing. It includes a video amplifier with clamp and gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

### QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{CCA}$	analog supply voltage	4.5	5.0	5.5	V
$V_{CCD}$	digital supply voltage	4.5	5.0	5.5	V
$V_{CCO}$	TTL output supply voltage	4.2	5.0	5.5	V
$I_{CCA}$	analog supply current	–	37	45	mA
$I_{CCD}$	digital supply current	–	24	30	mA
$I_{CCO}$	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	$\pm 1$	LSB
DLE	DC differential linearity error	–	–	$\pm 0.5$	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (AGC amplifier)	12	18	–	MHz
$P_{tot}$	total power dissipation	–	365	500	mW

### ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8708A	28	DIP	plastic	SOT117-1
TDA8708AT	28	SO28L	plastic	SOT136-1

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BLOCK DIAGRAM

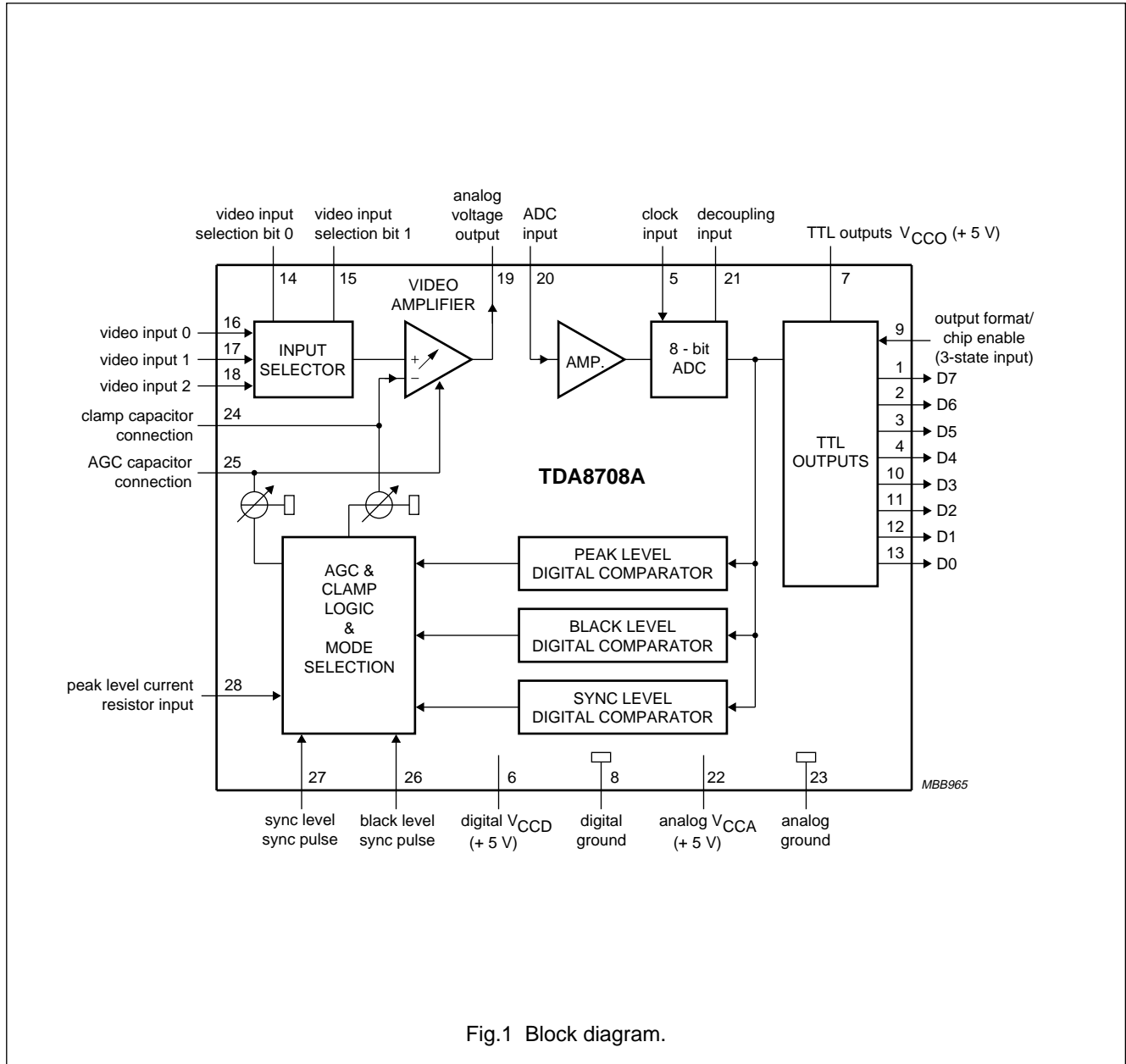


Fig.1 Block diagram.

Video analog input interface

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PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V <sub>CCD</sub>	6	digital supply voltage (+5 V)
V <sub>CCO</sub>	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
OF	9	output format/chip enable (3-state input)
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V <sub>CCA</sub>	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
AGC	25	AGC capacitor connection
GATE B	26	black level synchronization pulse
GATE A	27	sync level synchronization pulse
RPEAK	28	peak level current resistor input

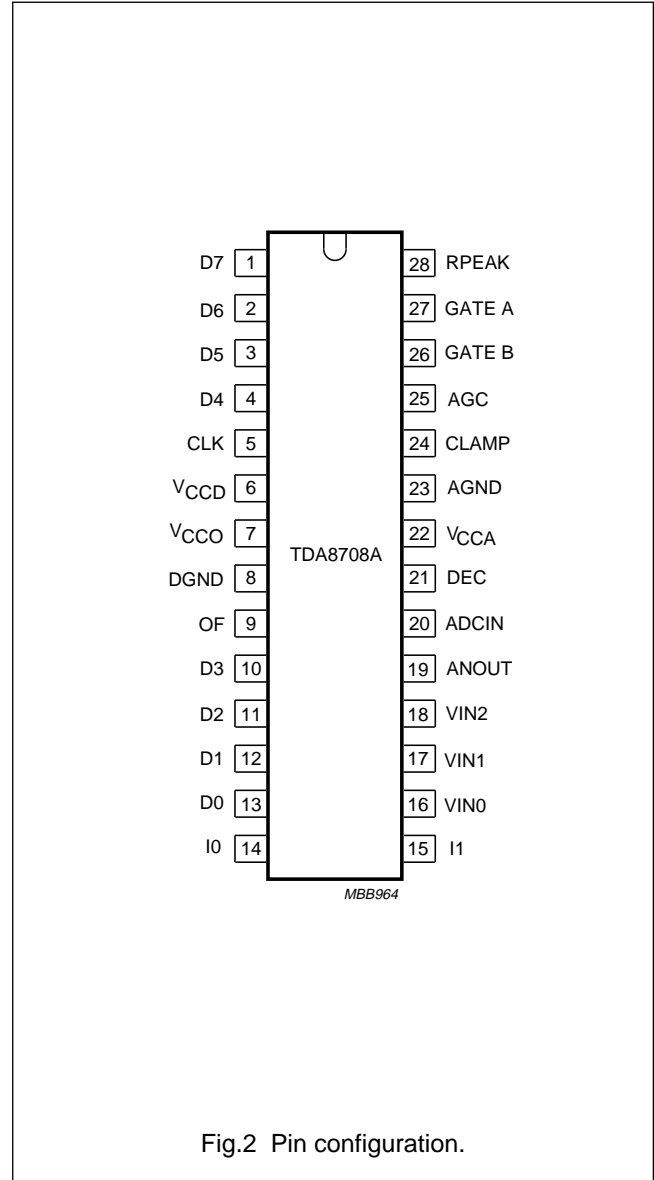


Fig.2 Pin configuration.

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**FUNCTIONAL DESCRIPTION**

The TDA8708A provides a simple interface for decoding video signals.

The TDA8708A operates in configuration mode 1 (see Fig.4) when the video signals are weak (i.e. when the gain of the AGC amplifier has not yet reached its optimum value). This enables a fast recovery of the synchronization pulses in the decoder circuit. When the pulses at the GATE A and GATE B inputs become distinct (GATE A and GATE B pulses are synchronization pulses occurring during the sync period and rear porch respectively) the TDA8708A automatically switches to configuration mode 2 (see Fig.5).

When the TDA8708A is in configuration mode 1, the gain of the AGC amplifier will be roughly adjusted (sync level to a digital output level of 0 and the peak level to a digital output level of 255).

In configuration mode 2 the digital output of the ADC is compared to internal digital reference levels. The resultant outputs control the charge or discharge current of a capacitor connected to the AGC pin. The voltage across this capacitor controls the gain of the video amplifier. This is the gain control loop.

The sync level comparator is active during a positive-going pulse at the GATE A input. This means that the sync pulse of the composite video signal is used as an amplitude reference. The bottom of the sync pulse is adjusted to obtain a digital output of logic 0 at the converter output. As the black level is at digital level 64, the sync pulse will have a digital amplitude of 64 LSBs.

The peak-white control loop is always active. If the video signal tends to exceed the digital code of 248, the gain will be limited to avoid any over-range of the converter.

The use of nominal signals will prevent the output from exceeding a digital code of 213 and the peak-white control loop will be non-active.

The clamp level control is accomplished by using the same techniques as used for the gain control. The black-level digital comparator is active during a positive-going pulse at the GATE B input. The clamp capacitor will be charged or discharged to adjust the digital output to code 64.

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
$V_{CCA}$	analog supply voltage	-0.3	+7.0	V
$V_{CCD}$	digital supply voltage	-0.3	+7.0	V
$V_{CCO}$	output supply voltage	-0.3	+7.0	V
$\Delta V_{CC}$	supply voltage difference between $V_{CCA}$ and $V_{CCD}$	-1.0	+1.0	V
	supply voltage difference between $V_{CCO}$ and $V_{CCD}$	-1.0	+1.0	V
	supply voltage difference between $V_{CCA}$ and $V_{CCO}$	-1.0	+1.0	V
$V_I$	input voltage	-0.3	$V_{CCA}$	V
$I_O$	output current	0	+10	mA
$T_{stg}$	storage temperature	-55	+150	°C
$T_{amb}$	operating ambient temperature	0	+70	°C
$T_j$	junction temperature	0	+125	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

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**CHARACTERISTICS**

$V_{CCA} = V_{22}$  to  $V_{23} = 4.5$  to  $5.5$  V;  $V_{CCD} = V_6$  to  $V_8 = 4.5$  to  $5.5$  V;  $V_{CCO} = V_7$  to  $V_8 = 4.2$  to  $5.5$  V; AGND and DGND shorted together;  $V_{CCA}$  to  $V_{CCD} = -0.5$  to  $+0.5$  V;  $V_{CCO}$  to  $V_{CCD} = -0.5$  to  $+0.5$  V;  $V_{CCA}$  to  $V_{CCO} = -0.5$  to  $+0.5$  V;  $T_{amb} = 0$  to  $+70$  °C; typical readings taken at  $V_{CCA} = V_{CCD} = V_{CCO} = 5$  V and  $T_{amb} = 25$  °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Supplies</b>						
$V_{CCA}$	analog supply voltage		4.5	5.0	5.5	V
$V_{CCD}$	digital supply voltage		4.5	5.0	5.5	V
$V_{CCO}$	TTL output supply voltage		4.2	5.0	5.5	V
$I_{CCA}$	analog supply current		–	37	45	mA
$I_{CCD}$	digital supply current		–	24	30	mA
$I_{CCO}$	TTL output supply current	TTL load (see Fig.8)	–	12	16	mA
<b>Video amplifier inputs</b>						
VIN(0 TO 2) INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	AGC load with external capacitor; note 1	0.6	–	1.5	V
$ Z_i $	input impedance	$f_i = 6$ MHz	10	20	–	k $\Omega$
$C_i$	input capacitance	$f_i = 6$ MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_I = 0.4$ V	–400	–	–	$\mu$ A
$I_{IH}$	HIGH level input current	$V_I = 2.7$ V	–	–	20	$\mu$ A
GATE A AND GATE B TTL INPUTS (SEE FIGS 4 AND 5)						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_I = 0.4$ V	–400	–	–	$\mu$ A
$I_{IH}$	HIGH level input current	$V_I = 2.7$ V	–	–	20	$\mu$ A
$t_W$	pulse width	see Fig.5	2	–	–	$\mu$ s
RPEAK INPUT (PIN 28)						
$I_{28(min)}$	minimum peak level current	$R_{28} = 0$ $\Omega$	–	80	150	$\mu$ A
AGC INPUT (PIN 25)						
$V_{25(min)}$	AGC voltage for minimum gain		–	2.8	–	V
$V_{25(max)}$	AGC voltage for maximum gain		–	4.0	–	V
	AGC output current		see Table 2			
CLAMP INPUT (PIN 24)						
$V_{24}$	clamp voltage for code 128 output		–	3.5	–	V
$I_{24}$	clamp output current		see Table 3			

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Video amplifier outputs</b>						
ANOUT OUTPUT (PIN 19)						
$V_{19(p-p)}$	AC output voltage (peak-to-peak value)	$V_{VIN} = 1.33 \text{ V (p-p)}$ ; $V_{25} = 3.6 \text{ V}$	–	1.33	–	V
$I_{19}$	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p-p)}$	output current driven by the load	$V_{ANOUT} = 1.33 \text{ V (p-p)}$ ; note 2	–	–	1.0	mA
$V_{19}$	DC output voltage for black level	note 3	–	$V_{CCA} - 2.24$	–	V
$Z_{19}$	output impedance		–	20	–	$\Omega$
<b>Video amplifier dynamic characteristics</b>						
$\alpha_{ct}$	crosstalk between VIN inputs	$V_{CCA} = 4.75 \text{ to } 5.25 \text{ V}$	–	–50	–45	dB
$G_{diff}$	differential gain	$V_{VIN} = 1.33 \text{ V (p-p)}$ ; $V_{25} = 3.6 \text{ V}$	–	2	–	%
$\varphi_{diff}$	differential phase	$V_{VIN} = 1.33 \text{ V (p-p)}$ ; $V_{25} = 3.6 \text{ V}$	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
$\Delta G$	gain range	see Fig.10	–4.5	–	+6.0	dB
$G_{stab}$	gain stability as a function of supply voltage and temperature	see Fig.10	–	–	5	%
<b>Analog-to-digital converter inputs</b>						
CLK INPUT (PIN 5)						
$V_{IL}$	LOW level input voltage		0	–	0.8	V
$V_{IH}$	HIGH level input voltage		2.0	–	$V_{CCD}$	V
$I_{IL}$	LOW level input current	$V_{clk} = 0.4 \text{ V}$	–400	–	–	$\mu\text{A}$
$I_{IH}$	HIGH level input current	$V_{clk} = 2.7 \text{ V}$	–	–	100	$\mu\text{A}$
$ Z_i $	input impedance	$f_{clk} = 10 \text{ MHz}$	–	4	–	k $\Omega$
$C_i$	input capacitance	$f_{clk} = 10 \text{ MHz}$	–	4.5	–	pF
OF INPUT (3-STATE; SEE TABLE 4)						
$V_{IL}$	LOW level input voltage		0	–	0.2	V
$V_{IH}$	HIGH level input voltage		2.6	–	$V_{CCD}$	V
$V_9$	input voltage in high impedance state		–	1.15	–	V
$I_{IL}$	LOW level input current		–370	–300	–	$\mu\text{A}$
$I_{IH}$	HIGH level input current		–	300	450	$\mu\text{A}$

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>ADCIN INPUT (PIN 20; SEE TABLE 5)</b>						
V <sub>20</sub>	input voltage	digital output = 00	–	V <sub>CCA</sub> – 2.42	–	V
V <sub>20</sub>	input voltage	digital output = 255	–	V <sub>CCA</sub> – 1.41	–	V
V <sub>20(p-p)</sub>	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I <sub>20</sub>	input current		–	1.0	10	μA
Z <sub>i</sub>	input impedance	f <sub>i</sub> = 6 MHz	–	50	–	MΩ
C <sub>1</sub>	input capacitance	f <sub>i</sub> = 6 MHz	–	1	–	pF
<b>Analog-to-digital converter outputs</b>						
DIGITAL OUTPUTS D0 TO D7						
V <sub>OL</sub>	LOW level output voltage	I <sub>OL</sub> = 2 mA	0	–	0.6	V
V <sub>OH</sub>	HIGH level output voltage	I <sub>OL</sub> = –0.4 mA	2.4	–	V <sub>CCD</sub>	V
I <sub>OZ</sub>	output current in 3-state mode	0.4 V < V <sub>O</sub> < V <sub>CCD</sub>	–20	–	+20	μA
<b>Switching characteristics</b>						
f <sub>clk(max)</sub>	maximum clock input frequency	see Fig.6; note 6	30	32	–	MHz
<b>Analog signal processing (f<sub>clk</sub> = 32 MHz; see Fig.8)</b>						
G <sub>diff</sub>	differential gain	V <sub>20</sub> = 1.0 V (p-p); see Fig.3; note 7	–	2	–	%
Φ <sub>diff</sub>	differential phase	see Fig.3; note 7	–	2	–	deg
f <sub>1</sub>	fundamental harmonics (full-scale)	f <sub>i</sub> = 4.43 MHz; note 7	–	–	0	dB
f <sub>all</sub>	harmonics (full-scale); all components	f <sub>i</sub> = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
<b>Transfer function (see Fig.8)</b>						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
<b>Timing (f<sub>clk</sub> = 32 MHz; see Figs 6, 7 and 8)</b>						
DIGITAL OUTPUTS (C <sub>L</sub> = 15 pF; I <sub>OL</sub> = 2 mA; R <sub>L</sub> = 2 kΩ)						
t <sub>ds</sub>	sampling delay time		–	2	–	ns
t <sub>h</sub>	output hold time		6	8	–	ns
t <sub>d</sub>	output delay time		–	16	20	ns
t <sub>dEZ</sub>	3-state delay time; output enable		–	19	25	ns
t <sub>dDZ</sub>	3-state delay time; output disable		–	14	20	ns



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**Notes**

1. 0 dB is obtained at the AGC amplifier when applying  $V_{i(p-p)} = 1.33$  V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance  $R_L$  should be referenced to  $V_{CCA}$  and defined as:
  - a) AC impedance  $\geq 1$  k $\Omega$  and the DC impedance  $> 2.7$  k $\Omega$ .
  - b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Control mode 2 is selected.
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

$$\frac{S}{N} = 20 \log \frac{V_{ANOUTC(p-p)}}{V_{ANOUTY(RMS\ noise)}} \text{ at } B = 5 \text{ MHz.}$$

5. The voltage ratio is expressed as:

$$SVRR1 = 20 \log \frac{\Delta V_{CCA}}{V_{CCA}} \times \frac{G}{\Delta G} \text{ for } V_I = 1 \text{ V (p-p), gain at 100 kHz} = 1 \text{ and 1 V supply variation.}$$

6. It is recommended that the rise and fall times of the clock are  $\geq 2$  ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

$$SVRR2 = \frac{\Delta (V_{I(00)} - V_{I(FF)}) + (V_{I(00)} - V_{I(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave ( $f_i = 4.4$  MHz;  $f_{clk} = 27$  MHz).

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**Table 1** Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN2

**Table 2** AGC output current.

GATE A	GATE B	DIGITAL OUTPUT	I <sub>AGC</sub>	MODE <sup>(2)</sup>
1	1	output < 255	-2.5 μA	1
		output > 255	I <sub>AGCM</sub>	1
0	X <sup>(1)</sup>	output < 248	0 μA	2
		output > 248	I <sub>AGCM</sub>	2
1	0	output < 0	+2.5 μA	2
		0 < output < 248	-2.5 μA	2
		output > 248	I <sub>AGCM</sub>	2

**Note**

1. X = don't care.
2. Mode 2 can only be initialized with successive pulses on GATE A and GATE B (see Fig.5).

**Table 5** Output coding and input voltage (typical values).

STEP	V <sub>ADCIN</sub>	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V <sub>CCA</sub> – 2.41 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V <sub>CCA</sub> – 1.41 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

**Table 3** CLAMP output current.

GATE A	GATE B	DIGITAL OUTPUT	I <sub>CLAMP</sub>	MODE
1	1	output < 0	I <sub>CLAMP</sub> PM	1
		output > 0	-2.5 μA	1
X <sup>(1)</sup>	0	X <sup>(1)</sup>	0 μA	2
0	1	output < 64	+50 μA	2
		64 < output	-50 μA	2

**Note**

1. X = don't care.

**Table 4** OF input coding.

OF	D0 TO D7
0	active, two's complement
1	high impedance
open circuit <sup>(1)</sup>	active, binary

**Note**

1. Use C ≥ 10 pF to DGND.

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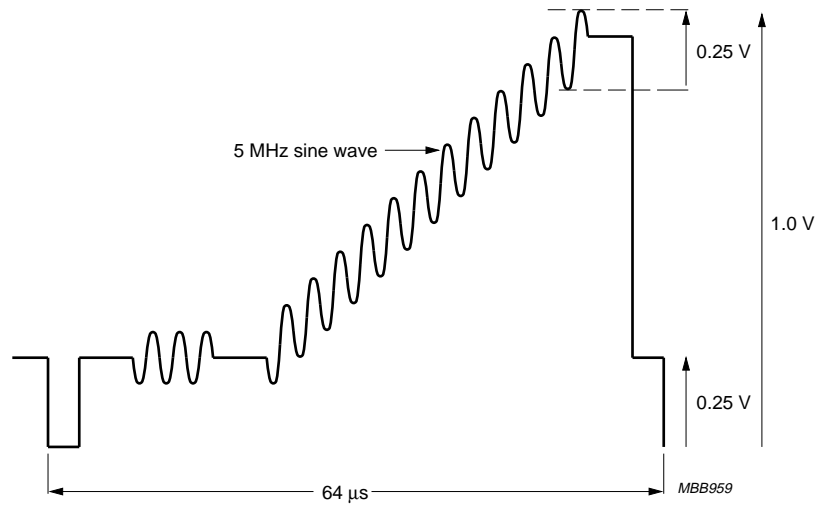


Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

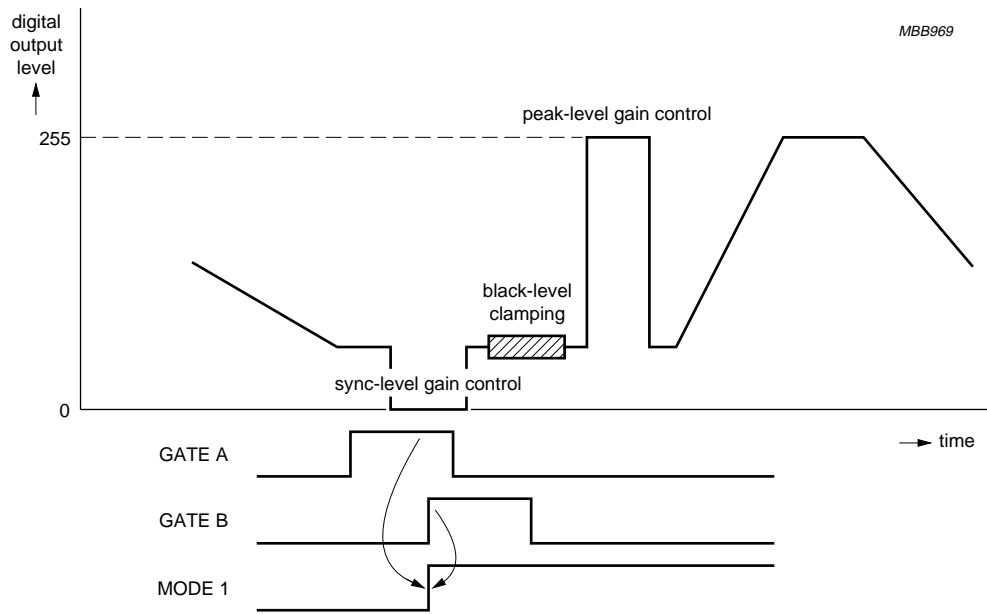


Fig.4 Control mode 1.

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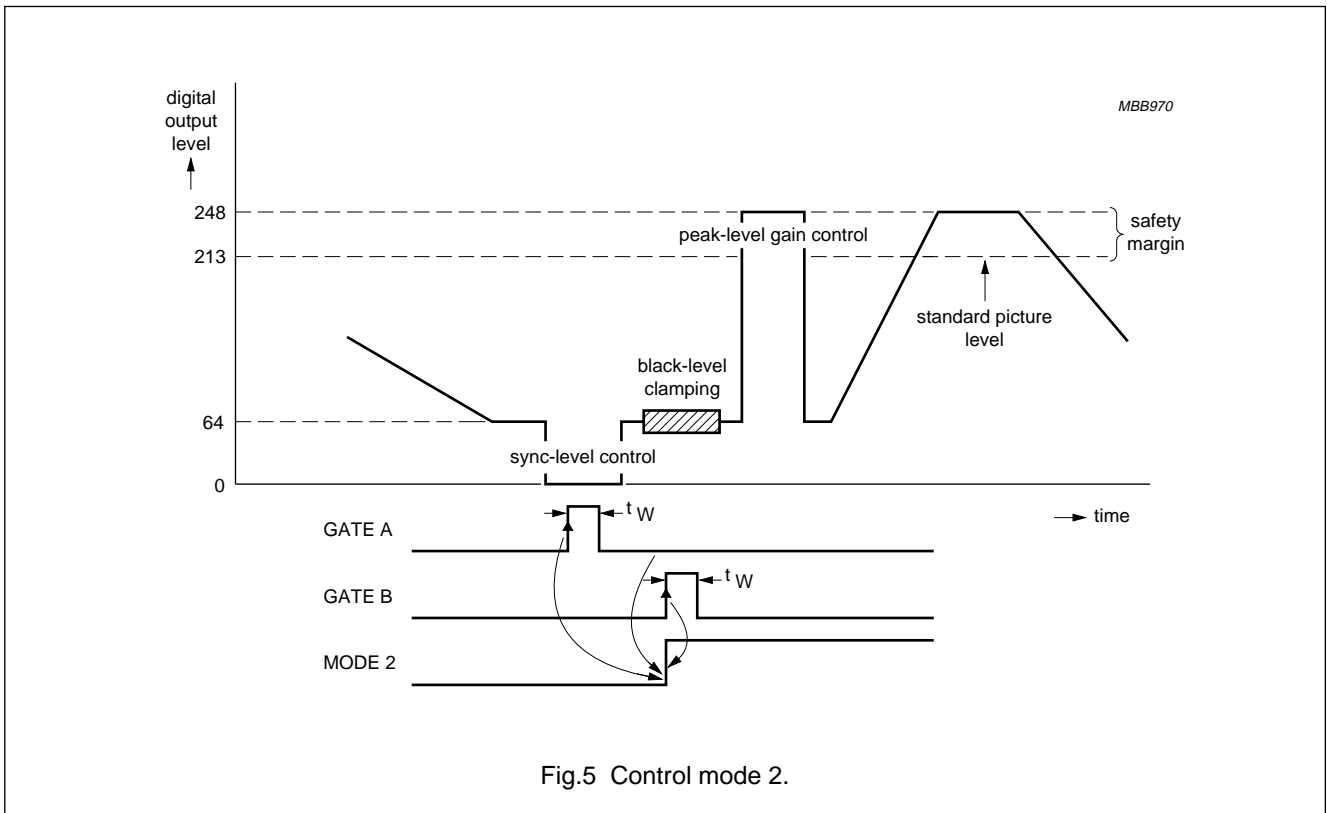


Fig.5 Control mode 2.

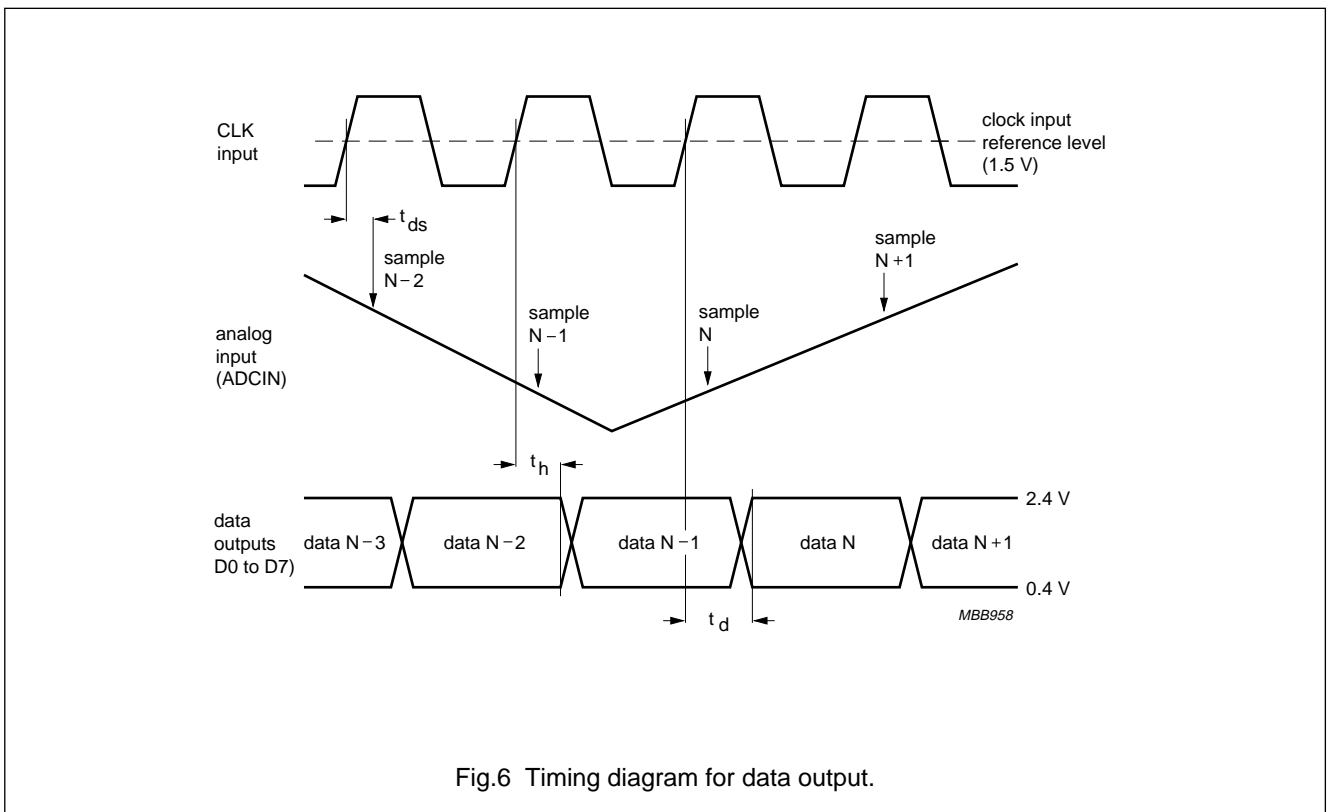


Fig.6 Timing diagram for data output.

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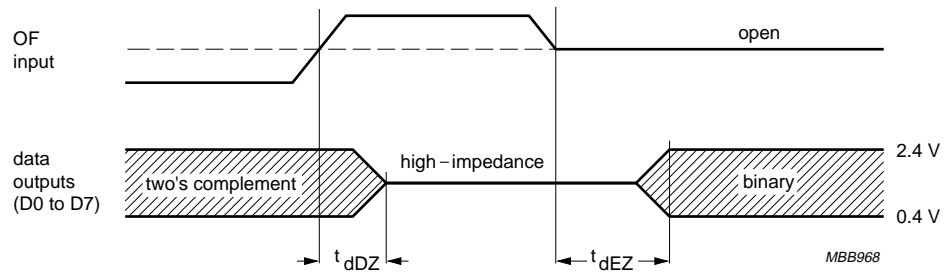


Fig.7 Output format timing diagram.

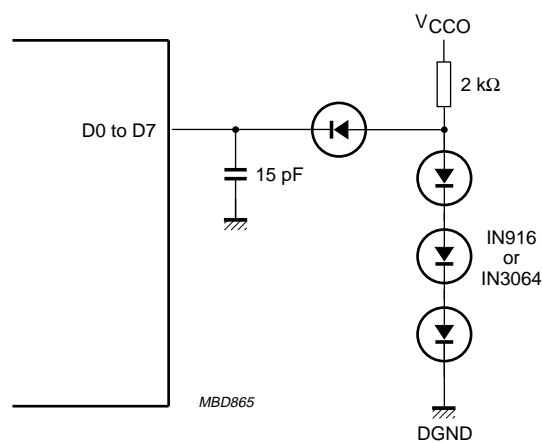


Fig.8 Load circuit for timing measurement; data outputs (OF = LOW or open-circuit).

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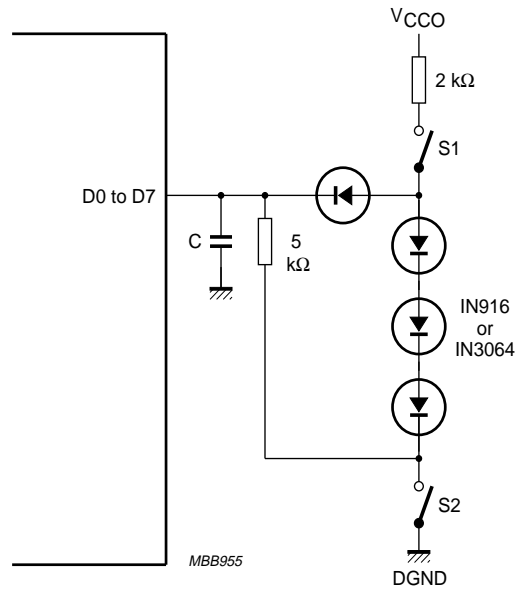
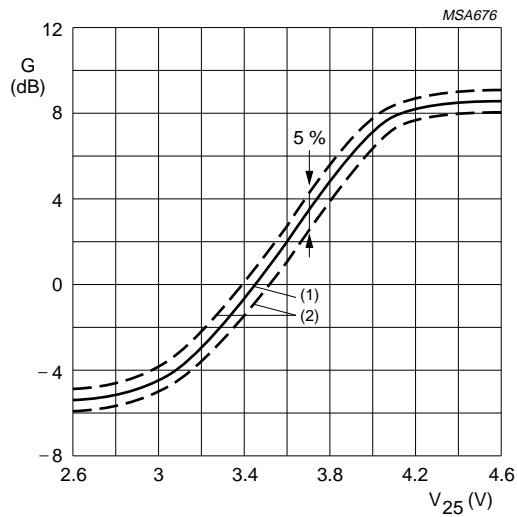


Fig.9 Load circuit for timing measurement; 3-state outputs (OF:  $f_i = 1$  MHz;  $V_{OF} = 3$  V).



- (1) Typical value ( $V_{CCA} = V_{CCD} = 5$  V;  $T_{amb} = 25$  °C).
- (2) Minimum and maximum values (temperature and supply).

Fig.10 Gain control curve.

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INTERNAL PIN CIRCUITRY

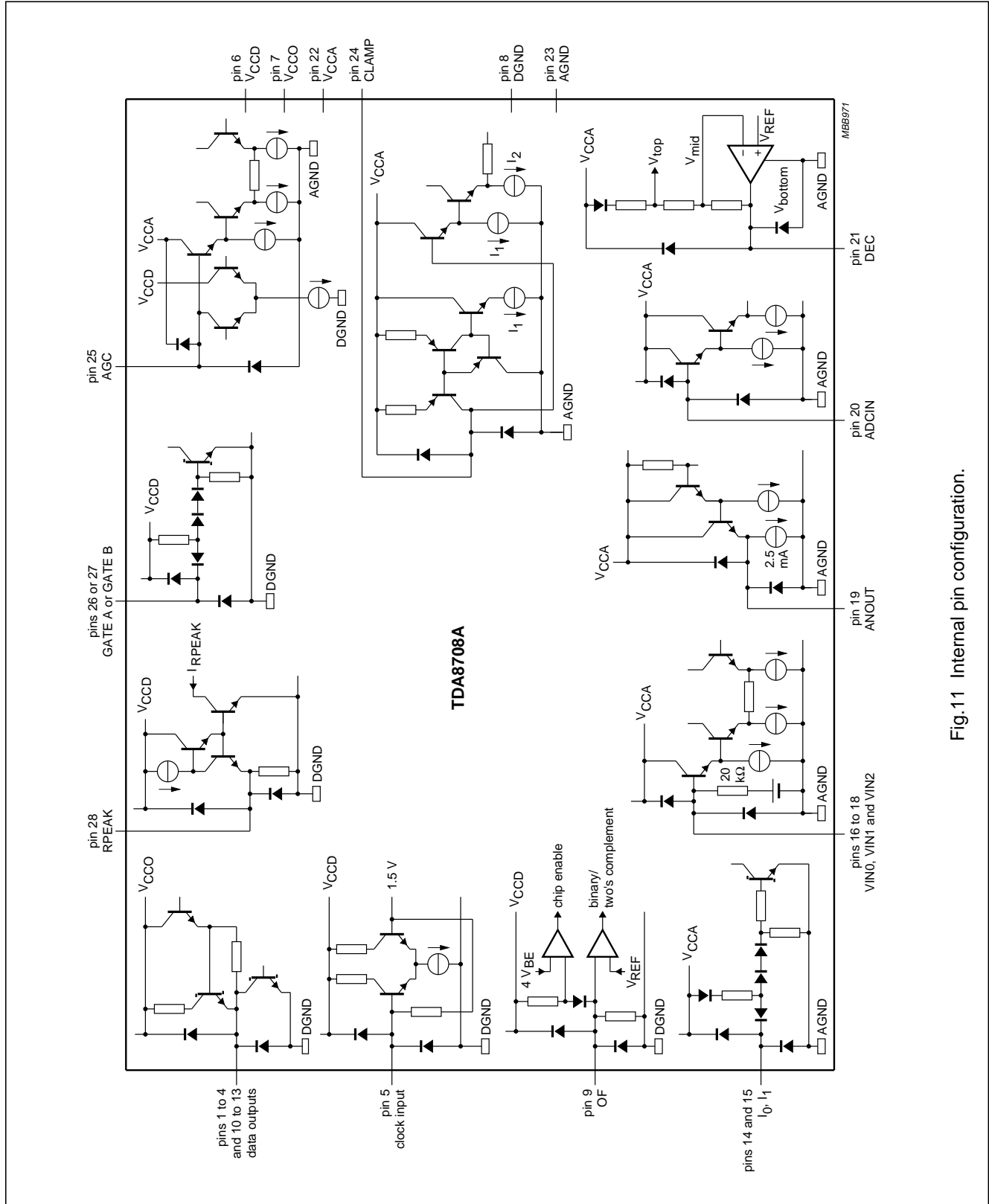


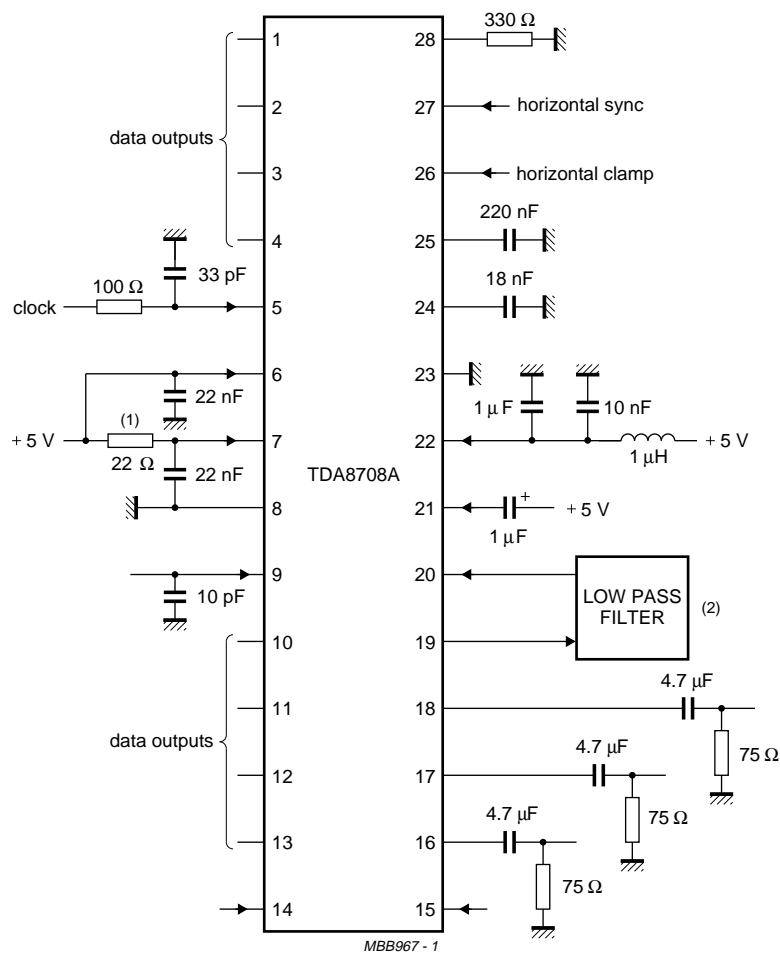
Fig.11 Internal pin configuration.

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APPLICATION INFORMATION

Additional information can be found in the laboratory report "FBL/AN9308".



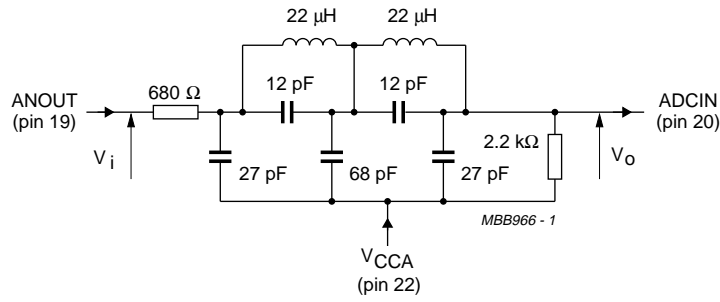
- (1) It is recommended to decouple V<sub>CCO</sub> through a 22 Ω resistor especially when the output data of TDA8708A interfaces with a capacitive CMOS load device.
- (2) See Figs 13 and 15 for examples of the low-pass filters.

Fig.12 Application diagram.



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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.13 Example of a low-pass filter for CVBS and Y signals.

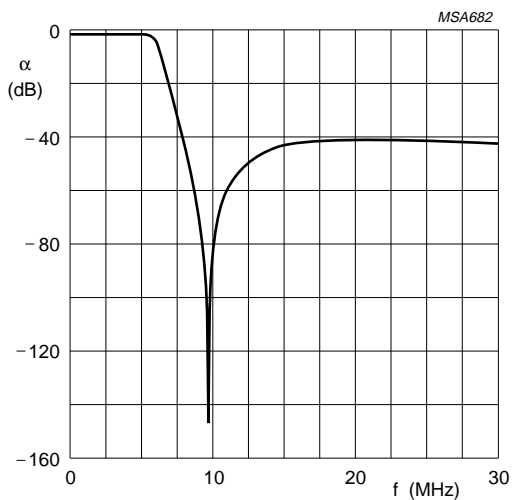


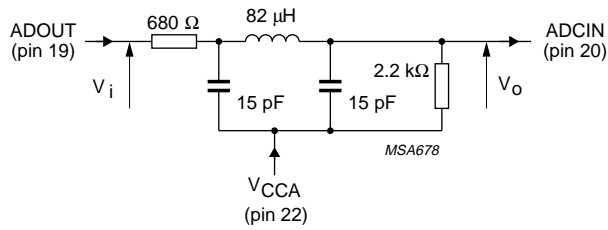
Fig.14 Frequency response for filter shown in Fig.13.

Characteristics of Fig. 13

- Order 5; adapted CHEBYSHEV
- Ripple  $\rho \leq 0.4$  dB
- $f = 6.5$  MHz at  $-3$  dB
- $f_{\text{notch}} = 9.75$  MHz.

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This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680  $\Omega$  and 2.2 k $\Omega$  must in any event be applied.

Fig.15 Example of an economical low-pass filter for CVBS and Y signals.

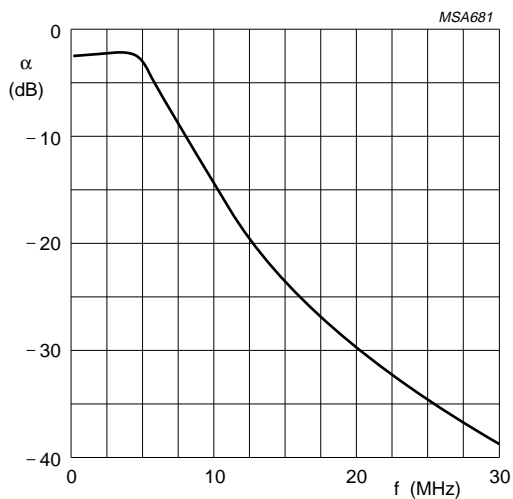


Fig.16 Frequency response for filter shown in Fig.15.

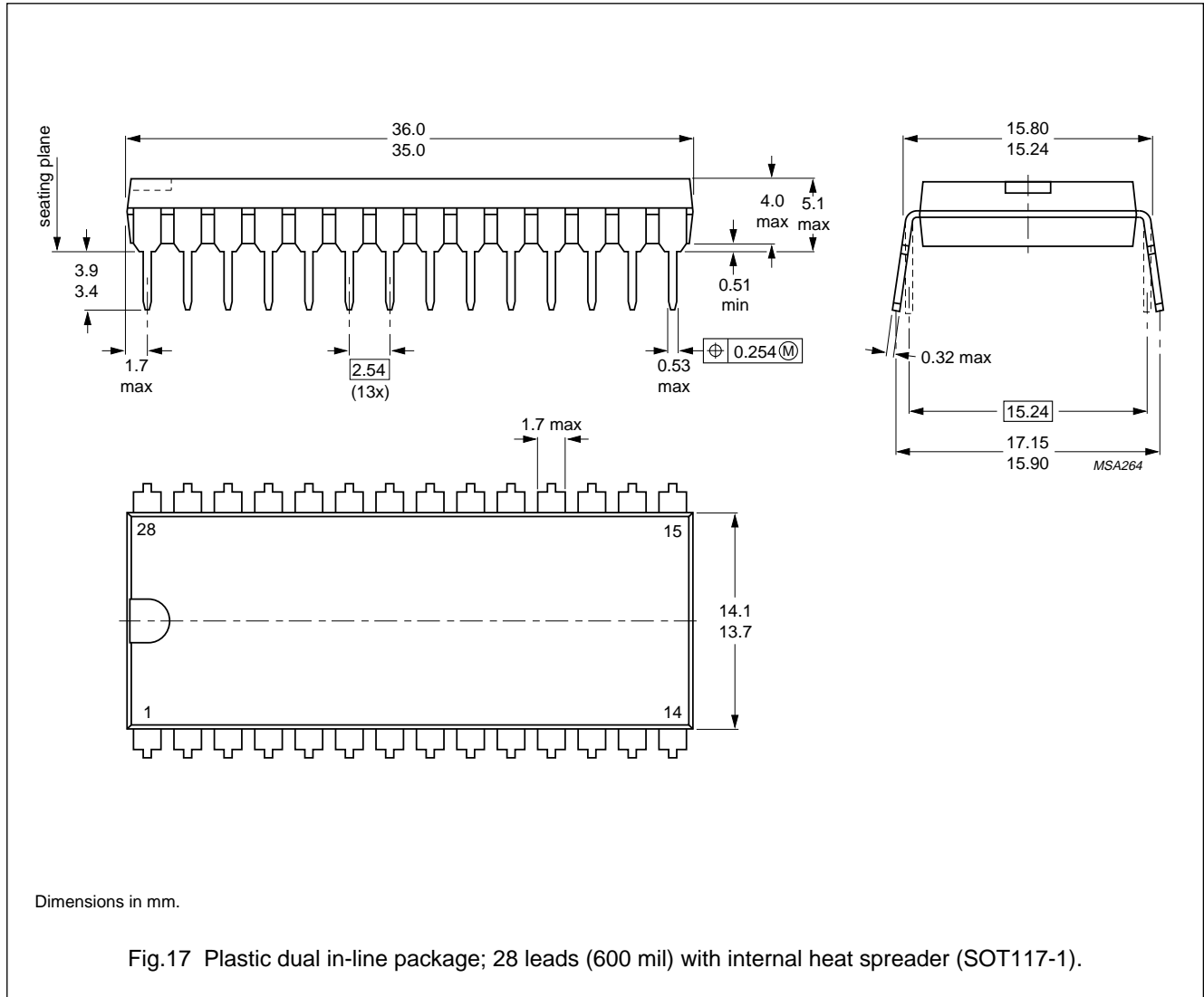
**Characteristics of Fig. 15**

- Order 5; adapted CHEBYSHEV
- Ripple  $\rho \leq 0.4$  dB
- $f = 6.5$  MHz at  $-3$  dB.

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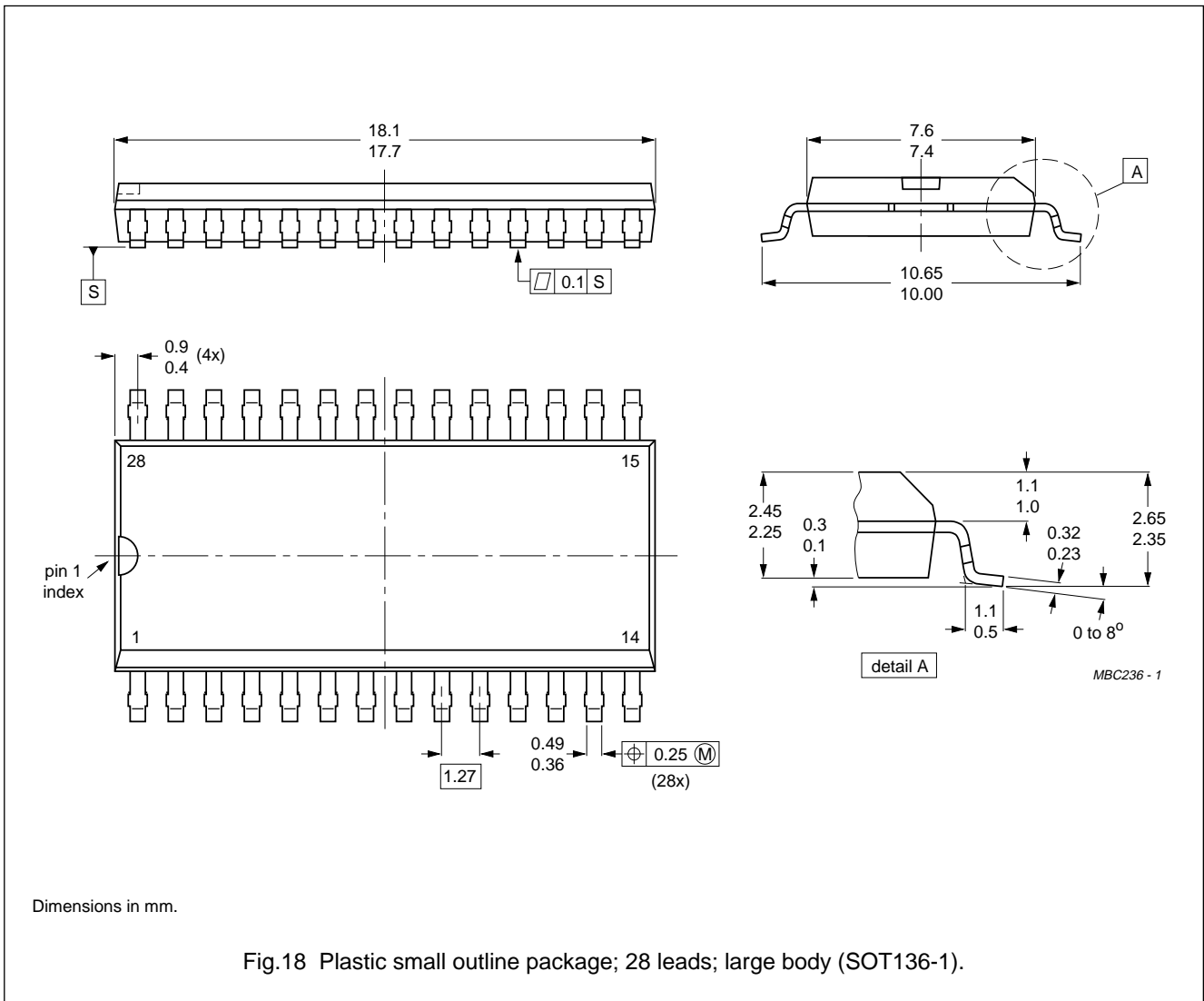
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PACKAGE OUTLINES



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### SOLDERING

#### Plastic dual in-line packages

##### BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

#### Plastic small-outline packages

##### BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

##### BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

##### REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

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**DEFINITIONS**

<b>Data sheet status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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## Philips Semiconductors – a worldwide company

**Argentina:** IEROD, Av. Juramento 1992 - 14.b, (1428)  
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**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
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**Austria:** Triester Str. 64, A-1101 WIEN, P.O. Box 213,  
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**Brazil:** Rua do Rocio 220 - 5<sup>th</sup> floor, Suite 51,  
CEP: 04552-903-SÃO PAULO-SP, Brazil.  
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Tel. (011)821-2327, Fax. (011)829-1849

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**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
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**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
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**France:** 4 Rue du Port-aux-Vins, BP317,  
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Tel. (01)4099 6161, Fax. (01)4099 6427

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**India:** Philips INDIA Ltd, Components Dept,  
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**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
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**Japan:** Philips Bldg 13-37, Kohnan2-chome, Minato-ku, TOKYO 108,  
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**Spain:** Balmes 22, 08007 BARCELONA,  
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**Sweden:** Kottbygatan 7, Akalla. S-164 85 STOCKHOLM,  
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**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
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**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. (0212)279 2770, Fax. (0212)269 3094

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Philips House, Torrington Place, LONDON, WC1E 7HD,  
Tel. (071)436 41 44, Fax. (071)323 03 42

**United States:** INTEGRATED CIRCUITS:  
811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. (800)234-7381, Fax. (708)296-8556  
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