



Migrating to Macronix MX25L25635F from Spansion S25FL256S

1. Introduction

This application note is the migration guide for migrating to Macronix MX25L25635F from Spansion S25FL256S. The document does not provide detailed information on individual device, but highlights the similarities and differences between them. The comparison covers the general features, performance, command codes and other differences.

The information provided is based on the data available at the time the document was released. Macronix MX25L25635F and Spansion S25FL256S datasheets may override this application note if there is a different description for the same specification in the datasheets.

Please refer to the contents and comparison tables below for more details.



2. General Features

2-1. Feature Comparison

Table 2-1. Feature Comparison Table

Company	Macronix	Spansion
Part No.	MX25L25635F	S25FL256S
VCC	2.7V-3.6V	2.7V-3.6V
Architecture		
I/O	1-1-1 1-1-2/1-2-2 1-1-4/1-4-4	1-1-1 1-1-2/1-2-2 1-1-4/1-4-4
DTR	N/A	66MHz (3.0V-3.6V)
QPI Interface	V	N/A
Sector Size	4KB/32KB/64KB	4KB/64KB
Program Buffer Size	256Byte	256Byte/512Byte
Security OTP	512 Byte	1K Byte
Features		
Program/ Erase Suspend & Resume	V	V
Read Enhance Mode	V	V
Read Burst Mode	V	N/A
Configurable Dummy Cycle	V	V
Adjustable Output Driver	V	N/A
Fast Boot (XIP) Mode	V	V
S/W Reset Command	V	V
Reset# Pin	V	V (16SOP, 24BGA)
BP Protect	Top/Bottom	Top/Bottom
Password Protection	V	V
Volatile Write Protection	V	V
Non-volatile Write Protection	V	V



3. Address Protocol Support

Table 3-1. Address Protocol

		4Byte Mode	Extended Address Register (EAR)	4Byte command set
Spansion	S25LF256S	V	V	V
Micronix	MX25L25635F	V	V	V

Both Macronix and Spansion support three kinds of address protocols:

"4Byte Mode addressing"

"Extended Address Register (EAR)"

"4Byte Command Set"

However, there are some differences between the MX25L25635F and S25FL256S. In the following section we'll point out those differences.

 Table 3-2. Related Command Set

	Instruction	Description	Macronix MX25L25635F	Spansion S25FL256S
	EN4B	Enter 4-byte address mode	B7h	-
	EX4B	Exit 4-byte address mode	E9h	-
4Byte ADD	RDEAR	Read Extended Address Register	C8h	16h
Approach	WREAR	Write Extended Address Register	C5h	17h
		Access Extended Address Register	-	B9h
		Write Register	-	01h



3-1. 4Byte Mode:

Issue Enter 4-Byte mode command to set up the 4BYTE bit in Configuration Register. After 4BYTE bit has been set, the device enter 4-byte Address mode, the number of address bits for all instructions become 32-bit.

	Spansion	Macronix
Related Register	Bank Address Register (BAR)	Configuration Register (CR)
Related Bit	Bit [7] - EXTADD	Bit [5]- 4Byte
Enable/Write Command	BRWR(17h)	EN4B(B7h)
Disable/Clear Command	BRWR(17h)	EX4B(E9h)
WREN	Not required	Not required

3-1-1. S25FL256S

Table 3-3. Related Register: Bank Register

Bits	Description	Bit Status	Default Status	Туре
7	EXTADD (Extended Address Enable)	1= 4 byte address 0=3byte address+ Bank address	0	Volatile
6 to 1	RFU		000000	Volatile
0	A24 (Bank address)	A24 for 256Mb	0	Volatile

Entry 4Byte Mode Method

1. Using "Bank Register Write (17h)" command to update the Bit 7 (EXTADD) value of Bank Register to enable or disable the 4Byte address mode.

Exit 4Byte Mode

Power-on or Reset cycle.

3-1-2. MX25L25635F

Table 3-4. Related Register: Configuration Register

Bits	Description	Bit Status	Default Status	Туре
Bit7	DC1 (Dummy cycle 1)		0	Volatile
Bit 6	DC0 (Dummy cycle 0)		0	Volatile
Bit 5	4 BYTE (4Byte address enable)	0=3-byte address mode 1=4-byte address mode	0	Volatile
Bit 4	x		х	Volatile
Bit 3	TB (top/bottom selected)	0 = Top 1=Bottom	0	OTP
Bit 2	ODS 2 (output driver strength)		1	Volatile
Bit 1	ODS 1 (output driver strength)		1	Volatile
Bit 0	ODS 0 (output driver strength)		1	Volatile



Enter 4Byte Mode Method

Using Enter 4-byte Mode (B7h) command to enable 4-byte address mode, the bit 5 (4BYTE) of Configuration should become to "1" after enter 4-byte mode. No WREN command is required.

Exit 4Byte Mode

- 1. Issue Exit 4Byte Mode (E9h) command to exit the 4Byte address Mode.
- 2. H/W Reset or S/W Reset Command.
- 3. Power-on cycle.

3-2. Extended Address Register (EAR)

The Extended Address Register provides the 4th byte of address, which configures the memory device for two 128Mb segments. Selected which one is active through the bit 0 of the Extended Address Register (EAR). It identifies the extended address (A31~A24) above 128Mb density and only requires using 3-byte addresses.

	Spar	Macronix	
Related Register	Bank Address Register (BAR)	Bank Address Register (BAR)	Extended Address Register (EAR)
Related Bit	Bit [0]	Bit [0:1]	Bit [0]
Write Command	BRWR(17h)	BRAC(B9h)+ WRR(01h)	WREAR(C5h)
Read Command	BRRD(16h)	BRRD(16h)	RDEAR(C8h)
WREN	Not required	Not required	Required

3-2-1 S25FL256S

Table 3-5. Related Register: Bank Register

Bits	Description	Bit Status	Default Status	Туре
7	EXTADD (Extended Address Enable)	1= 4 byte address 0=3byte address+ Bank address	0	Volatile
6 to 1	RFU		000000	Volatile
0	A24 (Bank address)	A24 for 256Mb	0	Volatile

- 1. Using "Bank Register Write (17h)" command to update the Bit 0 (A24) value of Bank Register to set Bank address A24 for 256Mb device.
- 2. By using legacy command B9h (BRAC) and following 01h (WRR) command to update the Bit 0 and Bit 1 value of Bank Register. This command cycle will only change the value of the BAR[1:0], not affect on the value of the EXTADD bit (BAR[7]). No WREN command is requested between BRAC and WRR command.
- 3. No WREN command is required between BRAC and WRR command. No affect on the value of the EXTADD bit (BAR[7]).



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Table 3-6. Related Register: Extended Address Register

Bits	Description	Default Status	Туре
Bit7	A31(Bank address)	0	volatile
Bit 6	A30(Bank address)	0	volatile
Bit 5	A29(Bank address)	0	volatile
Bit 4	A28(Bank address)	0	volatile
Bit 3	A27(Bank address)	0	volatile
Bit 2	A26(Bank address)	0	volatile
Bit 1	A25(Bank address)	0	volatile
Bit 0	A24(Bank address)	0	volatile

Issue WREAR (C5h) to update the value of EAR[7:0]. For the 256Mb, the A32 to A25 are "Don't Care" and reading these bits will result as 0. The data can be continually read out without 128Mb boundary, however, the EAR (Extended Address Register) value does not change.

3-3. 4Byte Command Set

New command sets for 4 byte address. The operation of 4-byte address command sets were very similar to original 3-byte address command sets. The only difference is that all the 4-byte command set require 4-byte addresses (A31-A0) followed by the instruction code.

	Instruction	Description	Macronix MX25L25635F	Spansion S25FL256S
	READ4B	Read Data Bytes	13h	13h
	Fast_READ4B	Read Data Bytes at Higher Speed	0Ch	0Ch
	DREAD4B	Dual Output Fast Read	3Ch	3Ch
	2READ4B	Dual Input/Output Fast Read	BCh	BCh
	QREAD4B	Quad Output Fast Read	6Ch	6Ch
	4READ4B	Quad Input/Output Fast Read	ECh	ECh
4Byte	4DDRFR	DDR fast Read	-	0Eh
Command 4	4DDRDIOR	DDR dual Input/Output Read	-	BEh
	4DDRQIOR	DDR Quad Input/Output Read	-	EEh
	PP4B	Page Program	12h	12h
	4PP4B	Quad page program 1-4-4	3Eh	-
	QPP4B	Quad page program 1-1-4	-	34h
	SE4B	Sector Erase	21h	21h
	BE4B	Block Erase 64KB	DCh	DCh
	BE32K4B	Block erase 32KB	5Ch	-





4. Performance Comparison

Table below is the performance comparison of the two products.

Parameter\Company		MX25L25635F	S25FL256S	
Туре		SDR	SDR	DDR
VCC		2.7-3.6V	2.7-3.6V	3.0-3.6V
Normal R	lead	50MHz	50MHz	
	1 I/O	133MHz	133MHz	66MHz
Faat	1-in/2-out	133MHz	104MHz	
Pood	2-in/2-out	133MHz	104MHz	66MHz
Reau	1-in/4-out	133MHz	104MHz	
	4-in/4-out	133MHz	104MHz	66MHz
	15pf	6ns	6.5ns(3.0-3.6V)	6.5ns(3.0-3.6V)
	30pf	8ns	8ns	_

Table 4-1. Read Performance Comparison

The MX25L25635F provides industry fast SDR read performance as 133MHz frequency with all kinds of protocols. It features same throughput as 66MHz DTR , with wider data valid window and more reliable data catch ability.

Table 4-2. Write Performance and Power Consumption Comparison

Parameter\Company		Macronix	Spansion
Part no.		MX25L25635F	S25FL256S
	4KB (typ)	0.03s	0.13s
Eraca	32KB (typ)	0.19s	-
Erase	64KB (typ)	0.34s	2.08s
	Top/Bottom 64KB	0.34s	2.08s
Drogrom	256B (typ)	0.6ms	0.25ms
Frogram	512B(typ)	-	0.34ms
Active Write Current (max)		20mA	100mA
Active Read Current (max)		25mA	50mA
Standby Cur	rent (typ/max)	30uA/100uA	70uA /100uA

The MX25L25635F provides lower power consumption on Read and Write operation, which perform better efficiency for the operating of host system.



5. Command Code Comparison

Instruction Type	Instruction	Description	Macronix MX25L25635F	Spansion S25FL256S
Read ID	RDID	Read Identification	9Fh	9Fh
	RES	Read electronic ID	ABh	ABh
	REMS	Read electronic manufacturer & device ID	90h	90h
	REMS 2		EFh	-
	REMS 4		DFh	-
	READ	Read Data Bytes	03h	03h
	FAST_READ	Read Data Bytes at Higher Speed	0Bh	0Bh
	DOFR	Dual Output Fast Read	3Bh	3Bh
	DIOFR	Dual Input/Output Fast Read	BBh	BBh
	QOFR	Quad Output Fast Read	6Bh	6Bh
Read	QIOFR	Quad Input/Output Fast Read EBh		EBh
	DDRFR	DDR fast Read	-	0Dh
	DDRDIOR	DDR dual Input/Output Read	-	BDh
	DDRQIOR	DDR Quad Input/Output Read	-	EDh
	RDSFDP	Read Serial Flash Discovery Parameter	5Ah	-
	WREN	Write Enable	06h	06h
	WRDI	Write Disable	04h	04h
	PP	Page Program	02h	02h
Write	4PP	Quad page program	38h	32h/38h
VVIILE	SE	Sector Erase	20h	20h
	SE 64K	Block Erase 64KB	D8h	D8h
	BE 32K	Block erase 32KB	52h	-
	CE	Chip Erase	60 or C7h	60 or C7h
	EQIO	Enable QPI	35h	-
ΟΤΡ	RSTQIO	Reset QPI	F5h	-
	QPIID	QPI ID Read	Afh	-
	ENSO	Enter secured OTP	B1h	-
	EXSO	Exit secured OTP	C1h	-
	ROTP	Read OTP (Read of OTP area)	-	4Bh
	POTP	area)	-	42h



Command Code Comparison - Continued

Instruction Type	Instruction	Description	Macronix MX25L25635F	Spansion S25FL256S
	RDSR	Read Status Register 1	05h	05h
	RDCR 2	Read Status Register 2	15h	35h
	WRSR	Write Status Register	01h	01h
	RDSCUR	Read security register	2Bh	-
	WRSCUR	Write security register	2Fh	-
	RDLR	Read Lock Register	2Dh	2Bh
	WRLR	Write to Lock Register	2Ch	2Fh
	RDSPBLK	SPB Lock Bit Read	A7h	A7h
	SPBLK	SPB Lock Bit Write	A6h	A6h
Deviater	RDSPB	SPB Bit Read	E2h	E2h
Register	WRSPB	SPB Bit Write	E3h	E3h
	ESSPB	SPB Bit Erase	E4h	E4h
	RDPASS	Password Read	27h	E7h
	WRPASS	Password Write	28h	E8h
	PASSULK	Password Unlock	29h	E9h
	RDDPB	DPB Read	E0h	E0h
	WRDPB	DPB Write	E1h	E1h
	RDFBR	Fast Boot Register Read	16h	14h
	WRFBR	Fast Boot Register Write	17h	15h
	ESFBR	Fast Boot Register Erase	18h	-
Others	PER /PGRS	Program Resume	30h	8Ah
	PES /PGSP	Program Suspend	B0h	85h
	ERRS	Erase Resume	30h	7Ah
	ERSP	Erase Suspend	B0h	75h
	RSTEN	Reset Enable	66h	-
	RST	Reset Memory	99h	F0h
		Reset from enhance mode	FFh	FFh
	DP	Deep Power-down	B9h	B9h
	RDP	Release from Deep Power-down	ABh	ABh
	NOP	No Operation	00h	-
	SBL	Set Burst Length	C0h	77h



6. References

The following datasheets were used for preparing this comparison note:

Datasheet	Location	Date Issued	Versions
MX25L25635F	Macronix Website	SEP. 2011	1.2
S25FL256S	Spansion Website	NOV. 2011	02

For more functional and parametric specifications, please refer to the datasheet on the Macronix Website at <u>http://www.macronix.com/</u> and go to: Products/Flash Memory/Serial Flash.



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