National Semiconductor

November 1995

CD4046BM/CD4046BC Micropower Phase-Locked Loop

CD4046BM/CD4046BC Micropower Phase-Locked Loop

General Description

The CD4046B micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

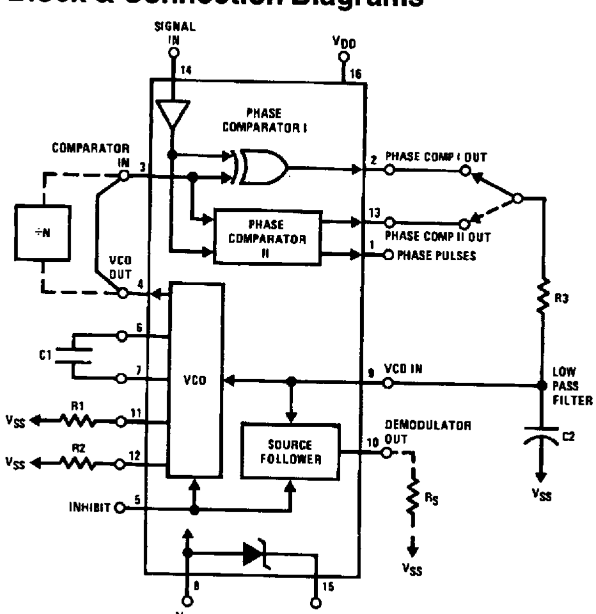
Features

- Wide supply voltage range — 3.0V to 18V
- Low dynamic power consumption — 70 μW (typ.) at f_o = 10 kHz, V_{DD} = 5V
- VCO frequency — 1.3 MHz (typ.) at V_{DD} = 10V
- Low frequency drift with temperature — 0.06%/°C at V_{DD} = 10V
- High VCO linearity — 1% (typ.)

Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

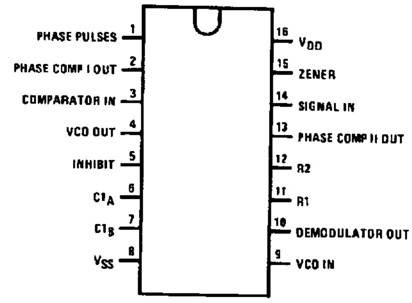
Block & Connection Diagrams



TL/F/5968-1

FIGURE 1

Dual-In-Line Package



TL/F/5968-2

Top View

Order Number CD4046B

RRD-B30M115/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

DC Supply Voltage (V_{DD})	3 to 15 V_{DC}
Input Voltage (V_{IN})	0 to V_{DD} V_{DC}
Operating Temperature Range (T_A)	
CD4046BM	−55°C to +125°C
CD4046BC	−40°C to +85°C

DC Electrical Characteristics CD4046BM (Note 2)

Symbol	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	Pin 5 = V_{DD}, Pin 14 = V_{DD}, Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		5		0.005	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.015	20		600	μA
		Pin 5 = V_{DD}, Pin 14 = Open, Pin 3, 2 = V_{SS}								
		V_{DD} = 5V		45		5	35		185	μA
		V_{DD} = 10V		450		20	350		650	μA
		V_{DD} = 15V		1200		50	900		1500	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 14V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
C_{IN}	Input Capacitance	Any Input (Note 3)							7.5	pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ, R2 = ∞, VCO_{IN} = $V_{DD}/2$								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

DC Electrical Characteristics CD4046BC (Note 2)

Symbol	Parameter	Conditions	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Units
I_{DD}	Quiescent Device Current	Pin 5 = V_{DD}, Pin 14 = V_{DD}, Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		20		0.005	20		150	µA
		V_{DD} = 10V		40		0.01	40		300	µA
		V_{DD} = 15V		80		0.015	80		600	µA
		Pin 5 = V_{DD}, Pin 14 = Open, Pin 3, 9 = V_{SS}								
		V_{DD} = 5V		70		5	55		205	µA
		V_{DD} = 10V		530		20	410		710	µA
		V_{DD} = 15V		1500		50	1200		1800	µA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	µA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	µA
C_{IN}	Input Capacitance	Any Input (Note 3)					7.5			pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ, R2 = ∞, VCO_{IN} = $V_{DD}/2$								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics* CD4046BM/CD4046BC $T_A = 25°C$, $C_L = 50$ pF

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VCO SECTION						
I_{DD}	Operating Current	f_o = 10 kHz, R1 = 1 MΩ, R2 = ∞, $VCO_{IN} = V_{DD}/2$				
		V_{DD} = 5V		20		μA
		V_{DD} = 10V		90		μA
		V_{DD} = 15V		200		μA
f_{MAX}	Maximum Operating Frequency	C1 = 50 pF, R1 = 10 kΩ, R2 = ∞, $VCO_{IN} = V_{DD}$				
		V_{DD} = 5V	0.4	0.8		MHz
		V_{DD} = 10V	0.6	1.2		MHz
		V_{DD} = 15V	1.0	1.6		MHz
	Linearity	VCO_{IN} = 2.5V ±0.3V, R1 ≥ 10 kΩ, V_{DD} = 5V		1		%
		VCO_{IN} = 5V ±2.5V, R1 ≥ 400 kΩ, V_{DD} = 10V		1		%
		VCO_{IN} = 7.5V ±5V, R1 ≥ 1 MΩ, V_{DD} = 15V		1		%
	Temperature-Frequency Stability No Frequency Offset, $f_{MIN} = 0$	%/°C ∝ 1/f. V_{DD} R2 = ∞				
		V_{DD} = 5V		0.12–0.24		%/°C
		V_{DD} = 10V		0.04–0.08		%/°C
		V_{DD} = 15V		0.015–0.03		%/°C
	Frequency Offset, $f_{MIN} \neq 0$	V_{DD} = 5V		0.06–0.12		%/°C
		V_{DD} = 10V		0.05–0.1		%/°C
		V_{DD} = 15V		0.03–0.06		%/°C
VCO_{IN}	Input Resistance	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
VCO	Output Duty Cycle	V_{DD} = 5V		50		%
		V_{DD} = 10V		50		%
		V_{DD} = 15V		50		%
t_{THL}	VCO Output Transition Time	V_{DD} = 5V		90	200	ns
t_{THL}		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		45	80	ns

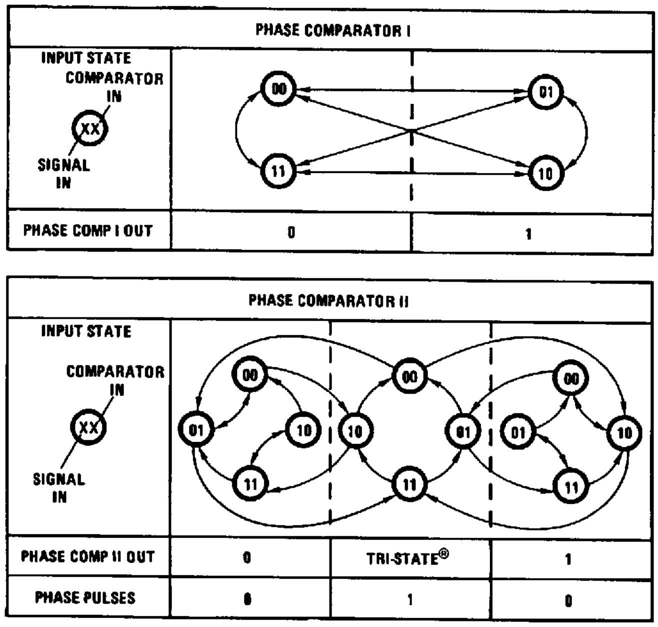
*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* CD4046BM/CD4046BC T_A = 25°C, C_L = 50 pF (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
PHASE COMPARATORS SECTION						
R_{IN}	Input Resistance					
	Signal Input	V_{DD} = 5V	1	3		MΩ
		V_{DD} = 10V	0.2	0.7		MΩ
		V_{DD} = 15V	0.1	0.3		MΩ
	Comparator Input	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
	AC-Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000 pF				
		f = 50 kHz				
		V_{DD} = 5V		200	400	mV
		V_{DD} = 10V		400	800	mV
		V_{DD} = 15V		700	1400	mV
DEMODULATOR OUTPUT						
VCO_{IN} – V_{DEM}	Offset Voltage	RS ≥ 10 kΩ, V_{DD} = 5V		1.50	2.2	V
		RS ≥ 10 kΩ, V_{DD} = 10V		1.50	2.2	V
		RS ≥ 50 kΩ, V_{DD} = 15V		1.50	2.2	V
	Linearity	RS ≥ 50 kΩ				
		VCO_{IN} = 2.5V ±0.3V, V_{DD} = 5V		0.1		%
		VCO_{IN} = 5V ±2.5V, V_{DD} = 10V		0.6		%
		VCO_{IN} = 7.5V ±5V, V_{DD} = 15V		0.8		%
ZENER DIODE						
V_Z	Zener Diode Voltage	I_Z = 50 μA	6.3	7.0	7.7	V
R_Z	Zener Dynamic Resistance	I_Z = 1 mA		100		Ω

*AC Parameters are guaranteed by DC correlated testing.

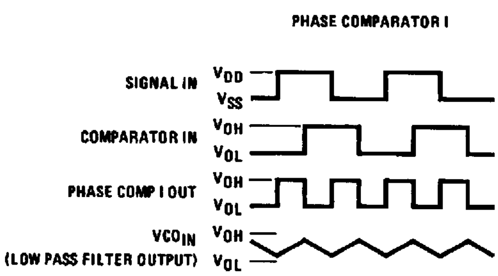
Phase Comparator State Diagrams



TL/F/5968-3

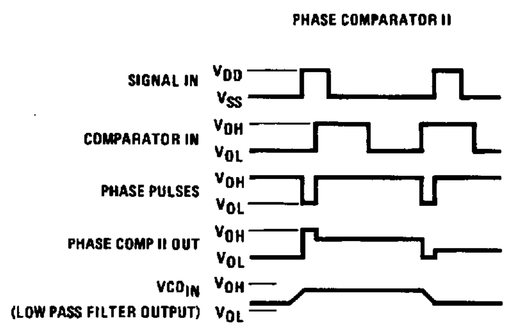
FIGURE 2

Typical Waveforms



TL/F/5968-4

FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition



TL/F/5968-5

FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Performance Characteristics

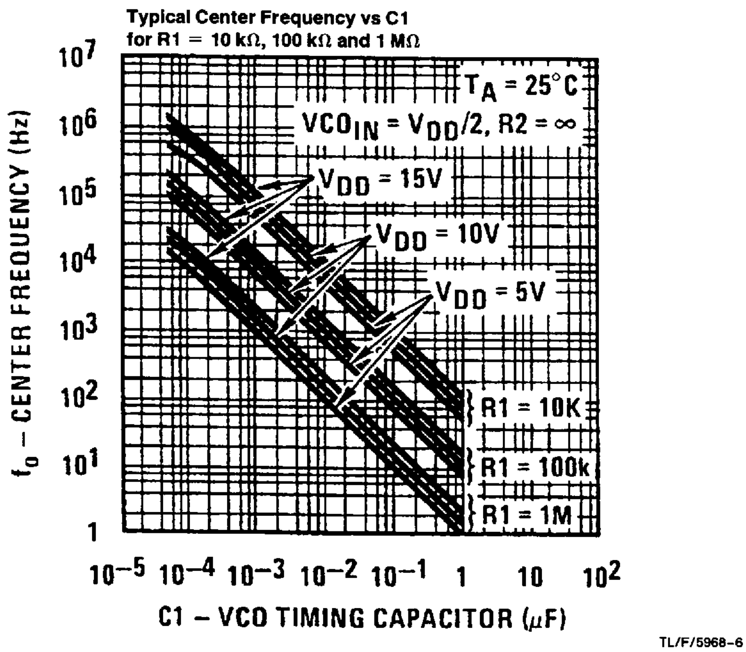


FIGURE 5a

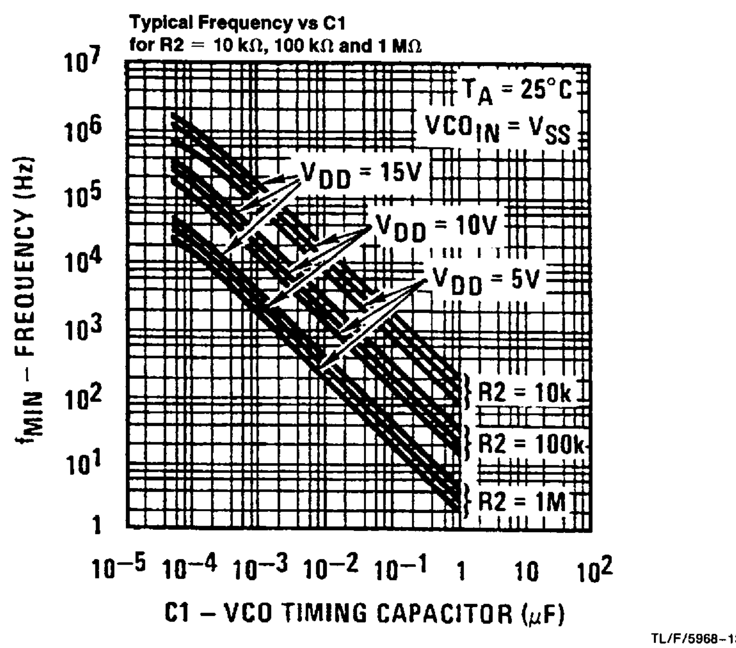
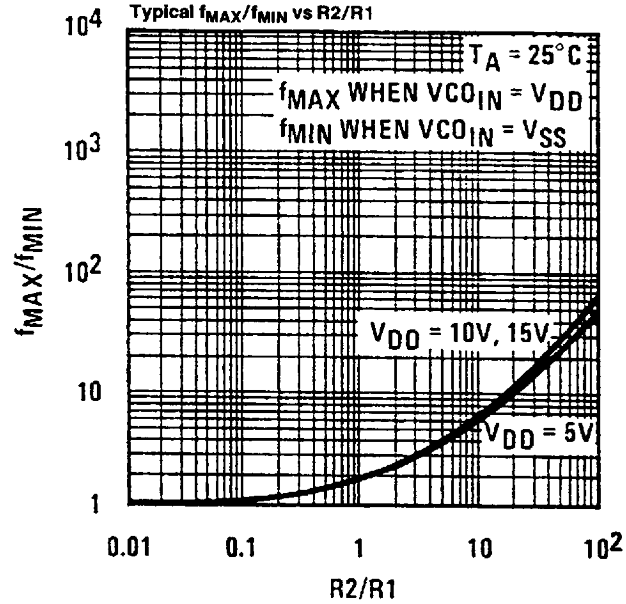


FIGURE 5b

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Typical Performance Characteristics (Continued)

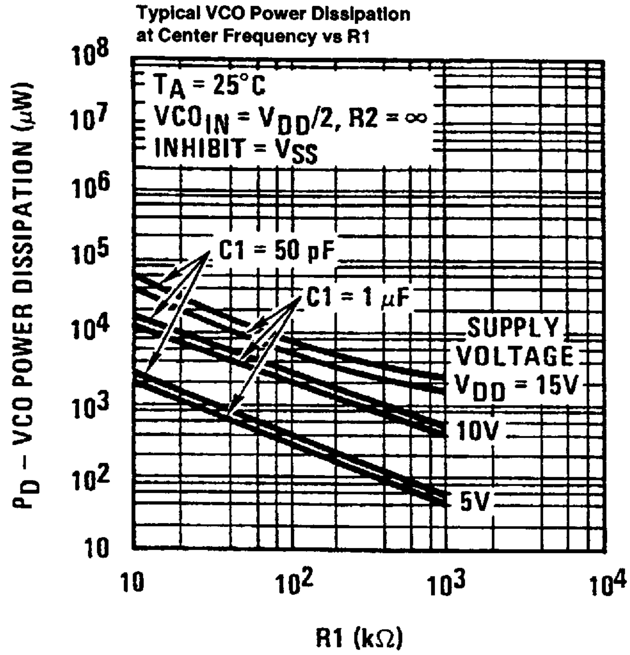
Typical f_{MAX}/f_{MIN} vs R2/R1



TL/F/5968–14

FIGURE 5C

Typical VCO Power Dissipation at Center Frequency vs R1

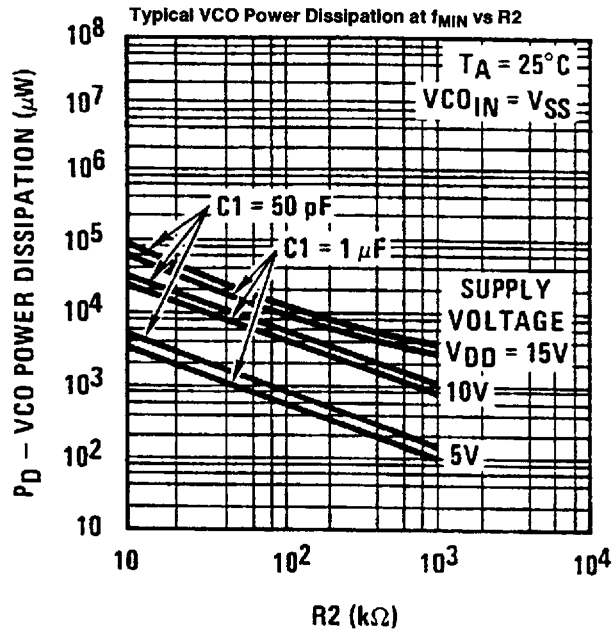


TL/F/5968–15

FIGURE 6a

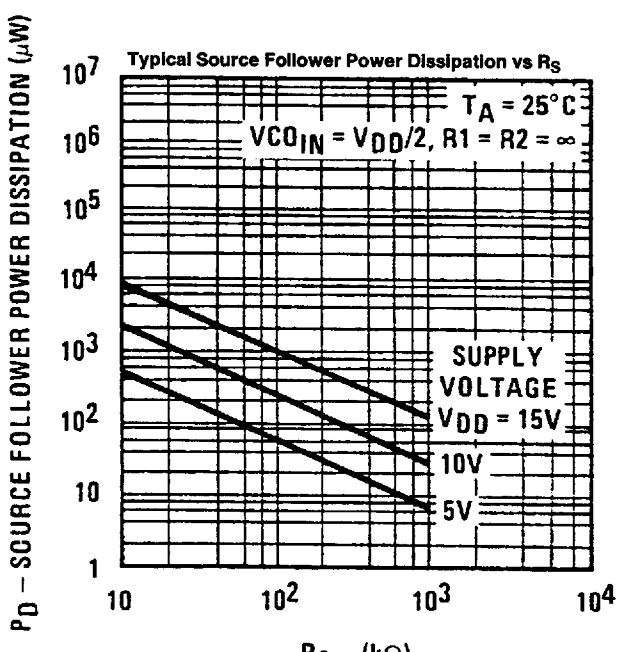
Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Typical Performance Characteristics (Continued)



TL/F/5968–16

FIGURE 6b

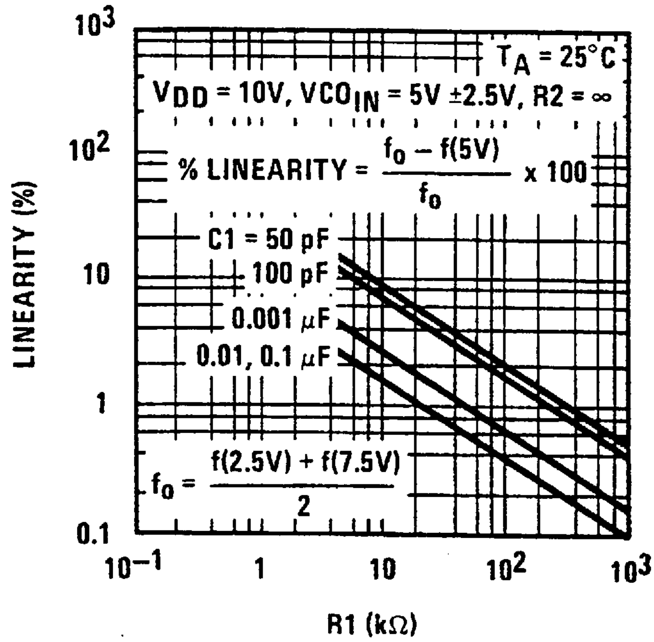


TL/F/5968–17

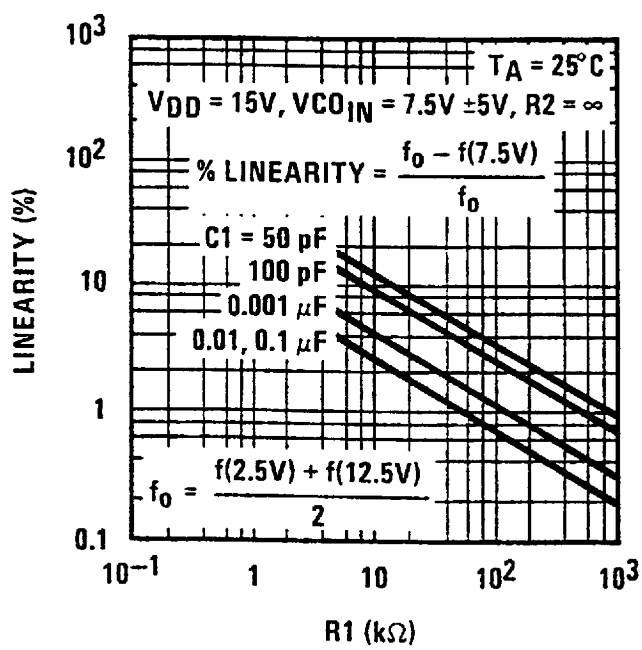
FIGURE 6c

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Typical Performance Characteristics (Continued)



TL/F/5968–18



TL/F/5968–19

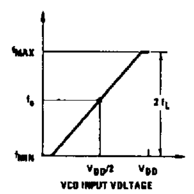
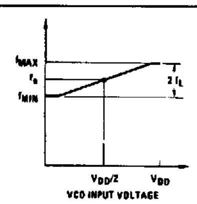
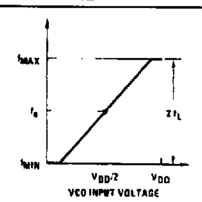
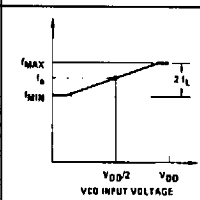
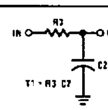
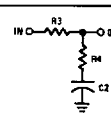
FIGURE 7. Typical VCO Linearity vs R1 and C1

Note: To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Design Information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges: R1, R2 ≥ 10 kΩ, R_S ≥ 10 kΩ, C1 ≥ 50 pF.

In addition to the given design information, refer to *Figure 5* for R1, R2 and C1 component selections.

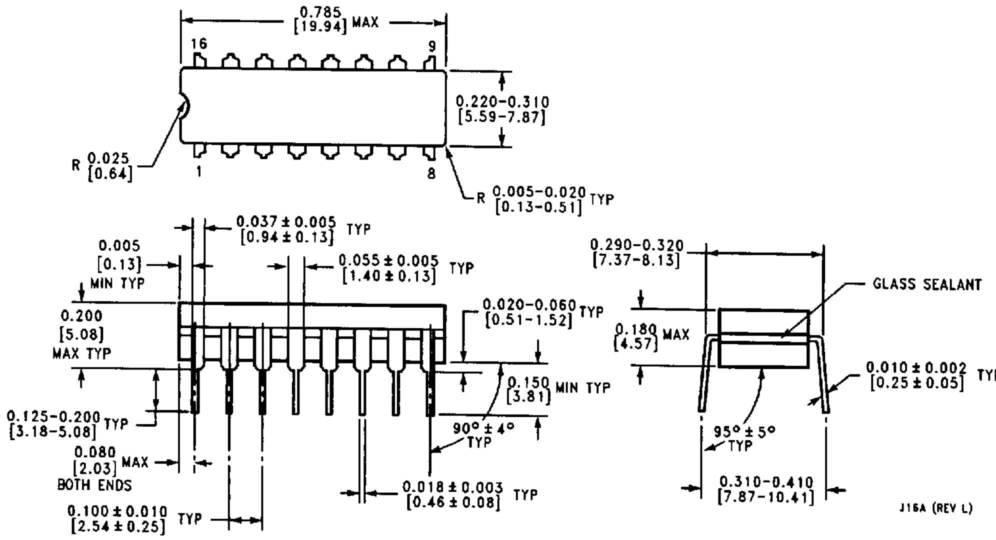
Characteristics	Using Phase Comparator I		Using Phase Comparator II	
	VCO Without Offset $R2 = \infty$	VCO With Offset	VCO Without Offset $R2 = \infty$	VCO With Offset
VCO Frequency	 TL/F/5968-7	 TL/F/5968-8	 TL/F/5968-9	 TL/F/5968-10
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2 f_L$	$2 f_L$ = full VCO frequency range $2 f_L = f_{max} - f_{min}$			
Frequency Capture Range, $2 f_C$	 TL/F/5968-11	$2 f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$	$f_C = f_L$	
Loop Filter Component Selection	 TL/F/5968-12	For $2 f_C$, see Ref.		
Phase Angle Between Single and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range ($2 f_L$)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	Given: f_o. Use f_o with *Figure 5a* to determine R1 and C1.	Given: f_o and f_L. Calculate f_{min} from the equation $f_{min} = f_o - f_L$. Use f_{min} with *Figure 5b* to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$. Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1.	Given: f_{max}. Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$. Use f_o with *Figure 5a* to determine R1 and C1.	Given: f_{min} and f_{max}. Use f_{min} with *Figure 5b* to determine R2 and C1. Calculate $\frac{f_{max}}{f_{min}}$. Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1.

References

G.S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

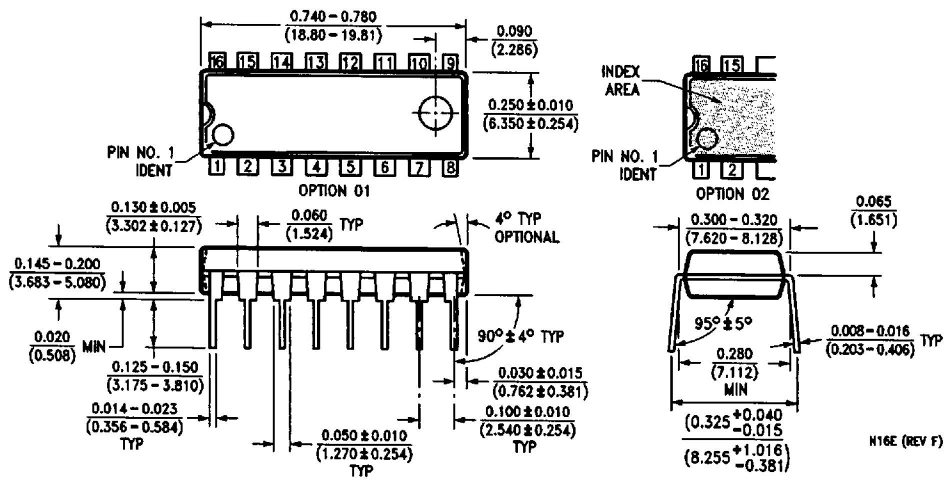
Floyd Gardner, "Phaselock Techniques", John Wiley & Sons, 1966.

Physical Dimensions inches (millimeters)



Order Number CD4046BMJ or CD4046BCJ
NS Package Number J16A

Physical Dimensions inches (millimeters) (Continued)



Order Number CD4046BMN or CD4046BCN
NS Package Number N16E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408