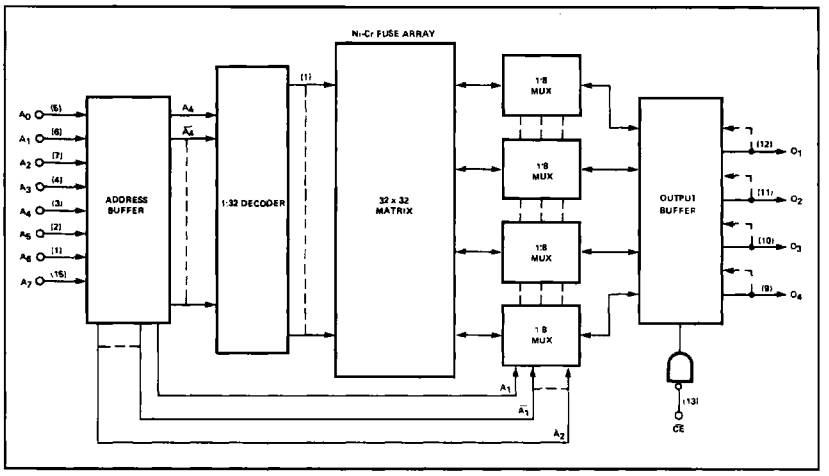
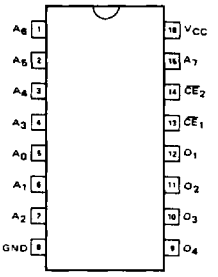
N82S126/129-B,F. • S82S126/129F

BLOCK DIAGRAM

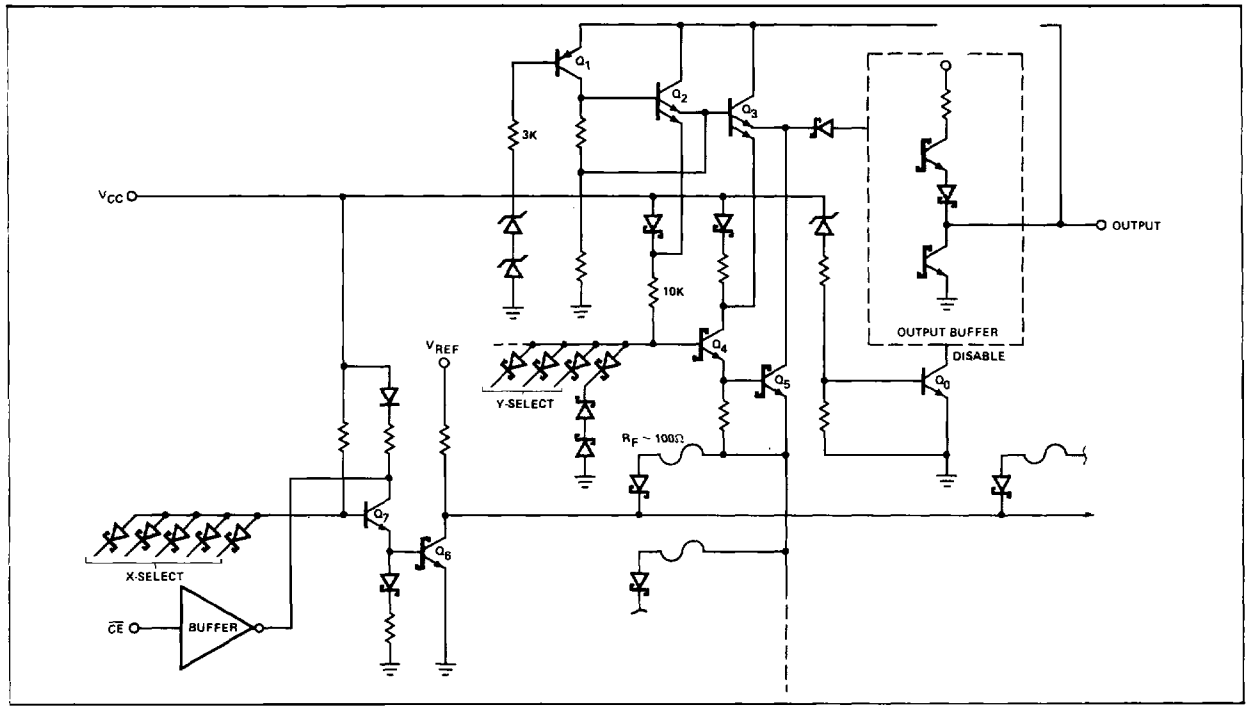


PIN CONFIGURATION

B,F PACKAGE



TYPICAL FUSING PATH



AC ELECTRICAL CHARACTERISTICS

S82S126/129 $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$
N82S126/129 $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

PARAMETER		TEST CONDITIONS	S82S126/129			N82S126/129			UNIT
			MIN	TYP2	MAX	MIN	TYP2	MAX	
Propagation Delay									
T_{AA}	Address to Output	C_L = 30pF		35	70		35	50	ns
T_{CD}	Chip Disable to Output	R_1 = 270Ω		15	35		15	20	ns
T_{CE}	Chip Enable to Output	R_2 = 600Ω		15	35		15	20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. Typical values are at V_{CC} = 5.0V, T_A = +25°C.

PROGRAMMING SPECIFICATIONS (Testing of these limits may cause programming of device.) T_A = +25°C

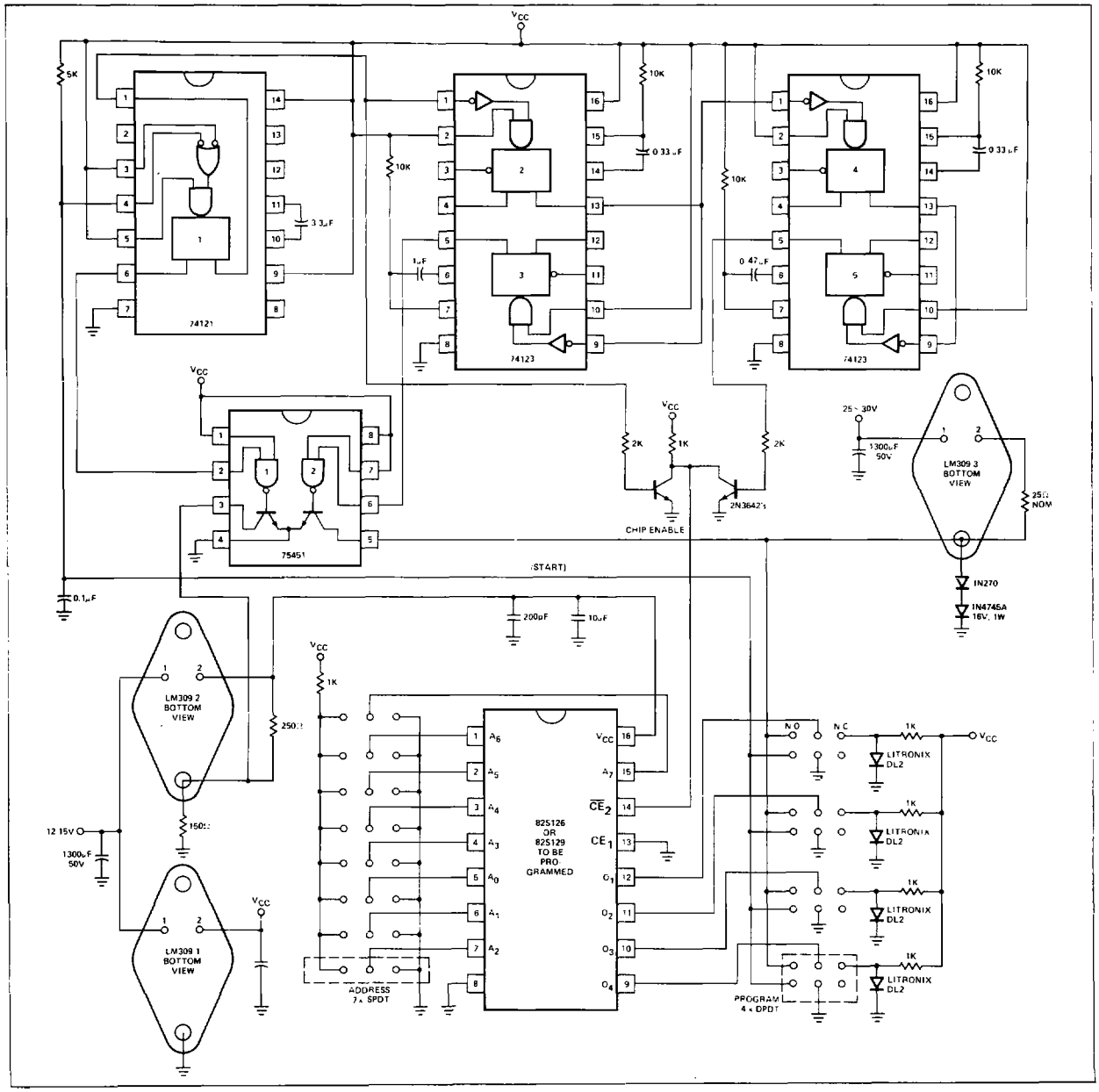
PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
Power Supply Voltage						
V_{CCP}[1]	To Program	I_{CCP} = 350 ± 50mA (Transient or steady state)	8.5	8.75	9.0	V
V_{CCH}	Upper Verify Limit		5.3	5.5	5.7	V
V_{CCL}	Lower Verify Limit		4.3	4.5	4.7	V
V_S[3]	Verify Threshold		0.9	1.0	1.1	V
I_{CCP}	Programming Supply Current	V_{CCP} = +8.75 ± .25V	300	350	400	mA
Input Voltage						
V_{IH}	Logical "1"		2.4		5.5	V
V_{IL}	Logical "0"		0	0.4	0.8	V
Input Current						
I_{IH}	Logical "1"	V_{IH} = +5.5V			50	μA
I_{IL}	Logical "0"	V_{IL} = +0.4V			-500	μA
V_{OUT}[2]	Output Programming Voltage	I_{OUT} = 200 ± 20mA (Transient or steady state)	16.0	17.0	18.0	V
I_{OUT}	Output Programming Current	V_{OUT} = +17 ± 1V	180	200	220	mA
T_R	Output Pulse Rise Time		10		50	μs
t_p	$\overline{CE}$ Programming Pulse Width		1		2	ms
t_D	Pulse Sequence Delay		10			μs
T_{PR}	Programming Time	V_{CC} = V_{CCP}			2.5	sec
T_{PS}	Programming Pause	V_{CC} = OV	5			sec
$\frac{T_{PR}}{T_{PR} + T_{PS}}$[4]	Programming Duty Cycle				33	%

PROGRAMMING PROCEDURE

1. Terminate all device outputs with a 10KΩ resistor to V_{CC}.
2. Select the Address to be programmed, and raise V_{CC} to V_{CCP} = 8.75 ± .25V.
3. After 10μs delay, apply V_{OUT} = +17 ± 1V to the output to be programmed. Program one output at the time.
4. After 10μs delay, pulse both $\overline{CE}$ inputs to logic "0" for 1 to 2 ms.
5. After 10μs delay, remove +17V from the programmed output.
6. To verify programming, after 10μs delay, lower V_{CC} to V_{CCH} = +5.5 ± .2V, and apply a logic "0" level to both $\overline{CE}$ inputs. The programmed output should remain in the "1" state. Again, lower V_{CC} to V_{CCL} = +4.5 ± .2V, and verify that the programmed output remains in the "1" state.
7. Raise V_{CC} to V_{CCP} = 8.75 ± .25V, and repeat steps 3 through 6 to program other bits at the same address.
8. After 10μs delay, repeat steps 2 through 7 to program all other address locations.

NOTES:
1. Bypass V_{CC} to GND with a 0.01μF capacitor to reduce voltage spikes.
2. Care should be taken to insure the 17 ± 1V output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit
3. V_S is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program Verify cycle with a Rest period (VCC = 0V) of 4ms

MANUAL PROGRAMMER



TIMING SEQUENCE