## DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS

The LSTTL/MSI SN54/74LS253 is a Dual 4-Input Multiplexer with 3-state outputs. It can select two bits of data from four sources using common select inputs. The outputs may be individually switched to a high impedance state with a HIGH on the respective Output Enable ( $\mathrm{E}_{0}$ ) inputs, allowing the outputs to interface directly with bus oriented systems. It is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Non-Inverting 3-State Outputs
- Input Clamp Diodes Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)


| PIN NAMES |  | LOADING (Note a) |  |
| :---: | :---: | :---: | :---: |
|  |  | HIGH | LOW |
| $S_{0}, S_{1}$ | Common Select Inputs | 0.5 U.L. | 0.25 U.L. |
| Multiplexer A |  |  |  |
| $\mathrm{E}_{0} \mathrm{a}$ | Output Enable (Active LOW) Input | 0.5 U.L. | 0.25 U.L. |
| ${ }^{1} a^{-1}{ }_{3 a}$ | Multiplexer Inputs | 0.5 U.L. | 0.25 U.L. |
| $\mathrm{Z}_{\mathrm{a}}$ | Multiplexer Output (Note b) | 65 (25) U.L. | 15 (7.5) U.L. |
| Multiplexer B |  |  |  |
| $\mathrm{E}_{0}$ | Output Enable (Active LOW) Input | 0.5 U.L. | 0.25 U.L. |
| $\mathrm{I}_{0} \mathrm{l}^{-1} 3 \mathrm{~b}$ | Multiplexer Inputs | 0.5 U.L. | 0.25 U.L. |
| $\mathrm{Z}_{\mathrm{b}}$ | Multiplexer Output (Note b) | 65 (25) U.L. | 15 (7.5) U.L. |

NOTES:
a) 1 TTL Unit Load (U.L.) $=40 \mu \mathrm{~A}$ HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

DUAL 4-INPUT MULTIPLEXER WITH 3-STATE OUTPUTS LOW POWER SCHOTTKY


## SN54/74LS253

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The LS253 contains two identical 4-Input Multiplexers with 3 -state outputs. They select two bits from four sources selected by common select inputs ( $\mathrm{S}_{0}, \mathrm{~S}_{1}$ ). The 4-input multiplexers have individual Output Enable ( $\mathrm{E}_{0 \mathrm{a}}, \mathrm{E}_{0 \mathrm{~b}}$ ) inputs which when HIGH, forces the outputs to a high impedance (high Z) state.
The LS253 is the logic implementation of a 2-pole, 4 -position switch, where the position of the switch is determined by the logic levels supplied to the two select inputs. The logic equations for the outputs are shown below:
$Z_{a}=\bar{E}_{0 a} \cdot\left(I_{0 a} \cdot \bar{S}_{1} \cdot \bar{S}_{0}+I_{1 a} \cdot \bar{S}_{1} \cdot S_{0} \cdot I_{2 a} \cdot S_{1} \cdot \bar{S}_{0}+I_{3 a} \cdot S_{1}\right.$ - $\mathrm{S}_{0}$ )
$Z_{b}=\bar{E}_{0 b} \cdot\left(I_{0 b} \cdot \bar{S}_{1} \cdot \bar{S}_{0}+I_{1 b} \cdot \bar{S}_{1} \cdot S_{0} \cdot I_{2 b} \cdot S_{1} \cdot \bar{S}_{0}+I_{3 b} \cdot S_{1}\right.$ So)

If the outputs of 3-state devices are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maximum ratings. Designers should ensure that Output Enable signals to 3-state devices whose outputs are tied together are designed so that there is no overlap.

TRUTH TABLE

| SELECT <br> INPUTS |  |  | DATA INPUTS |  | OUTPUT <br> ENABLE | OUTPUT |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{S}_{\mathbf{0}}$ | $\mathrm{S}_{\mathbf{1}}$ | $\mathrm{I}_{\mathbf{0}}$ | $\mathrm{I}_{\mathbf{1}}$ | $\mathrm{I}_{\mathbf{2}}$ | $\mathrm{I}_{\mathbf{3}}$ | $\mathrm{E}_{\mathbf{0}}$ | Z |
| X | X | X | X | X | X | H | $\mathrm{Z})$ |
| L | L | L | X | X | X | L | L |
| L | L | H | X | X | X | L | H |
| H | L | X | L | X | X | L | L |
| H | L | X | H | X | X | L | H |
| L | H | X | X | L | X | L | L |
| L | H | X | X | H | X | L | H |
| H | H | X | X | X | L | L | L |
| H | H | X | X | X | H | L | H |

[^0]GUARANTEED OPERATING RANGES

| Symbol | Parameter |  | Min | Typ | Max | Unit |
| :--- | :--- | :---: | :---: | :---: | :---: | :---: |
| $V_{\text {CC }}$ | Supply Voltage | 54 | 4.5 | 5.0 | 5.5 | $\mathrm{~V}^{\prime}$ |
|  |  | 74 | 4.75 | 5.0 | 5.25 |  |
| $\mathrm{~T}_{\mathrm{A}}$ | Operating Ambient Temperature Range | 54 | -55 | 25 | 125 | ${ }^{\circ} \mathrm{C}$ |
|  |  | 74 | 0 | 25 | 70 |  |
| IOH | Output Current — High | 54 |  |  | -1.0 | mA |
|  |  | 74 |  |  | -2.6 |  |
| IOL | Output Current - Low | 54 |  |  | 12 | mA |
|  |  | 74 |  |  | 24 |  |

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

| Symbol | Parameter |  | Limits |  |  | Unit | Test Conditions |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |  |
| $\mathrm{V}_{\mathrm{IH}}$ | Input HIGH Voltage |  | 2.0 |  |  | V | Guaranteed I All Inputs | HIGH Voltage for |
| VIL | Input LOW Voltage | 54 |  |  | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs |  |
|  |  | 74 |  |  | 0.8 |  |  |  |
| $\mathrm{V}_{\mathrm{IK}}$ | Input Clamp Diode Voltage |  |  | -0.65 | -1.5 | V | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}$, | 18 mA |
| $\mathrm{V}_{\mathrm{OH}}$ | Output HIGH Voltage | 54 | 2.4 | 3.4 |  | V | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MIN}, \mathrm{IOH}_{\mathrm{O}}=\mathrm{MAX}, \mathrm{~V}_{\mathrm{IN}}=\mathrm{V}_{\mathrm{IH}}$or VIL per Truth Table |  |
|  |  | 74 | 2.4 | 3.1 |  | V |  |  |
| VOL | Output LOW Voltage | 54, 74 |  | 0.25 | 0.4 | V | $\mathrm{IOL}=12 \mathrm{~mA}$ | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=\mathrm{V}_{\mathrm{CC}} \mathrm{MIN}, \\ & \mathrm{~V}_{\text {IN }}=\mathrm{V}_{\text {IL }} \text { or } \mathrm{V}_{\text {IH }} \\ & \text { per Truth Table } \end{aligned}$ |
|  |  | 74 |  | 0.35 | 0.5 | V | $\mathrm{IOL}=24 \mathrm{~mA}$ |  |
| IOZH | Output Off Current HIGH |  |  |  | 20 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {CC }}=\mathrm{MAX}, \mathrm{V}_{\text {OUT }}=2.7 \mathrm{~V}$ |  |
| IOZL | Output Off Current LOW |  |  |  | -20 | $\mu \mathrm{A}$ | $\mathrm{V}_{\text {CC }}=\mathrm{MAX}, \mathrm{V}_{\text {OUT }}=0.4 \mathrm{~V}$ |  |
| IIH | Input HIGH Current |  |  |  | 20 | $\mu \mathrm{A}$ | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}, \mathrm{V}_{\text {IN }}=2.7 \mathrm{~V}$ |  |
|  |  |  |  |  | 0.1 | mA | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}, \mathrm{V}_{\mathrm{IN}}=7.0 \mathrm{~V}$ |  |
| IIL | Input LOW Current |  |  |  | -0.4 | mA | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}, \mathrm{V}_{\text {IN }}=0.4 \mathrm{~V}$ |  |
| los | Short Circuit Current (Note 1) |  | -30 |  | -130 | mA | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}$ |  |
| ICC | Power Supply Current |  |  |  | 12 | mA | $\mathrm{V}_{C C}=\mathrm{MAX}, \mathrm{V}_{\mathrm{E}}=0 \mathrm{~V}$ |  |
|  |  |  |  |  | 14 | mA | $\mathrm{V}_{\mathrm{CC}}=\mathrm{MAX}, \mathrm{V}_{\mathrm{E}}=4.5 \mathrm{~V}$ |  |

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.
AC CHARACTERISTICS $\left(T_{A}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=5.0 \mathrm{~V}\right)$ See SN54LS251 for Waveforms

| Symbol | Parameter | Limits |  |  | Unit | Test Conditions |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |  |
| $\begin{aligned} & \text { tpLH } \\ & \text { tphen } \end{aligned}$ | Propagation Delay, Data to Output |  | $\begin{aligned} & 17 \\ & 13 \end{aligned}$ | $\begin{aligned} & 25 \\ & 20 \end{aligned}$ | ns | Figure 1 | $\begin{aligned} & C_{\mathrm{L}}=45 \mathrm{pF}, \\ & \mathrm{R}_{\mathrm{L}}=667 \Omega \end{aligned}$ |
| $\begin{aligned} & \text { tpLH } \\ & \text { tPHL } \end{aligned}$ | Propagation Delay, Select to Output |  | $\begin{aligned} & 30 \\ & 21 \end{aligned}$ | $\begin{aligned} & 45 \\ & 32 \end{aligned}$ | ns | Figure 1 |  |
| $\begin{aligned} & \text { tpZH } \\ & \text { tp7l } \end{aligned}$ | Output Enable Time |  | $\begin{aligned} & 15 \\ & 15 \end{aligned}$ | $\begin{aligned} & 28 \\ & 23 \end{aligned}$ | ns | Figures 4, 5 |  |
| $\begin{aligned} & \text { tPHZ } \\ & \text { tpLZ } \\ & \hline \end{aligned}$ | Output Disable Time |  | $\begin{aligned} & 27 \\ & 18 \end{aligned}$ | $\begin{aligned} & 41 \\ & 27 \end{aligned}$ | ns | Figures 3, 5 | $\begin{aligned} & \mathrm{C}_{\mathrm{L}}=5.0 \mathrm{pF}, \\ & \mathrm{R}_{\mathrm{L}}=667 \Omega \end{aligned}$ |


[^0]:    $\mathrm{H}=\mathrm{HIGH}$ Level
    L = LOW Level
    X = Irrelevant
    (Z) = High Impedance (off)

    Address inputs $\mathrm{S}_{0}$ and $\mathrm{S}_{1}$ are common to both sections.

