

# MC10EL52, MC100EL52

## 5V ECL Differential Data and Clock D Flip-Flop

The MC10EL/100EL52 is a differential data, differential clock D flip-flop with reset. The device is functionally equivalent to the E452 device with higher performance capabilities. With propagation delays and output transition times significantly faster than the E452, the EL52 is ideally suited for those applications which require the ultimate in AC performance.

Data enters the master portion of the flip-flop when the clock is LOW and is transferred to the slave, and thus the outputs, upon a positive transition of the clock. The differential clock inputs of the EL52 allow the device to also be used as a negative edge triggered device.

The EL52 employs input clamping circuitry so that under open input conditions (pulled down to  $V_{EE}$ ) the outputs of the device will remain stable.

The 100 Series contains temperature compensation.

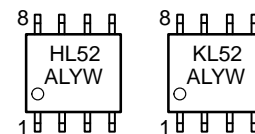
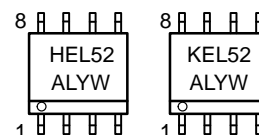
- 365 ps Propagation Delay
- 2.0 GHz Toggle Frequency
- ESD Protection: > 1 KV HBM, > 100 V MM
- PECL Mode Operating Range:  $V_{CC} = 4.2 \text{ V to } 5.7 \text{ V}$  with  $V_{EE} = 0 \text{ V}$
- NECL Mode Operating Range:  $V_{CC} = 0 \text{ V}$  with  $V_{EE} = -4.2 \text{ V to } -5.7 \text{ V}$
- Internal Input Pulldown Resistors on D and CLK
- Meets or Exceeds JEDEC Spec EIA/JESD78 IC Latchup Test
- Moisture Sensitivity Level 1
- For Additional Information, see Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 48 devices



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### MARKING DIAGRAMS\*



H = MC10                      L = Wafer Lot  
K = MC100                    Y = Year  
A = Assembly Location      W = Work Week

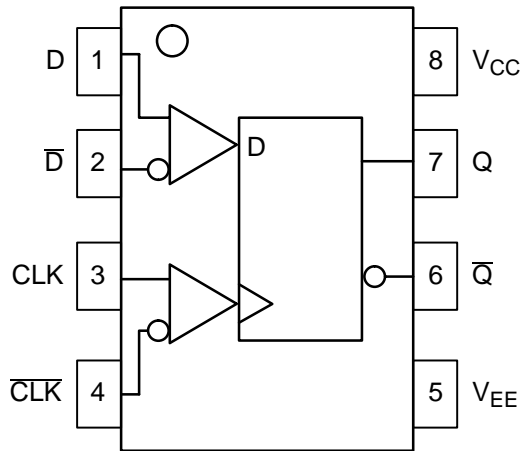
\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC10EL52D	SO-8	98 Units/Rail
MC10EL52DR2	SO-8	2500 Tape & Reel
MC100EL52D	SO-8	98 Units/Rail
MC100EL52DR2	SO-8	2500 Tape & Reel
MC10EL52DT	TSSOP-8	98 Units/Rail
MC10EL52DTR2	TSSOP-8	2500 Tape & Reel
MC100EL52DT	TSSOP-8	98 Units/Rail
MC100EL52DTR2	TSSOP-8	2500 Tape & Reel

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## LOGIC DIAGRAM AND PINOUT ASSIGNMENT



**TRUTH TABLE**

D*	CLK*	Q
L	Z	L
H	Z	H

Z = LOW to HIGH Transition

\* Pin will default low when left open.

**PIN DESCRIPTION**

PIN	FUNCTION
D, $\bar{D}$	ECL Data Input
CLK, $\overline{\text{CLK}}$	ECL Clock Input
Q, $\bar{Q}$	ECL Data Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply

## MAXIMUM RATINGS (Note 1.)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		8	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-8	V
$V_I$	PECL Mode Input Voltage	$V_{EE} = 0\text{ V}$	$V_I \leq V_{CC}$	6	V
	NECL Mode Input Voltage	$V_{CC} = 0\text{ V}$	$V_I \geq V_{EE}$	-6	V
$I_{out}$	Output Current	Continuous Surge		50 100	mA mA
$T_A$	Operating Temperature Range			-40 to +85	°C
$T_{stg}$	Storage Temperature Range			-65 to +150	°C
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
$\theta_{JC}$	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	°C/W
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
$\theta_{JC}$	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44 ± 5%	°C/W
$T_{sol}$	Wave Solder	<2 to 3 sec @ 248°C		265	°C

1. Maximum Ratings are those values beyond which device damage may occur.

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## 10EL SERIES PECL DC CHARACTERISTICS $V_{CC}= 5.0\text{ V}$ ; $V_{EE}= 0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		21	25		21	25		21	25	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	3770		4110	3870		4190	3940		4280	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	3050		3500	3050		3520	3050		3555	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	D	3.4	4.6	3.4		4.6	3.4		4.6	V
		CLK	2.5	4.4	2.5		4.4	2.5		4.4	
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.3			$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  
 $V_{EE}$  can vary +0.25 V / -0.5 V for +25°C and +85°C. or  $V_{EE}$  can vary +0.06 V / -0.5 V for -40°C.
- Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and 1 V.

## 10EL SERIES NECL DC CHARACTERISTICS $V_{CC}= 0.0\text{ V}$ ; $V_{EE}= -5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		21	25		21	25		21	25	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	-1080	-990	-890	-980	-895	-810	-910	-815	-720	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	-1950	-1800	-1650	-1950	-1790	-1630	-1950	-1773	-1595	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1230		-890	-1130		-810	-1060		-720	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1950		-1500	-1950		-1480	-1950		-1445	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	D	-1.6	-0.4	-1.6		-0.4	-1.6		-0.4	V
		CLK	-2.5	-0.6	-2.5		-0.6	-2.5		-0.6	
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.3			$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lpm is maintained.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  
 $V_{EE}$  can vary +0.25 V / -0.5 V for +25°C and +85°C. or  $V_{EE}$  can vary +0.06 V / -0.5 V for -40°C.
- Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.
- $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{PPmin}$  and 1 V.

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## 100EL SERIES PECL DC CHARACTERISTICS $V_{CC}=5.0\text{ V}$ ; $V_{EE}=0.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		21	25		21	25		24	29	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	3835		4120	3835		4120	3835		4120	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	3190		3525	3190		3525	3190		3525	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	D	2.6	4.6	2.6		4.6	2.6		4.6	V
		CLK	2.5	4.2	2.5		4.2	2.5		4.2	
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

## 100EL SERIES NECL DC CHARACTERISTICS $V_{CC}=0.0\text{ V}$ ; $V_{EE}=-5.0\text{ V}$ (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		21	25		21	25		24	29	mA
$V_{OH}$	Output HIGH Voltage (Note 2.)	-1085	-1005	-880	-1025	-955	-880	-1025	-955	-880	mV
$V_{OL}$	Output LOW Voltage (Note 2.)	-1830	-1695	-1555	-1810	-1705	-1620	-1810	-1705	-1620	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1165		-880	-1165		-880	-1165		-880	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1810		-1475	-1810		-1475	-1810		-1475	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 3.)	D	-2.4	-0.4	-2.4		-0.4	-2.4		-0.4	V
		CLK	-2.5	-0.8	-2.5		-0.8	-2.5		-0.8	
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained.

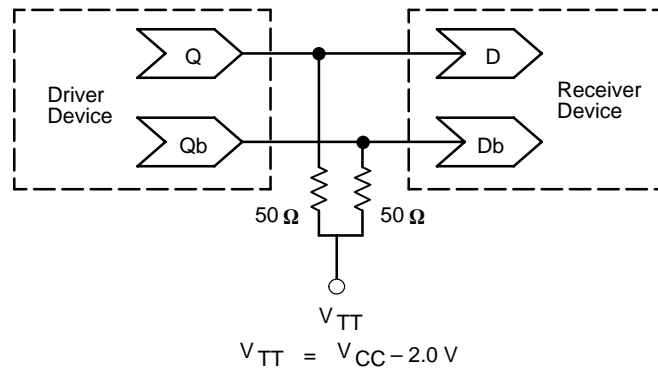
1. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.8 V / -0.5 V.
2. Outputs are terminated through a 50 ohm resistor to  $V_{CC}$ -2 volts.
3.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1 V.

# MC10EL52, MC100EL52

**AC CHARACTERISTICS**  $V_{CC}= 5.0\text{ V}$ ;  $V_{EE}= 0.0\text{ V}$  or  $V_{CC}= 0.0\text{ V}$ ;  $V_{EE}= -5.0\text{ V}$  (Note 1.)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Toggle Frequency	1.8	2.5		2.2	2.8		2.2	2.8		GHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation Delay to Output CLK	225	335	515	275	365	465	320	410	510	ps
$t_{\text{S}}$	Setup Time	125	0		125	0		125	0		ps
$t_{\text{H}}$	Hold Time	150	50		150	50		150	50		ps
$t_{\text{PW}}$	Minimum Pulse Width	400			400			400			ps
$V_{\text{PP}}$	Input Swing (Note 2.)	150		1000	150		1000	150		1000	mV
$t_{\text{JITTER}}$	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
$t_{\text{r}}$ $t_{\text{f}}$	Output Rise/Fall Times Q (20% – 80%)	100	225	350	100	225	350	100	225	350	ps

- 10 Series:  $V_{EE}$  can vary  $+0.25\text{ V} / -0.5\text{ V}$  for  $+25^{\circ}\text{C}$  and  $+85^{\circ}\text{C}$ . or  $V_{EE}$  can vary  $+0.06\text{ V} / -0.5\text{ V}$  for  $-40^{\circ}\text{C}$   
100 Series:  $V_{EE}$  can vary  $+0.8\text{ V} / -0.5\text{ V}$ .
- $V_{\text{PP}}(\text{min})$  is minimum input swing for which AC parameters guaranteed. The device has a DC gain of  $\approx 40$ .



**Figure 1. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020 – Termination of ECL Logic Devices.)

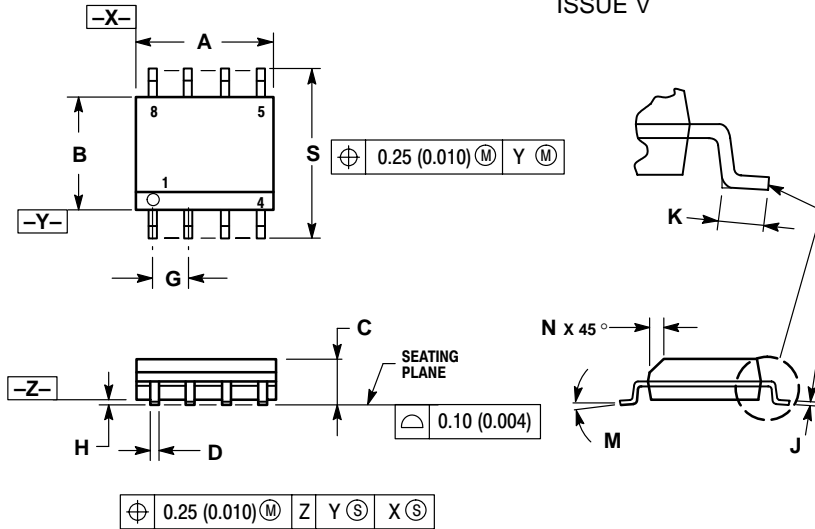
## Resource Reference of Application Notes

- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{\text{IH}}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at  $+5.0\text{ V}$ )
- AN1503** – ECLinPS I/O SPICE Modeling Kit
- AN1504** – Metastability and the ECLinPS Family
- AN1560** – Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** – Interfacing Between LVDS and ECL
- AN1596** – ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8020** – Termination of ECL Logic Devices

# MC10EL52, MC100EL52

## PACKAGE DIMENSIONS

### SO-8 D SUFFIX PLASTIC SOIC PACKAGE CASE 751-07 ISSUE V

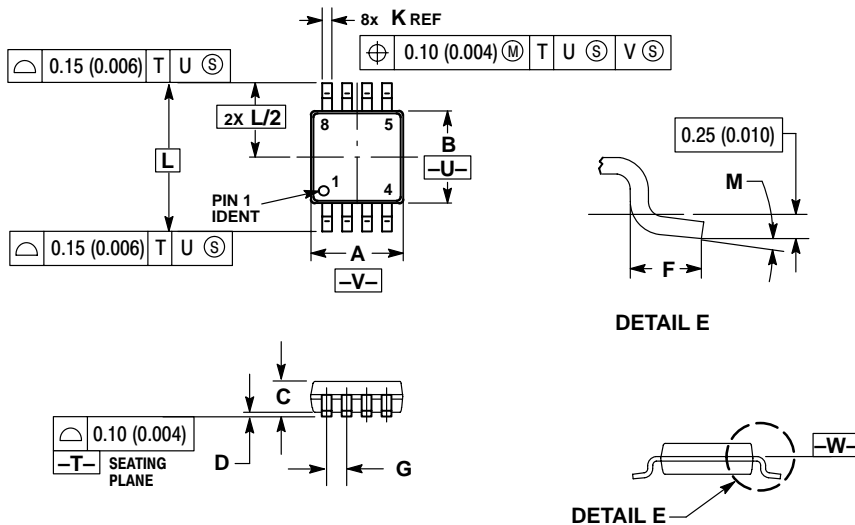


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

## Notes

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