

**μ A139 • μ A239 • μ A339
 μ A2901 • μ A3302
 Quad Comparators**

Linear Division Comparators

Description

The μ A139 series consists of four independent precision voltage comparators designed specifically to operate from a single power supply. Operation from split power supplies is also possible and the low power supply current drain is independent of the supply voltage range. Darlington connected PNP input stages allow the input common mode voltage to include ground.

- **Single Supply Operation +2.0 V To +36 V**
- **Dual Supply Operation ± 1.0 V To ± 18 V**
- **Allow Comparison Of Voltages Near Ground Potential**
- **Low Current Drain 800 μ A Typ**
- **Compatible With All Forms Of Logic**
- **Low Input Bias Current 25 nA Typ**
- **Low Input Offset Current ± 5.0 nA Typ**
- **Low Offset Voltage ± 2.0 mV**

Absolute Maximum Ratings

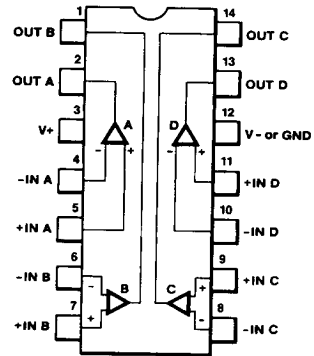
Storage Temperature Range	
Ceramic DIP	-65°C to +175°C
Molded DIP and SO-14	-65°C to +150°C
Operating Temperature Range	
Extended (μ A139M)	-55°C to +125°C
Automotive (μ A2901V, μ A3302V)	-40°C to +85°C
Industrial (μ A239V)	-25°C to +85°C
Commercial (μ A339C)	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP and SO-14 (soldering, 10 s)	265°C
Internal Power Dissipation^{1, 2}	
14L-Ceramic DIP	1.36 W
14L-Molded DIP	1.04 W
SO-14	0.93 W
Supply Voltage	
μ A139 Series/ μ A2901	36 V or ± 18 V
μ A3302	28 V or ± 14 V
Differential Input Voltage	
μ A139 Series/ μ A2901	36 V
μ A3302	28 V
Output Short Circuit to GND³	
	Indefinite
Input Current ($V_I < -0.3$ V)⁴	
	50 mA

Notes

1. T_J Max = 150°C for the Molded DIP and SO-14, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 14L-Ceramic DIP at 9.1 mW/°C, the 14L-Molded DIP at 8.3 mW/°C, and the SO-14 at 7.5 mW/°C.
3. Short circuits from the output to V+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V+.

Connection Diagram

14-Lead DIP and SO-14 Package (Top View)



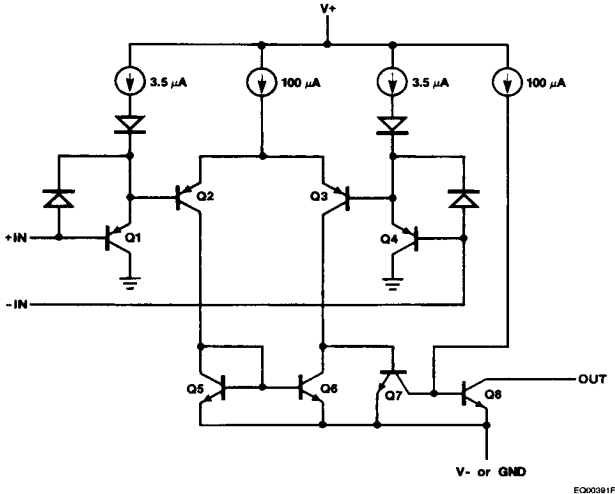
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Order Information

Device Code	Package Code	Package Description
μ A139DM	6A	Ceramic DIP
μ A239DV	6A	Ceramic DIP
μ A239PV	9A	Molded DIP
μ A239SV	KD	Molded Surface Mount
μ A339DC	6A	Ceramic DIP
μ A339PC	9A	Molded DIP
μ A339SC	KD	Molded Surface Mount
μ A2901DV	6A	Ceramic DIP
μ A2901PV	9A	Molded DIP
μ A3302DV	6A	Ceramic DIP
μ A3302PV	9A	Molded DIP
μ A3302SV	KD	Molded Surface Mount

4. This input current will exist only when the voltage at any of the input leads is driven negative. It is due to the collector base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V+ voltage level or to ground for a large overdrive, for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which is negative, again returns to a value greater than -0.3 V.

Equivalent Circuit



μA139 , μA239 , μA339

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_+ = 5.0\text{ V}$, unless otherwise specified.

Symbol	Characteristic	Condition	μA139			μA239 , μA339			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage ⁵			± 2.0	± 5.0		± 2.0	± 5.0	mV
I_{IB}	Input Bias Current ¹	I_{I+} or I_{I-} with Output in Linear Range		25	100		25	250	nA
I_{IO}	Input Offset Current	$(I_{I+}) - (I_{I-})$		± 5.0	± 25		± 5.0	± 50	nA
V_{IR}	Input Common Mode Voltage Range ²		0		$(V_+) - 1.5$	0		$(V_+) - 1.5$	V
I_{CC}	Supply Current	$R_L = \infty$ on all Comparators		0.8	2.0		0.8	2.0	mA
A_{VS}	Large Signal Voltage Gain	$R_L \geq 15\text{ k}\Omega$, $V_+ = 15\text{ V}$ (To Support Large V_O Swing)		200			200		V/mV
t_{PD1}	Large Signal Response Time	$V_I = \text{TTL Logic Swing}$, $V_{REF} = 1.4\text{ V}$, $V_{RL} = 5.0\text{ V}$, $R_L = 5.1\text{ k}\Omega$		300			300		ns
t_{PD2}	Response Time ³	$V_{RL} = 5.0\text{ V}$, $R_L = 5.1\text{ k}\Omega$		1.3			1.3		μs

**$\mu\text{A139} \bullet \mu\text{A239} \bullet \mu\text{A339}$
 $\mu\text{A2901} \bullet \mu\text{A3302}$**

μA139 , μA239 , μA339 (Cont.)

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_+ = 5.0\text{ V}$, unless otherwise specified.

Symbol	Characteristic	Condition	μA139			μA239 , μA339			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{OL}	Output Sink Current	$V_{I-} \geq 1.0\text{ V}$, $V_{I+} = 0\text{ V}$, $V_O \leq 1.5\text{ V}$	6.0	16		6.0	16		mA
V_{SAT}	Saturation Voltage	$V_{I-} \geq 1.0\text{ V}$, $V_{I+} = 0\text{ V}$, $I_{OL} \leq 4.0\text{ mA}$		250	400		250	400	mV
I_{CEX}	Output Leakage Current	$V_{I+} \geq 1.0\text{ V}$, $V_{I-} = 0\text{ V}$, $V_O = 30\text{ V}$			200			200	nA

The following specifications apply for $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ for the μA139 , $-25^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$ for the μA239 and $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ for the μA339 .

V_{IO}	Input Offset Voltage ⁵				9.0			9.0	mV
I_{IO}	Input Offset Current	$(I_{I+}) - (I_{I-})$			± 100			± 150	nA
I_{IB}	Input Bias Current	I_{I+} or I_{I-} with Output in Linear Range			300			400	nA
V_{IR}	Input Voltage Range		0		$(V_+) - 2.0$	0		$(V_+) - 2.0$	V
V_{SAT}	Saturation Voltage	$V_{I-} \geq 1.0\text{ V}$, $V_{I+} = 0\text{ V}$, $I_{OL} \leq 4.0\text{ mA}$			700			700	mV
I_{CEX}	Output Leakage Current	$V_{I+} \geq 1.0\text{ V}$, $V_{I-} = 0\text{ V}$, $V_O = 30\text{ V}$			1.0			1.0	μA
V_{ID}	Differential Input Voltage ⁴	Keep all $V_{I's} \geq 0\text{ V}$ (or V_{-} , if used)			36			36	V

μA139 • μA239 • μA339
μA2901 • μA3302

μA2901, μA3302

Electrical Characteristics $T_A = 25^\circ\text{C}$, $V_+ = 5.0\text{ V}$, unless otherwise specified.

Symbol	Characteristic	Condition	μA2901			μA3302			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage ⁵			± 2.0	± 7.0		± 3.0	± 2.0	mV
I_{IB}	Input Bias Current ¹	I_{I+} or I_{I-} with Output in Linear Range		25	250		25	500	nA
I_{IO}	Input Offset Current	$(I_{I+}) - (I_{I-})$		± 5.0	± 50		± 5.0	± 100	nA
V_{IR}	Input Common Mode Voltage Range ²		0		$(V_+) - 1.5$	0		$(V_+) - 1.5$	V
I_{CC}	Supply Current	$R_L = \infty$ on all Comparators		0.8	2.0		0.8	2.0	mA
		$R_L = \infty$, $V_+ = 30\text{ V}$		1.0	2.5				
A_{VS}	Large Signal Voltage Gain	$R_L \geq 15\text{ k}\Omega$, $V_+ = 15\text{ V}$ (To Support Large V_O Swing)	25	100		2.0	30		V/mV
t_{PD1}	Large Signal Response Time	$V_I = \text{TTL Logic Swing}$, $V_{REF} = 1.4\text{ V}$, $V_{RL} = 5.0\text{ V}$, $R_L = 5.1\text{ k}\Omega$		300			300		ns
t_{PD2}	Response Time ³	$V_{RL} = 5.0\text{ V}$, $R_L = 5.1\text{ k}\Omega$		1.3			1.3		μs
I_{OL}	Output Sink Current	$V_{I-} \geq 1.0\text{ V}$, $V_{I+} = 0\text{ V}$, $V_O \leq 1.5\text{ V}$	6.0	16		2.0	16		mA
V_{SAT}	Saturation Voltage	$V_{I-} \geq 1.0\text{ V}$, $V_{I+} = 0\text{ V}$, $I_{OL} \leq 4.0\text{ mA}$			400		250	500	mV
I_{CEX}	Output Leakage Current	$V_{I+} \geq 1.0\text{ V}$, $V_{I-} = 0\text{ V}$, $V_O = 30\text{ V}$			200			200	nA

μA2901, μA3302 (Cont.)

Electrical Characteristics $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$, $V_+ = 5.0\text{ V}$, unless otherwise specified.

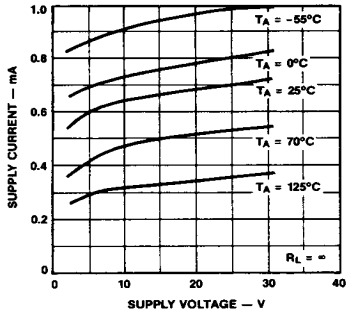
Symbol	Characteristic	Condition	μA2901			μA3302			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{IO}	Input Offset Voltage ⁵			9.0	15			40	mV
I_{IO}	Input Offset Current	$(I_{I+}) - (I_{I-})$		50	200			300	nA
I_{IB}	Input Bias Current	I_{I+} or I_{I-} with Output in Linear Range		200	500			1000	nA
V_{IR}	Input Voltage Range		0		$(V_+) - 2.0$	0		$(V_+) - 2.0$	V
V_{SAT}	Saturation Voltage	$V_{I-} \geq 1.0\text{ V}$, $V_{I+} = 0\text{ V}$, $I_{OL} \leq 4.0\text{ mA}$		400	700			700	mV
I_{CEX}	Output Leakage Current	$V_{I+} \geq 1.0\text{ V}$, $V_{I-} = 0\text{ V}$, $V_O = 30\text{ V}$			1.0			1.0	μA
V_{ID}	Differential Input Voltage ⁴	Keep all $V_{I's} \geq 0\text{ V}$ (or V_- , if used)			V_+			V_+	V

Notes

1. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
2. The input common mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common mode voltage range is $(V_+) - 1.5\text{ V}$, but either or both inputs can go to +30 V without damage.
3. The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance curves segment.
4. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common mode range, comparator will provide a proper output state. The low input voltage state must not be less than -0.3 V or 0.3 V below the magnitude of the negative power supply, if used.
5. At output switch point, $V_O \approx 1.4\text{ V}$, $R_S = 0\ \Omega$ with V_+ from 5.0 V; and over the full input common mode range 0 V to $V_+ - 1.5\text{ V}$.
6. For input signals that exceed V_{CC} , only the overdriven comparator is affected. With a 5.0 V supply, V_I should be limited to 25 V maximum and a limiting resistor should be used on all inputs that might exceed the positive supply.

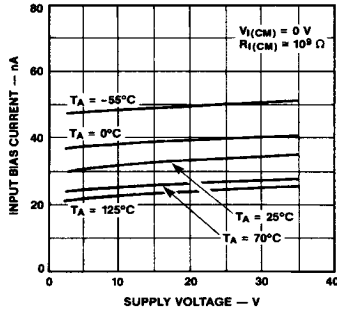
Typical Performance Curves for $\mu\text{A}139, \mu\text{A}239, \mu\text{A}339$

Supply Current



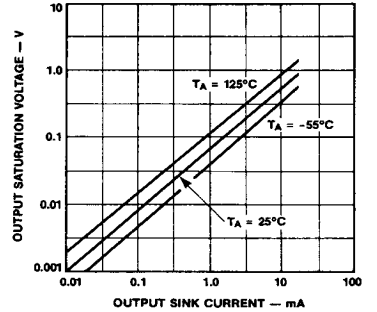
PC06900F

Input Bias Current



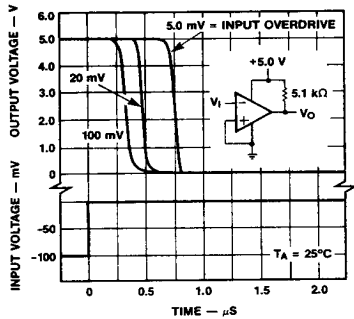
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Output Saturation Voltage



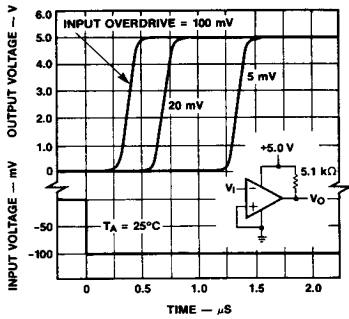
PC06970F

Response Time for Various Input Overdrives — Negative Transition



PC06900F

Response Time for Various Input Overdrives — Positive Transition

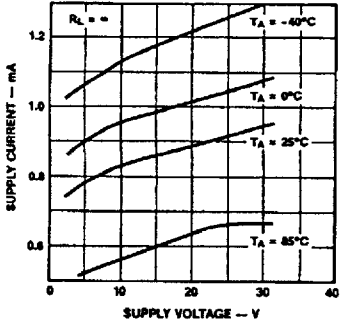


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$\mu A139 \bullet \mu A239 \bullet \mu A339$
 $\mu A2901 \bullet \mu A3302$

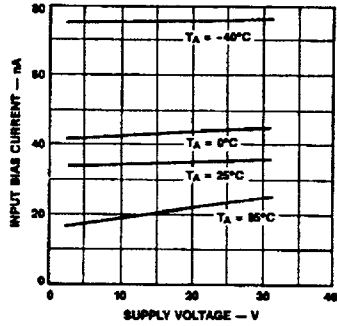
Typical Performance Curves for $\mu A2901, \mu A3302$

Supply Current



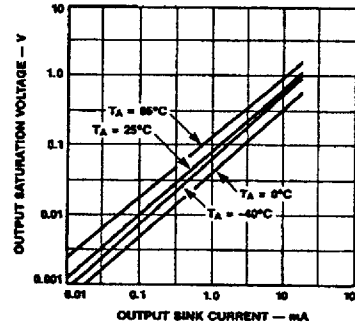
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Input Bias Current



PC06950F

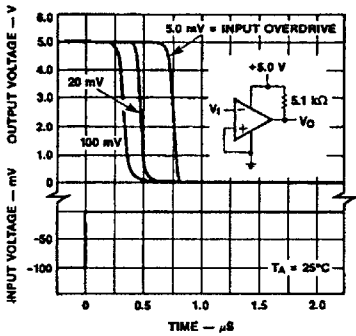
Output Saturation Voltage



PC06921F

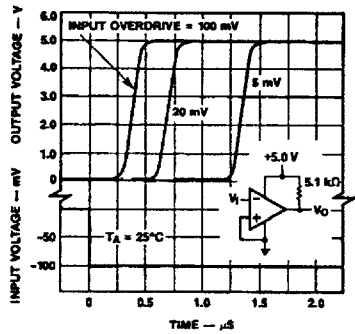
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Response Time for Various Input Overdrives — Negative Transition



PC06950F

Response Time for Various Input Overdrives — Positive Transition



PC06950F

Application Information

The $\mu\text{A}139$ series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input/output coupling. Reducing the input resistors to $< 10 \text{ k}\Omega$ reduces the feedback signal levels and finally, adding even a small amount (1.0 V to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the leads will cause input/output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All leads of any unused comparators should be grounded.

The bias network of the $\mu\text{A}139$ series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of 2.0 V to 30 V.

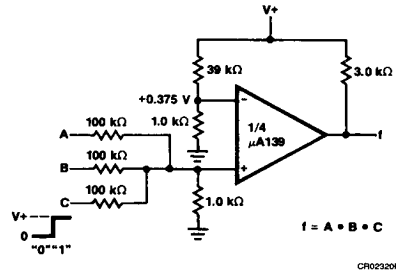
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than $V+$ without damaging the device. Protection should be provided to prevent the input voltages from going more negative than -0.3 V (at 25°C). An input clamp diode can be used as shown in the applications segment of this data sheet.

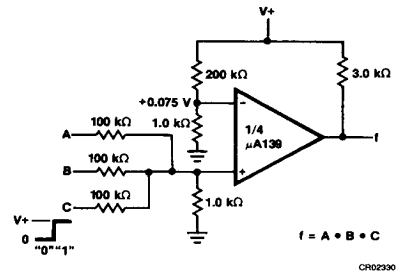
The output of the $\mu\text{A}139$ series is the uncommitted collector of grounded emitter NPN output transistor. Many collectors can be tied together to provide wired OR output function. An output pull-up resistor can be connected to any available power supply within the permitted supply voltage range. There is no restriction on this voltage due to the magnitude of the voltage which is applied to the $V+$ terminal of the $\mu\text{A}139$ package. The output can also be used as a simple SP/ST switch to ground (when a pull up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of $V+$) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60Ω saturation resistance of the output transistor. The low offset voltage of the output transistor (1.0 mV) allows the output to clamp essentially to ground level for small load currents.

Typical Applications ($V+ = 15 \text{ V}$)

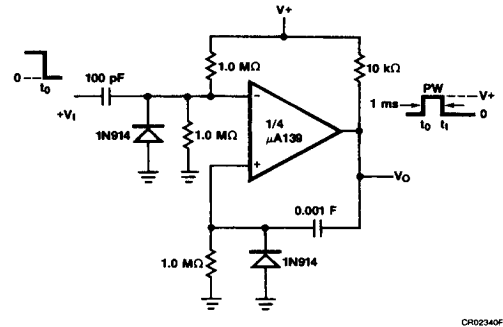
AND Gate



OR Gate



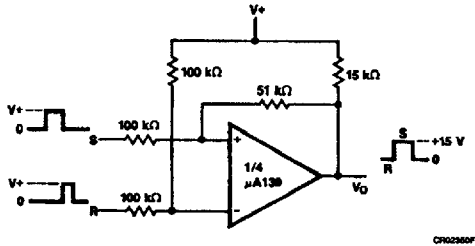
Monostable Multivibrator



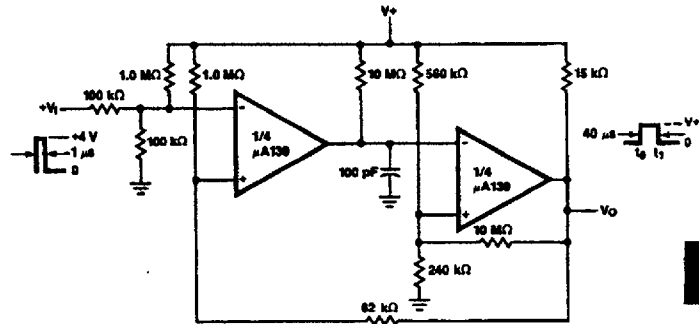
$\mu A139 \cdot \mu A239 \cdot \mu A339$
 $\mu A2901 \cdot \mu A3302$

Typical Applications ($V^+ = 15\text{ V}$) (Cont.)

Bistable Multivibrator

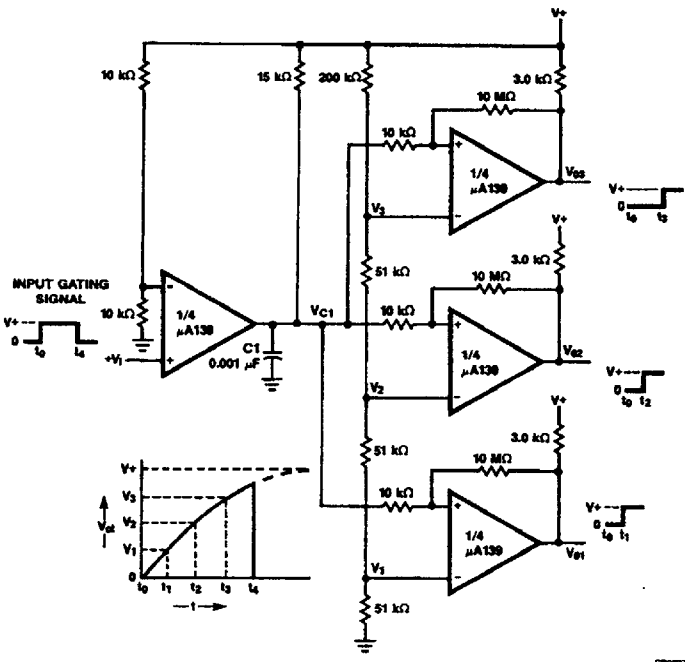


Monostable Multivibrator with Input Lock Out

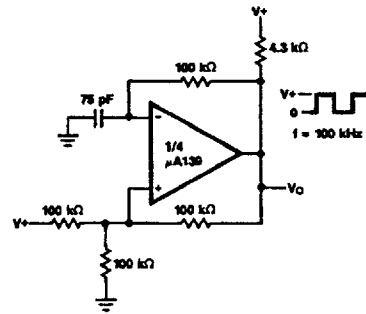


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Time Delay Generator

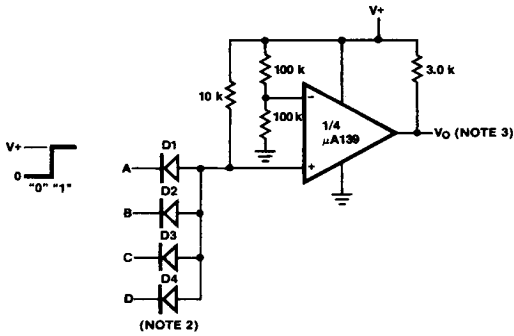


Squarewave Oscillator



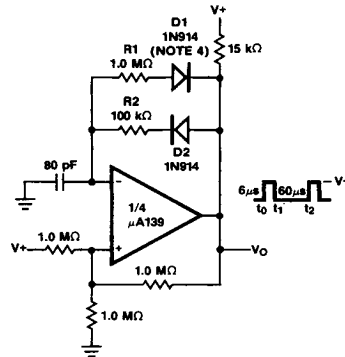
Typical Applications (V+ = 15 V) (Cont.)

Large Fan-In AND Gate (Note 1)



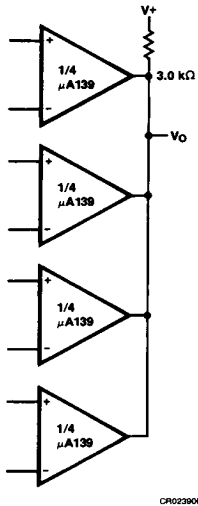
CR02400F

Pulse Generator



CR02410F

Wired-OR Outputs



CR02290F

Notes

- 1) All resistor values in ohms.
- 2) All diodes 1N914.
- 3) $V_O = A \cdot B \cdot C \cdot D$
- 4) For large ratios of R1/R2, D1 can be omitted.