HOLT INTEGRATED CIRCUITS INC.

HI-6110

MIL-STD-1553 / MIL-STD-1760 BC / RT / MT Message Processor

November 2006

GENERAL DESCRIPTION

The HI-6110 is a CMOS integrated circuit implementing the MIL-STD-1553 (1553) data communications protocol between a host processor and a dual redundant 1553 data bus. The single chip architecture has a digital section containing all necessary logic and memory to process and store the command and data words for one complete 1553 message. The analog section includes dual transceivers coupled to the 1553 buses through external current mode transformers. The device is available in an industry standard 64-pin 9 mm square LPCC package, making it the smallest dual redundant 1553 interface product on the market.

The HI-6110 may be configured as a Bus Controller (BC), a Remote Terminal (RT), a Monitor Terminal (MT), or a Monitor Terminal with assigned RT address. 16-bit registers store incoming and outgoing Command, Status and Data words. Using two 32-word data FIFOs, the HI-6110 can store the maximum number of 1553 words occurring in any message. For messages with transmitted data words, data may be written in advance or on-the-fly. Received data can be retrieved on-the-fly or all at once after the Valid Message flag is asserted.

BC message sequences are initiated by a rising edge on the BCSTART input, or a 0 to 1 transition at the BCSTART bit in the Control Register. All RT command responses are automatically initiated after a valid Command Word is received.

Each bus has a dedicated Manchester encoder and analog transformer driver. Each driver dissipates less than 200 mW of on-chip power at 100% duty cycle.

Each bus receiver has a dedicated Manchester decoder. In BC mode, a RCV signal indicates when valid 1553 words are received. In RT/MT modes, RCV indicates a valid command received, while the 1553 command decoder updates a Message register so the external controller can identify command type and respond appropriately. Guaranteed by design, the HI-6110 cannot generate messages exceeding 660uS, the duration of a Command or Status Word plus 32 contiguous data words.

The external host controller reads and writes a simplified register structure in the HI-6110 over a 16-bit parallel bus. The system designer has flexibility over many aspects of configuration. Control and status monitoring can be done in hardware (by reading/writing control pins) or in software (by reading/writing register bits).

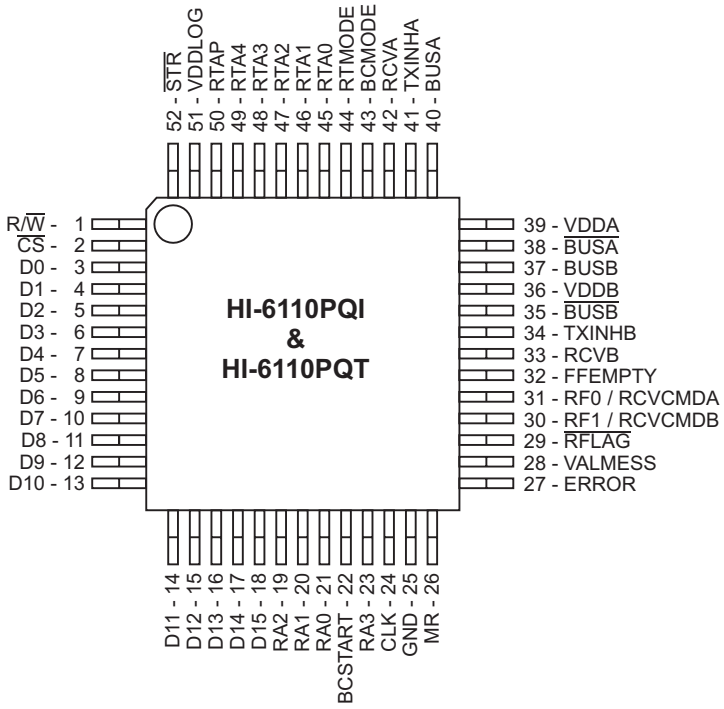
FEATURES

- Monolithic CMOS technology
- 3.3V operation
- Exceptionally low power
- On-chip message buffering
- Selectable master clock frequency
- Dual differential 1553 bus transceivers
- Bus Controller / Remote Terminal / Monitor Terminal operating modes
- Compliant to MIL-STD-1553B Notice 2 and MIL-STD-1760 Stores Management

APPLICATIONS

- MIL-STD-1553 Terminals
- Flight Control and Monitoring
- ECCM Interfaces
- Stores Management
- Test Equipment
- Sensor Interfaces
- Instrumentation

PIN CONFIGURATION (Top View)



52 Pin Plastic Quad Flat Pack (PQFP)

See page 35 for 64-Pin LPCC Pin Configuration

PIN DESCRIPTIONS

SIGNAL	FUNCTION	DESCRIPTION
$\overline{\text{STR}}$	INPUT	During I/O operations, data is latched on rising edge. (12K ohm pull-up resistor)
R/$\overline{\text{W}}$	INPUT	Device register access, READ = 1, WRITE = 0. (12K ohm pull-up resistor)
$\overline{\text{CS}}$	INPUT	Chip Select for register reads and writes, active low. (12K ohm pull-down resistor)
D0 - D15	I/O	Data bus signals. (12K ohm pull-down resistors)
RA0 - RA3	INPUTS	Register access address, inputs are ORed with corresponding Control register bits. (12K ohm pull-down resistors)
BCSTART	INPUT	Message starts on rising edge when in BC mode. Input is ORed with a corresponding Control register bit, where a 0 to 1 transition will also trigger message start. (This input has a 12K ohm pull-down resistor.)
CLK	INPUT	System Clock. (12K ohm pull-down resistor)
GND	POWER	Power supply Ground, 0V.
MR	INPUT	Master Reset, active high. Clears all data FIFOs and all registers except the Control, Transmit Status Word and Transmit Mode Data Word registers. This input is ORed with a corresponding Control register bit. (12K ohm pull-down resistor)
ERROR	OUTPUT	ERROR goes high when a message error is detected. In BC mode, ERROR resets when BCSTART is asserted to begin the next message. For RT and MT modes, ERROR resets automatically after 3 to 4uS. This output signal mirrors a corresponding Status register bit.
VALMESS	OUTPUT	Goes high at the end of a valid message sequence. This output signal mirrors a corresponding Status register bit.
FFEMPTY	OUTPUT	When low, data is available in the receive data FIFO for the active bus. This output signal mirrors a corresponding Status register bit.
$\overline{\text{RFLAG}}$	OUTPUT	Flag for register writes of received message words other than Data words. In BC mode: Goes low when a Status Word register is written. In RT or MT mode: Goes low when either a Command word, Status word, or Mode data word register is received and written in a register. This output mirrors a corresponding Status register bit.
RF0 / RCVCMDA	OUTPUT	RF0 function: If a “1” when reading Bus A Word or Bus B Word registers, the stored word had data sync. RCVCMDA function: In RT mode or MT mode, RCVCMDA goes high when a valid receive command has been decoded on Bus A. This output mirrors a corresponding Status register bit.
RF1 / RCVCMDB	OUTPUT	RF1 function: If a “1” when reading Bus A Word or Bus B Word registers, the stored word had command sync. RCVCMDB function: In RT mode or MT mode, RCVCMDB goes high when a valid receive command has been decoded on Bus B. This output mirrors a corresponding Status register bit.
RCVA RCVB	OUTPUTS	Receive A and Receive B flags: In BC mode, these signals go high when any valid word is received on Bus A or Bus B. In RT or MT mode, these signals go high when a valid command is received on Bus A or Bus B. For valid RT-to-RT only, RCV goes high after command word pair. These output signals mirror two corresponding Status register bits.
TXINHA	INPUT	Logic one disables the Bus A transmitter. (12K ohm pull-up resistor)
TXINHB	INPUT	Logic one disables the Bus B transmitter. (12K ohm pull-up resistor)
BUSA, $\overline{\text{BUSA}}$ BUSB, $\overline{\text{BUSB}}$	XFMR	Positive and negative polarity of 1553 signals for Buses A and B. These signal pairs connect the analog transceivers to the external transformer.
BCMODE	INPUT	Selects operating mode. This input signal is ORed with a corresponding Control register bit. (12K ohm pull-up resistor)
RTMODE	INPUT	Selects operating mode. This input signal is ORed with a corresponding Control register bit. (12K ohm pull-down resistor)
RTA0-RTA4	INPUTS	Remote Terminal address inputs, for RT mode. (12K ohm pull-up resistors)
RTAP	INPUT	This input sets Remote Terminal address parity, odd. (12K ohm pull-down resistor)
VDDLOG	POWER	+3.3VDC ±5% power supply input for internal logic
VDDA, VDDB	POWER	+3.3VDC ±5% power supply inputs for Bus A and Bus B transceivers

FUNCTIONAL DESCRIPTION

HOST INTERFACE

The Holt HI-6110 provides a simple interface between a host subsystem and a MIL-STD-1553 dual redundant data bus. Messages are processed one at a time. The HI-6110 automatically handles message formatting, error checking, message data buffering, protocol checking and default responses. The host may override default message responses by updating registers on-the-fly.

The host communicates with the HI-6110 using a 16-bit bidirectional data bus. On-chip bus transceivers allow the device to be connected to the MIL-STD-1553 data buses using external coupling transformers.

The HI-6110 can be configured as 1553 Bus Controller (BC), Remote Terminal (RT) or Bus Monitor (MT). The BCMODE and RTMODE inputs define the mode of operation as follows:

BCMODE	RTMODE	1553 OPERATING MODE
1	0	Bus Controller (BC)
0	1	Remote Terminal (RT)
1	1	Bus Monitor (no assigned RT address)
0	0	Bus Monitor with assigned RT address

The HI-6110 is further configured by setting various configuration bits in the on-chip Control Register. Different sets of 16-bit registers and message data FIFOs are available depending upon the mode of operation (BC, RT or MT). The $\overline{STR}$ pin is used as the timing signal for data read and write cycles. Data is output on the 16-bit bidirectional data bus, D15-D0, when R/$\overline{W}$ is high and $\overline{STR}$ is low. D15-D0 are inputs when R/$\overline{W}$ is low, and data is written into internal registers on the rising edge of the $\overline{STR}$ signal. The Chip Select input $\overline{CS}$ must be low for all register read / write operations:

$\overline{CS}$	R/$\overline{W}$	$\overline{STR}$	D15-D0	OPERATION
1	X	X	High impedance	No operation
0	X	1	High impedance	No operation
0	1	0	Output	Read
0	0	0	Input	Write (on $\overline{STR}$ rising edge)

Four Register address inputs (RA3, RA2, RA1, RA0) are used to select internal registers during host read or write operations. Note that internal registers may be write-only, read-only or read/write. The register address map is different for BC, RT and MT modes as not all registers are used in each mode. Table 1 defines the HI-6110 address map in detail.

Table 1. HI-6110 Internal Register Address Map

REGISTER READ (R/$\overline{W}$=1)			
ADDRESS	MODE		
RA3:0	BC	RT or MT with assigned RT address	MT without assigned RT address
0 0 0 0	STATUS WORD 1 (if RT-RT, Receive RT)	COMMAND WORD 1	COMMAND WORD 1
0 0 0 1	STATUS WORD 2 only RT-RT Transmit RT	COMMAND WORD 2 (from last RT-RT)	COMMAND WORD 2 (from last RT-RT)
0 0 1 0	-	RECEIVED MODE DATA WORD	RECEIVED MODE DATA WORD
0 0 1 1	-	RECEIVED STATUS WORD (from last RT-RT)	Xmitting RT STATUS WORD for RTRT
0 1 0 0	RECEIVED DATA FIFO	RECEIVED DATA FIFO	DATA FIFO, includes Xmitted Mode Data
0 1 0 1	STATUS REGISTER	STATUS REGISTER	STATUS REGISTER
0 1 1 0	-	MESSAGE REGISTER	MESSAGE REGISTER
0 1 1 1	ERROR REGISTER	ERROR REGISTER	ERROR REGISTER
1 0 0 0	-	-	STATUS WORD (Receiving RT if RTRT)
1 0 0 1	BUS A WORD	BUS A WORD	BUS A WORD
1 0 1 0	BUS B WORD	BUS B WORD	BUS B WORD
1 1 0 0	CONTROL REGISTER	CONTROL REGISTER	CONTROL REGISTER

REGISTER WRITE (R/$\overline{W}$=0)			
ADDRESS	MODE		
RA3:0	BC	RT or MT with assigned RT address	MT without assigned RT address
X 0 0 0	COMMAND WORD 1	TRANSMIT STATUS WORD	
X 0 0 1	COMMAND WORD 2 (used for RT-RT only)	TRANSMIT MODE DATA WORD	-
X 0 1 0	TRANSMIT DATA FIFO	RESET TRANSMIT DATA FIFO	-
X 0 1 1	-	TRANSMIT DATA FIFO	-
X 1 X X	CONTROL REGISTER	CONTROL REGISTER	CONTROL REGISTER

Table 2. MIL-STD-1553 Word Type Decoding

SIGNALS RF1 AND RF0 IDENTIFY LAST RECEIVED 1553 WORD TYPE			
SIGNAL		MODE	
RF1 RF0	BC	RT or MT with assigned RT address	MT without assigned RT address
0 0	-	-	-
0 1	pulses low if STATUS WORD 2	Valid Receive Command Bus A	Valid Receive Command Bus A
1 0	-	Valid Receive Command Bus B	Valid Receive Command Bus B

While reading the BUS A WORD or BUS B WORD registers, sync type for the stored word can be determined from the RF0 and RF1 outputs.
While the /STR input is held low, output RF1 = 1 if the stored Bus Word had Command Sync, or output RF0 = 1 if the stored Bus Word had Data Sync.

BUS CONTROLLER

The HI-6110 is configured for Bus Controller operation by setting the BCMODE input high and the RTMODE input low. Alternatively, Control Register bits 3:2 (RTMODE:BCMODE) may be programmed to 0:1. Control Register bits 3:2 are logically ORed with the input pins with the same signal name.

Figure 1. shows a block diagram of the HI-6110 in Bus Controller mode

INITIALIZATION

In Bus Controller mode, the user must first perform a Master Reset to initialize the BC protocol engine and clear all message registers and data FIFOs. This may be achieved by pulsing the MR input high, or writing a "1" to Control Register bit 0. The user must select a master clock (CLK) frequency by programming Control Register bits 11 and 12, and the Response Time Out must be programmed per Control Register bit 14. Refer to the BC Register Formats section for a full description of available registers and their functions in Bus Controller Mode.

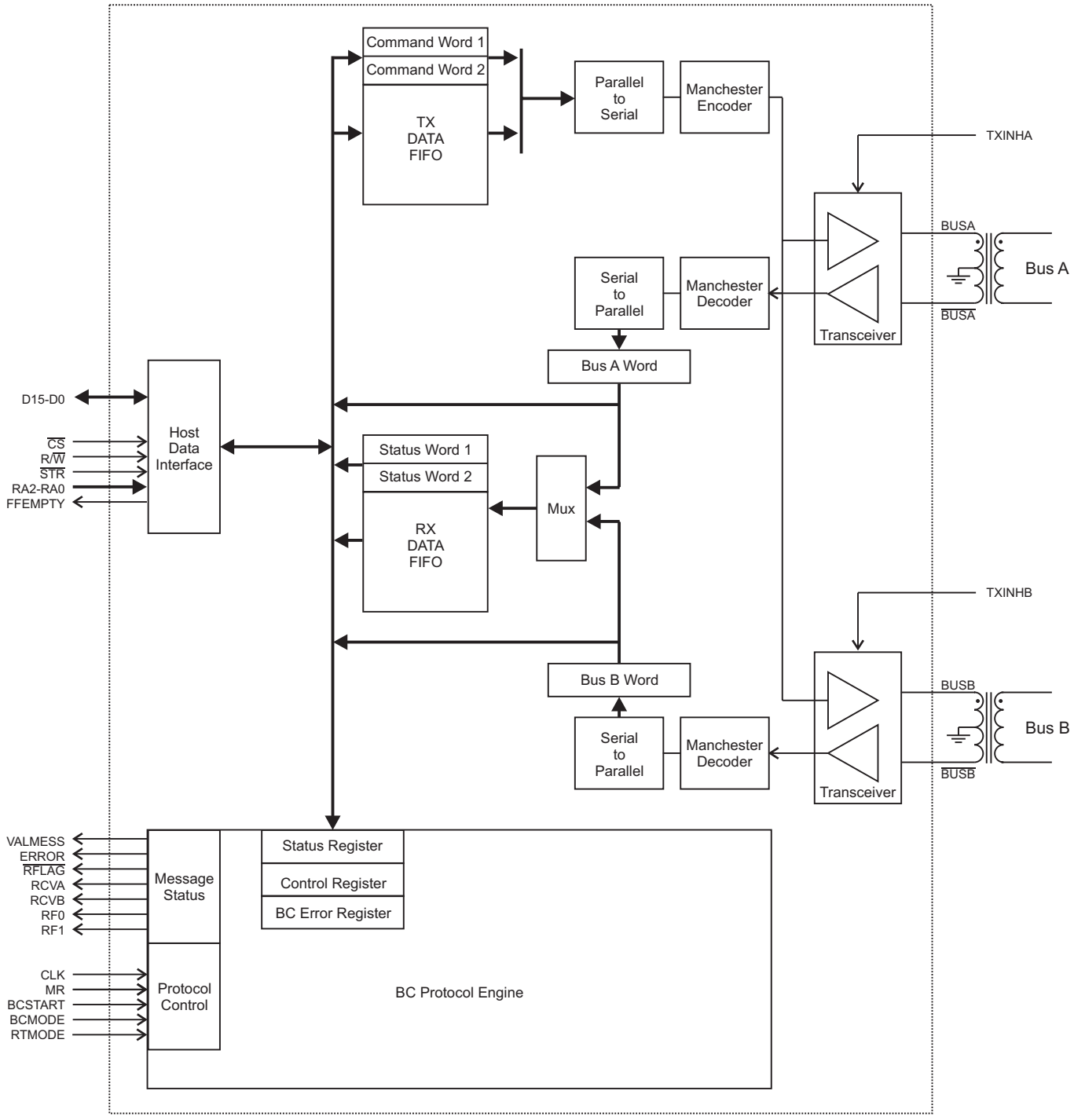
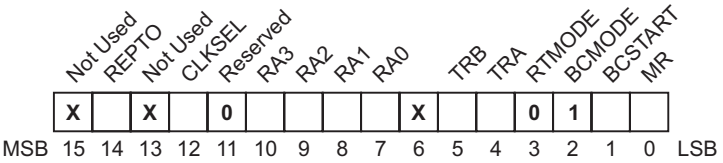


Figure 1. Block Diagram - Bus Controller Mode

REGISTER FORMATS (BC Mode)

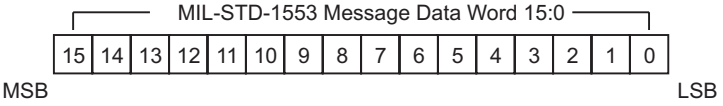
CONTROL REGISTER (R/W) Write Address: X1XX, Read Address: 1100



The Control Register settings determine HI-6110 operating mode, clock frequency and the bus enabled for transmit. It can also be used to address registers for read/write operations, to assert master reset, and to initiate MIL-STD-1553 message sequences.

BIT	NAME	FUNCTION
15	-	Not used in BC mode
14	REPTO	Controls the time-out which causes the No Response Error. 0 — 17 usec Gap (equivalent to 57 usec for 5.2.1.7 of the RT Validation Test Plan) 1 — 131 usec Gap
13	-	Not used in BC mode
12	CLKSEL	Selects the frequency of the HI-6110 external CLK input, as follows: CLKSEL — Value 0 — 24 MHz 1 — 12 MHz
11	Reserved	This bit must be written to “0”.
10 - 7	RA3:0	Register Address for HI-6110 register and data read and write operations. The register address is defined by the logical OR of these bits and their corresponding input pins. Writting Control Register bits 10:7 to 0000 is necessary if the RA0 - RA3 input pins are used for HI-6110 register addressing.
6	-	Not used in BC mode
5 - 4	TRB, TRA	Setting either TRA or TRB to "1" enables transmit on MIL-STD-1553 BUS A or BUS B. Setting both TRA and TRB selects neither bus. The BC protocol engine connects to the selected, active bus. The 1553 receiver, Manchester decoder and RCV output signal are still operational on the inactive bus. Valid words received on the inactive bus can be read without changing active bus by reading the Bus A Word or Bus B Word register. NOTE: The TXINHA and TXINHB input pins can override bus enablement.
3 - 2	RTMODE, BCMODE	HI-6110 mode select bits. These Control Register bits are logically OR'ed with their corresponding input pins, allowing the user to select 1553 operating mode under either hardware or software control: RTMODE — BCMODE — 1553 OPERATING MODE 0 — 0 — Bus Monitor (MT), with assigned RT address 0 — 1 — Bus Controller (BC) 1 — 0 — Remote Terminal (RT) 1 — 1 — Bus Monitor (MT), without assigned RT address
1	BCSTART	If initially reset, writing a "1" to this bit initiates a BC message sequence. This bit should be reset before next message.
0	MR	Master Reset. Writing "1" and then “0” to this bit performs the same function as pulsing the MR pin. All register and data FIFOs are cleared when master reset is asserted. The Control Register is the exception; it is not affected by Master Reset.

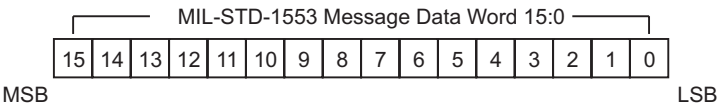
TRANSMIT DATA FIFO (Write only) Write Address: X010



The Transmit Data FIFO is 32-words deep and holds MIL-STD-1553 message data. The FIFO is cleared on Master Reset.

Message data to be transmitted by the BC may be loaded into the TRANSMIT DATA FIFO by the host prior to BCSTART. Any data word must be loaded before mid-parity bit for the 1553 word it follows. Words are transmitted in the order they are loaded.

RECEIVE DATA FIFO (Read only) Read Address: 0100

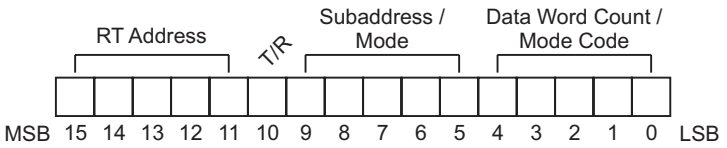


The Receive Data FIFO is 32-words deep and holds MIL-STD-1553 message data. The FIFO is cleared by Master Reset or when BCSTART occurs.

All MIL-STD-1553 data words received by the BC are stored in the Receive DATA FIFO. A low FFEMPTY flag (output pin or Status register bit) means message data is available to be read by the host. Successive data reads cause FFEMPTY to go high when the last word is read.

BC OPERATION

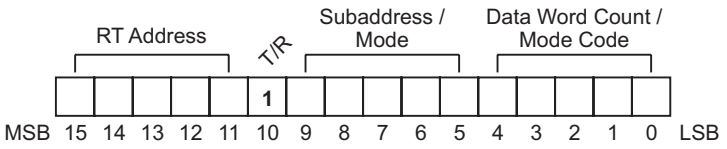
COMMAND WORD 1 REGISTER (Write only) Write Address: X000



The Command Word 1 register is loaded by the host with the MIL-STD-1553 Command Word to be issued by the Bus Controller. Bit 10 should be set for Transmit, reset for Receive.

For RT to RT commands, Command Word 1 register holds the receive command word and Command Word 2 register holds the transmit command word.

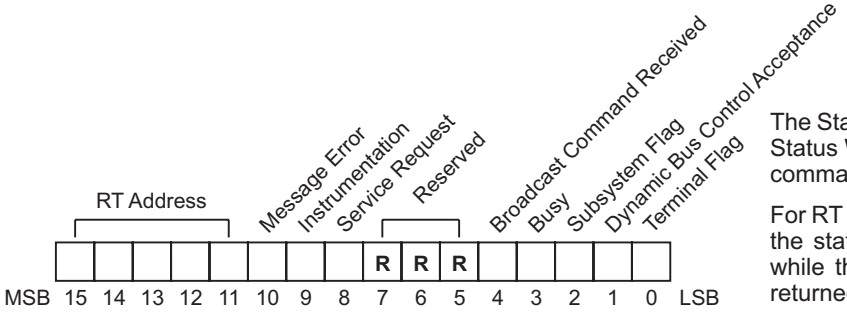
COMMAND WORD 2 REGISTER (Write only) Write Address: X001



Used only for RT-to-RT commands, the Command Word 2 register is loaded by the host with the MIL-STD-1553 transmit Command Word addressed to the transmitting Remote Terminal. The Command Word 1 register is loaded with the receive Command Word addressed to the receiving Remote Terminal.

If the next Message is not an RT-to-RT transfer, it is necessary to write the Transmit/Receive bit 10 to “0”.

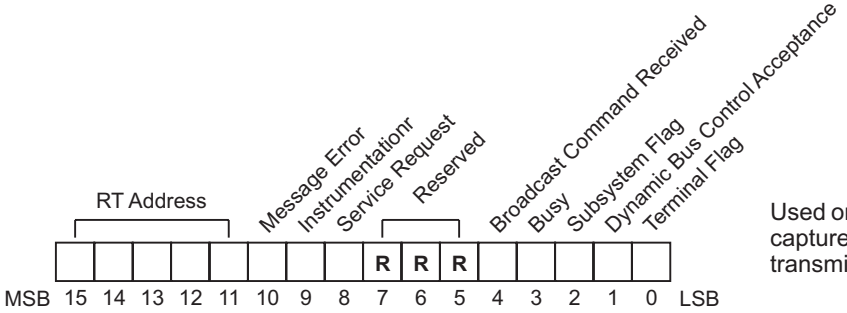
STATUS WORD 1 REGISTER (Read only) Read Address: 0000



The Status Word 1 register holds the returned MIL-STD-1553 Status Word received from an RT responding to a BC issued command.

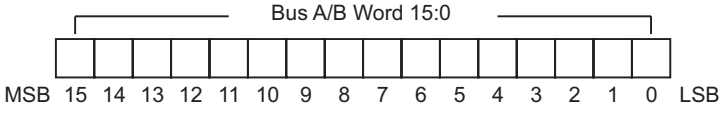
For RT to RT commands, the Status Word 1 register captures the status word returned by the receiving remote terminal, while the Status Word 2 register captures the status word returned by the transmitting remote terminal

STATUS WORD 2 REGISTER (Read only) Read Address: 0001



Used only for RT to RT commands, the Status Word 2 register captures the MIL-STD-1553 status word returned by the transmitting remote terminal.

BUS A WORD REGISTER (Read only) Read Address: 1001
BUS B WORD REGISTER (Read only) Read Address: 1010

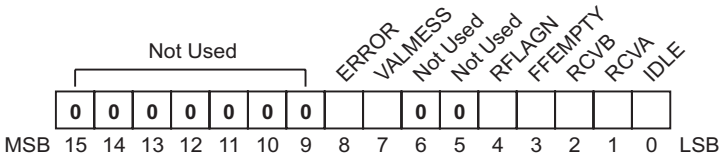


In BC mode, the Bus A Word register holds the last valid MIL-STD-1553 word received on Bus A. The Bus B Word register holds the last valid MIL-STD-1553 word received on Bus B.

While /STROBE is low to read a Bus Word register, the sync type associated with the stored word can be determined from the RF0 and RF1 pins. The RF1 signal is high for Command Sync, the RF0 signal is high for Data Sync.

BC OPERATION

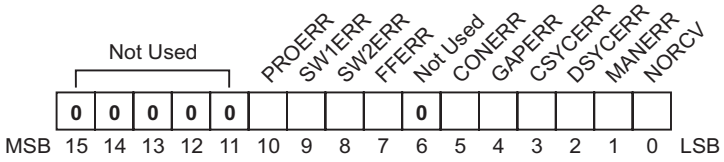
STATUS REGISTER (Read only) Read Address: 0101



The Status Register may be interrogated by the host at any time. It provides information that allows the user to determine whether the HI-6110 is busy executing a MIL-STD-1553 message and its progress. After a message sequence has completed, the Status register indicates whether an error was detected or if the message sequence was successful.

BIT	NAME	FUNCTION
15- 9	-	Not used. These bits are set to "0".
8	ERROR	This bit is "0" after Master Reset or if the last MIL-STD-1553 message sequence was valid. ERROR is set to a "1" if the last sequence had an error. The nature of the message error can be determined by examining the Error Register. The ERROR output pin reflects the state of this bit.
7	VALMESS	This bit is a "0" after reset or the last MIL-STD-1553 message containing an error. VALMESS goes high on the completion of an error-free MIL-STD-1553 message sequence. VALMESS is reset to a zero at the start of each new BC message. The VALMESS output pin reflects the state of this bit.
5-6	-	Not used.
4	RFLAGN	This bit goes low any time a Status Word is received
3	FFEMPTY	If "0" then the receive Data FIFO contains at least one word of data. This bit is set to a "1" on reset, or when a new BC command sequence is initiated, or when the user has read all available received data words from the receiver Data FIFO. The FFEMPTY output pin reflects the state of this bit.
2	RCVB	Set to a "1" if the Bus B Word register holds a valid MIL-STD-1553 word.
1	RCVA	Set to a "1" if the Bus A Word register holds a valid MIL-STD-1553 word.
0	IDLE	If "1" then the Bus Controller is idle. This bit is a zero throughout the time a MIL-STD-1553 message is in progress. The bit returns to a "1" when the message is completed.

ERROR REGISTER (Read only) Read Address: 0111



The BC Error Register is cleared at reset and at the beginning of each MIL-STD-1553 message sequence. If an error is encountered during message execution, the ERROR pin goes high, the ERROR bit is set in the Status Register, and one or more bits are set in the Error Register. After the error condition is flagged, the Error Register should be interrogated before the receipt of the next Manchester Word.

BIT	NAME	FUNCTION
15 - 11	-	Not used. These bits are set to "0".
10	PROERR	Protocol Error: Extraneous word detected on the bus during a message sequence.
9	SW1ERR	Status Word 1 Error: In an RT-RT sequence. the receiving RT Status Word has the wrong RT address. For RT to RT transfers, SW1ERR reports an error in the Status Word received from the receiving RT.
8	SW2ERR	Status Word 2 Error: In an RT-RT sequence. the transmitting RT Status Word has the wrong RT address.
7	FFERR	Data FIFO Error: Data was not available in the transmit Data FIFO in time to allow transmission.
6	-	Not used. This bit is set to "0".
5	CONERR	Contiguous Message Error: Transmission was not contiguous.
4	GAPERR	Bus activity was detected in the 4.0 uS gap after a valid message was completed.
3	CSYCERR	Command Sync Error: Expected Data Sync, but got Command Sync.
2	DSYCERR	Data Sync Error: Expected Command Sync, but got Data Sync.
1	MANERR	Manchester Encoding Error: The decoder detected an error in Manchester encoding, bit count or parity.
0	NORCV	This bit is set when a data word is expected while processing a receive command, but a gap is detected. It is also set when an RT-to-RT "No Response Timeout" occurs, as defined per MIL-HDBK-1553, Figure 8 "RT-RT Timeout Measurement". The HI-6110 asserts this error when the bus dead-time between the RT-RT command pair and the transmit RT Status Word exceeds 15 uS when Control Register bit 14 = "0" or 129uS when Control Register bit 14 = "1".

ISSUING BC COMMANDS

Register operations in the HI-6110 can be addressed using either the RA0-RA3 inputs or the RA3:RA0 bits in the Control Register. Each RA input is logically ORed with its corresponding Control Register bit. When using input pins for register addressing, the Control Register bits 10:7 must be reset. Register addressing via Control Register bits 10:7 is a 2-step process. First, the target register address is written to the Control Register (and the RA0-RA3 inputs must be held low). Next, the desired register operation is performed: the Control Register provides the register address while the R/$\overline{W}$ and $\overline{STB}$ inputs specify data direction and clock the data transfer.

A MIL-STD-1553 Bus Controller message can be pre-loaded into the HI-6110 by writing the required Command Word to the Command Word 1 Register. The Command Word 2 register is used to hold the second (Transmit) Command Word for RT to RT commands. Message data for MIL-STD-1553 Receive commands are loaded by the host into the Transmit Data FIFO. For Mode Code commands with data word, a data word to be transmitted must be written to the Transmit Data FIFO.

A BC message sequence commences when a positive edge occurs at the BCSTART input pin, or when Control Register bit 1 (BCSTART) transitions from 0 to 1 as a result of a register write operation by the Host. Control Register bit 1 is NOT automatically reset upon BC message sequence execution. Therefore, when using the Control Register to start message sequences, it is first necessary to reset bit 1 before it is set to initiate the next message sequence. The MIL-STD-1553 message is properly formatted by the HI-6110 and output on the selected MIL-STD-1553 data bus.

The HI-6110 waits for a response from the MIL-STD-1553 bus if the command type expects a response. The responding RT's Status Word is captured in the HI-6110 Status Word 1 Register. The Status Word 2 register is used to capture the Status Word from the transmitting RT during RT-to-RT transfer commands. Message data words received from the transmitting RT are stored in the Receive Data FIFO. A mode data word received from the transmitting RT is also stored in the Receive Data FIFO.

If the reply from the MIL-STD-1553 responding terminal was a valid response and met all response time, Sync and Data encoding, parity checks, word count, RT address, and contiguous message requirements, then the VALMESS output pin goes high and bit 7 in the Status Register is set. The host may then retrieve the contents of the Status Word register(s) and Receive Data FIFO as required by the application software. The FFEMPTY output pin will be low if the FIFO contains at least one data word, and the corresponding bit 3 in the Status Register will be set. When all data words have been read by the host controller, the FFEMPTY output pin goes high, and bit 3 in the Status Register is reset.

The final result of any BC message sequence is assertion of either a VALMESS flag or an ERROR flag. If an error is detected during a MIL-STD-1553 message sequence, the ERROR output pin is asserted, corresponding bit 8 in the Status Register is set, and the appropriate error bit(s) are set in the Error Register. The host may interrogate the Error Register to determine what action is necessary to correct the error. The VALMESS output remains low for any message for which an error is detected.

There are limited circumstances when VALMESS may be followed by ERROR. For example, if the BC requests an RT response with 4 data words but instead receives 5, the extra data word will cause the VALMESS flag to be reset and ERROR to be set. The host controller has the option of reading RT responses on-the-fly by monitoring the $\overline{RFLAG}$ and FFEMPTY flags, or may simply wait for end of sequence flags, VALMESS or ERROR.

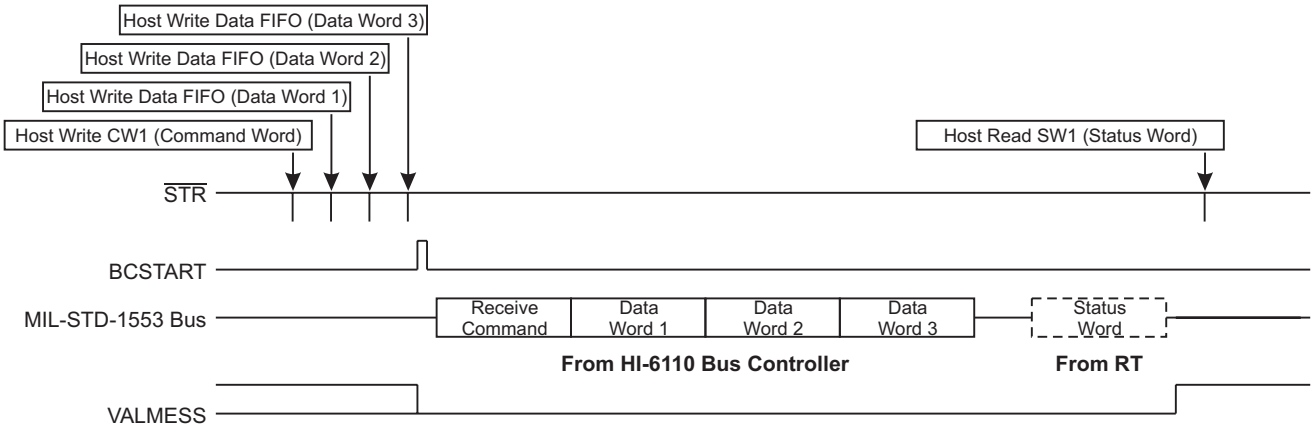
While the Transmit Data FIFO may be pre-loaded before starting a message sequence, any data word may be loaded on the fly, as long as it is written before mid-sync during that word's transmit window. In order to have the full 32 word capacity available, the Transmit Data FIFO should be cleared before writing data. The FIFO is cleared at Master Reset, or when VALMESS or ERROR is asserted at the end of a message.

The Receive Data FIFO is cleared at Master Reset, or by performing a series of FIFO read operations until FFEMPTY goes high. The Receive Data FIFO will not accept new receive data when full. The FIFO must have at least one empty register by mid-sync within the time window for any incoming data word.

EXAMPLE BC MIL-STD-1553 MESSAGE SEQUENCES

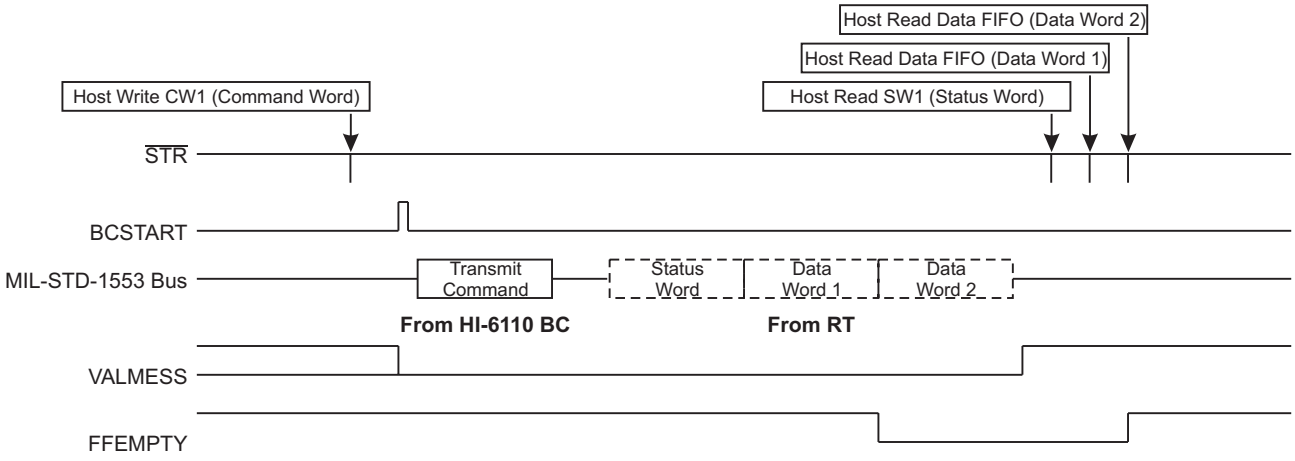
Example 1. BC TO RT Transfer (BCRT message)

The HI-6110 Bus Controller issues a Receive Command with 3 data words to a Remote Terminal on the bus. The correct Status Word is received.



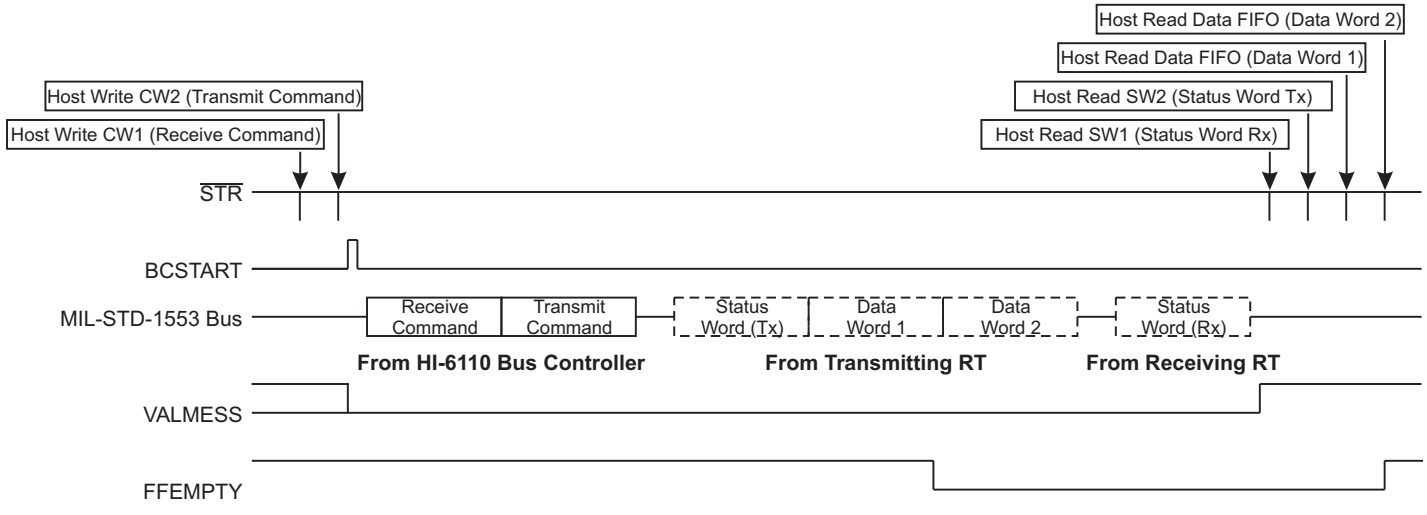
Example 2. RT TO BC Transfer (RTBC message)

The HI-6110 Bus Controller issues a Transmit Command requiring a 2 data word response to a Remote Terminal on the bus. The correct Status Word and 2 Data Words are received and read by the host.



Example 3. RT to RT Transfer (RTRT message)

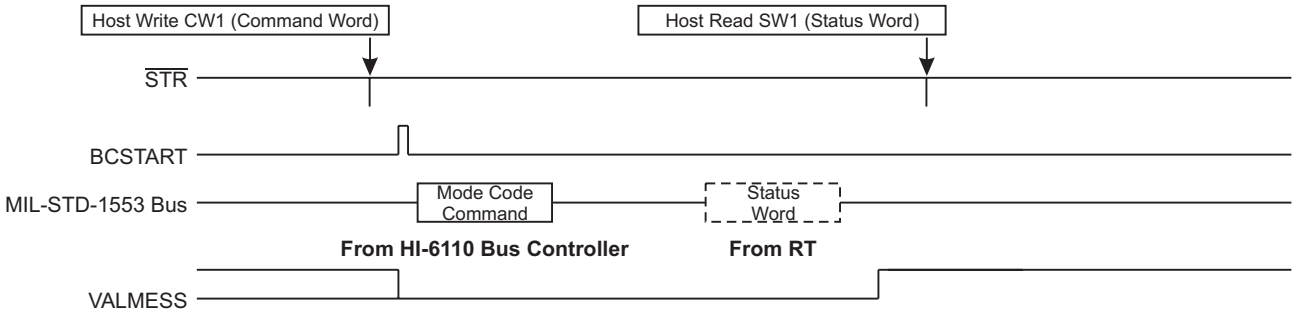
The HI-6110 Bus Controller issues an RT to RT transfer with 2 data words to two Remote Terminal on the bus. The RTs execute the command and the Bus Controller validates the RT responses. Note that the data transferred is captured by the HI-6110 Bus Controller and may be read by the host.



EXAMPLE BC MIL-STD-1553 MESSAGE SEQUENCES

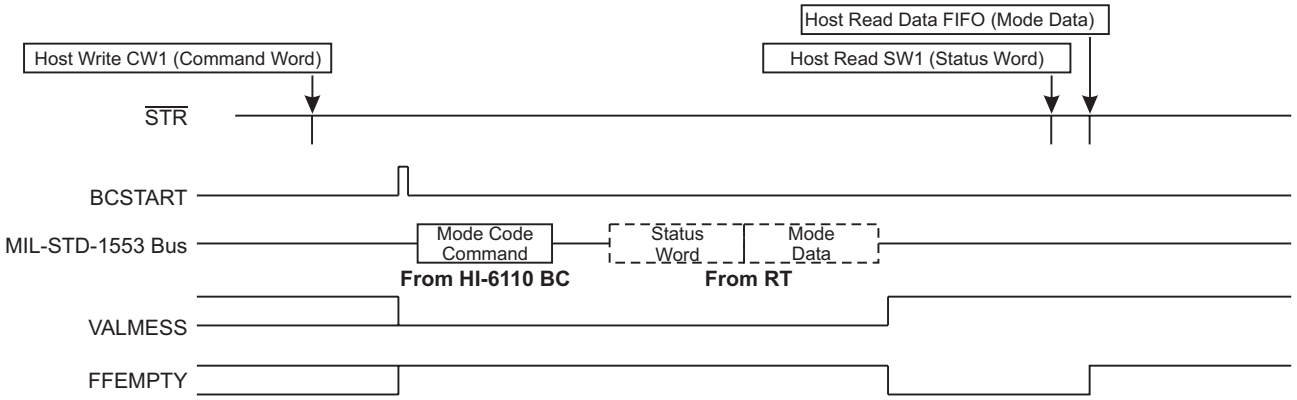
Example 4. Mode Code Command without Data Word

The HI-6110 Bus Controller issues a Mode Code Command to a Remote Terminal on the bus. The correct Status Word is received.



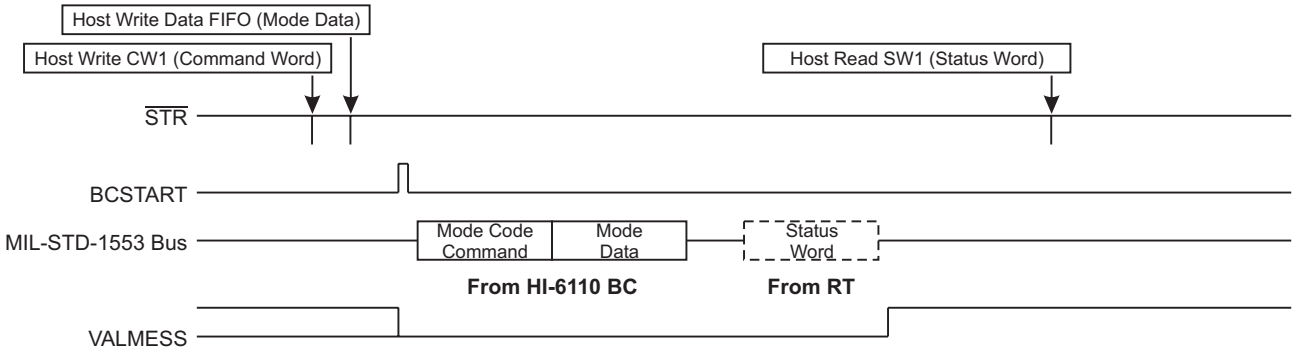
Example 5. Mode Code with Data Word (Transmit)

The HI-6110 Bus Controller issues a Mode Command with Data Word (Transmit) to a Remote Terminal. The Status Word and mode data word are received; the data word is stored in the Receive FIFO. Status Word and mode data are read by the host.



Example 6. Mode Code with Data Word (Receive)

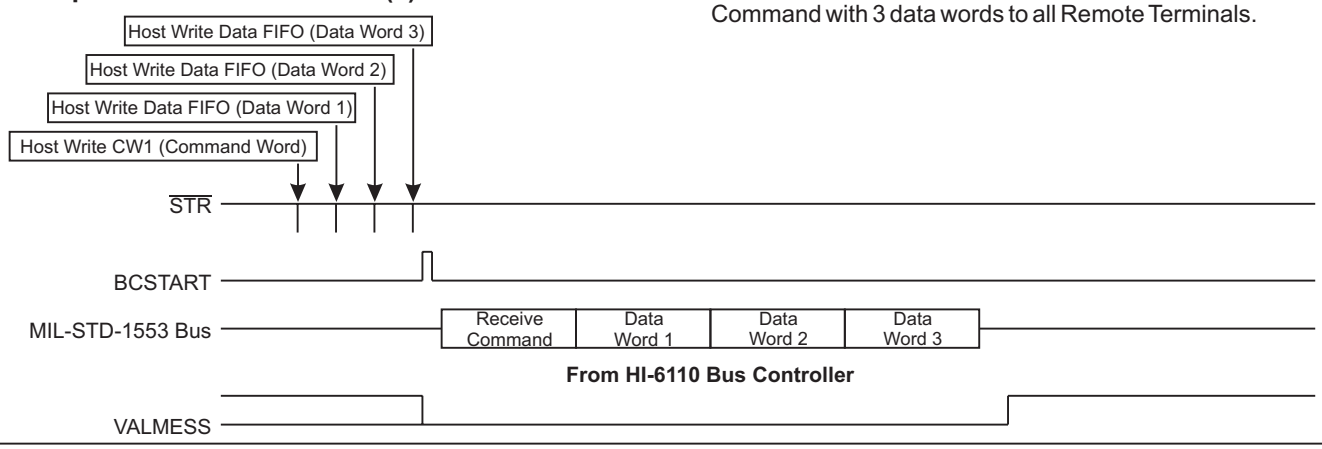
The HI-6110 Bus Controller issues a Mode Command with Data word (Receive) to a Remote Terminal on the bus. The correct Status Word is returned and read by the host.



EXAMPLE BC MIL-STD-1553 MESSAGE SEQUENCES

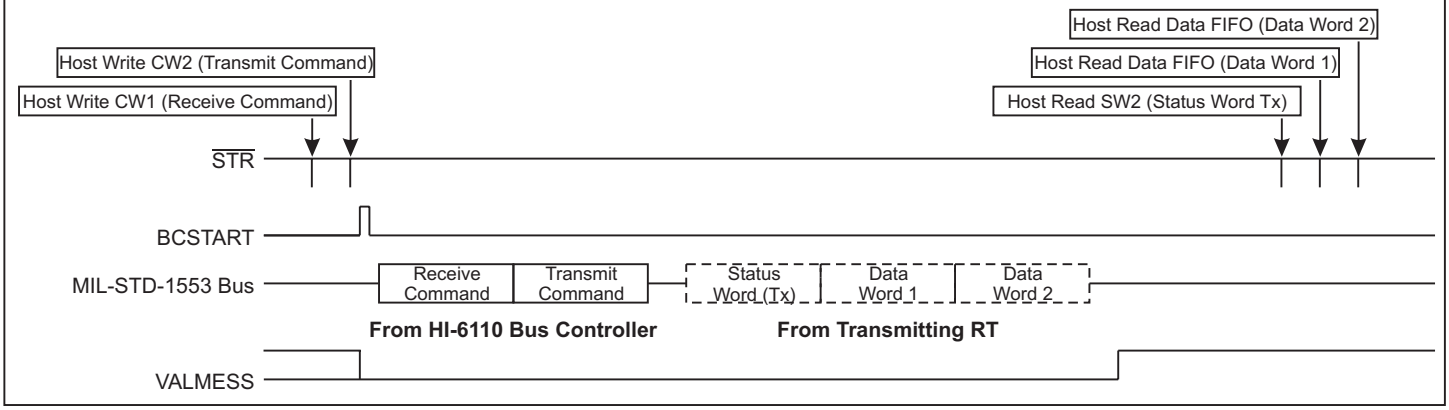
Example 7. Broadcast BC to RT(s) Transfer

The HI-6110 Bus Controller issues a Broadcast Receive Command with 3 data words to all Remote Terminals.



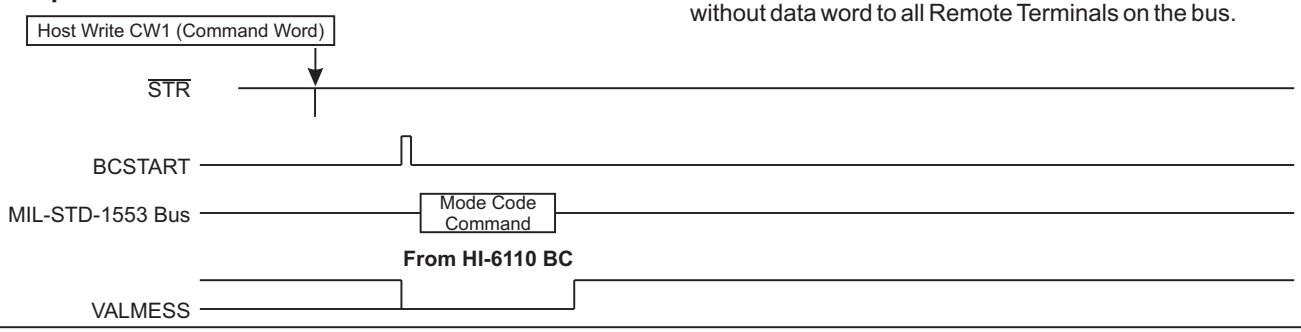
Example 8. Broadcast RT to RT(s) Transfer

The HI-6110 Bus Controller issues a Broadcast RT to RT transfer Command with 2 data words to a Remote Terminal on the bus. The RT broadcasts the message and the Bus Controller validates the RT response. The transmitted data words are captured by the HI-6110 Bus Controller and may be read by the host controller.



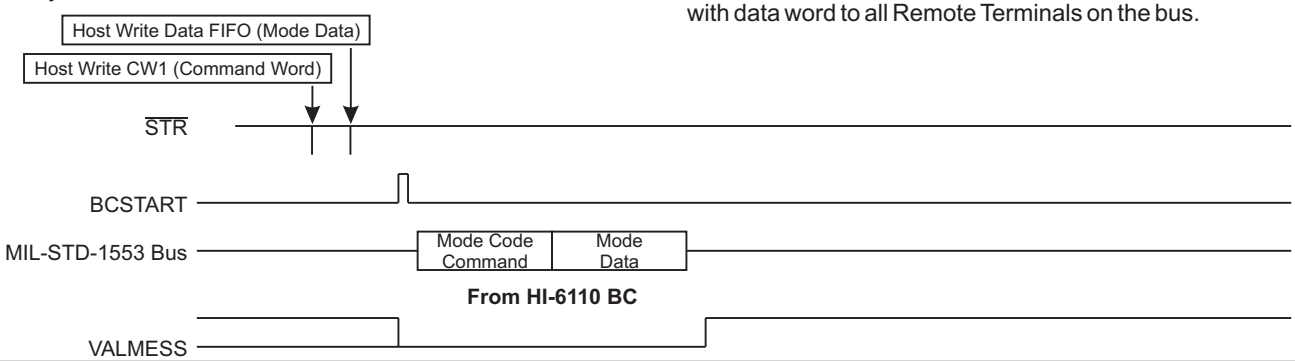
Example 9. Broadcast Mode Code without Data Word

The HI-6110 Bus Controller issues a Broadcast Mode Command without data word to all Remote Terminals on the bus.



Example 10. Broadcast Mode Code with Data Word

The HI-6110 Bus Controller issues a Broadcast Mode Command with data word to all Remote Terminals on the bus.



REMOTE TERMINAL

The HI-6110 is configured for Remote Terminal operation by setting the BCMODE input low and the RTMODE input high. An alternative is programming Control Register bit 2 (BCMODE) to a "0" and programming Control Register bit 3 (RTMODE) to a "1". These Control Register bits are logically ORed with their corresponding input pins.

Figure 2. shows a block diagram of the HI-6110 in Remote Terminal mode.

INITIALIZATION

In Remote Terminal mode, the host controller first performs a Master Reset to initialize the RT protocol engine and clear all message registers and data FIFOs. This may be achieved by pulsing the MR input high, or writing a "1" and then a "0" to Control Register bit 0. The user must select a master clock (CLK) frequency by programming Control Register bits 11 and 12. Refer to the RT Register Formats section for a full description of available registers and their functions in Remote Terminal Mode.

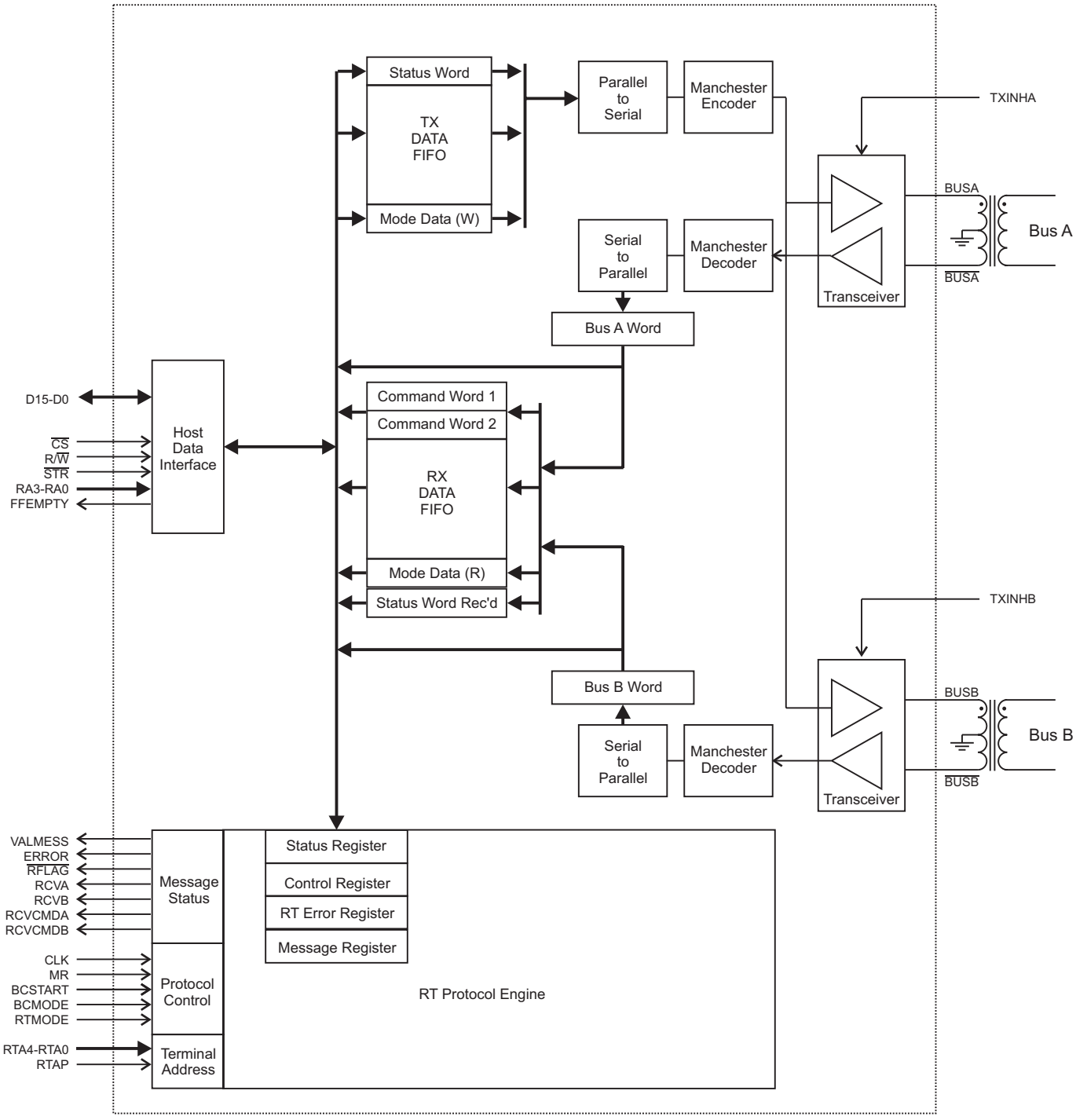
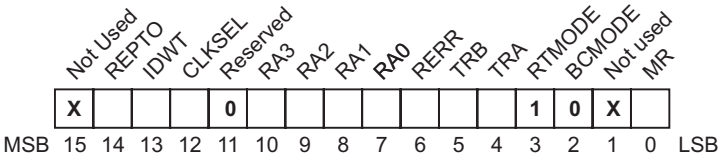


Figure 2. Block Diagram - Remote Terminal Mode

REGISTER FORMATS (RT Mode)

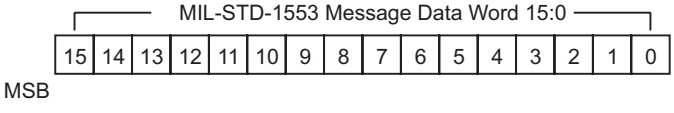
CONTROL REGISTER (R/W) Write Address: X1XX, Read Address: 1100



The Control Register value specifies HI-6110 operating mode, clock frequency and the bus enabled for transmit. It can also be used to address registers for read/write operations, assert master reset, as well as data word suppression when illegal command detection is implemented .

BIT	NAME	FUNCTION
15	-	Not used.
14	REPTO	Controls the time-out which causes the No Response Error. 0 — 17 usec Gap (equivalent to the 57 usec measurement of 5.2.1.7 of the RT Validation Test Plan) 1 — 131 usec Gap
13	IDWT	Inhibit Data Word Transmission. When “illegal command detection” is required, this feature alows “command illegalization”. When the IDWT bit is set, normal transmission of ordinary and mode data words is suppressed for all transmit commands. NOTE: There will be no VALMESS or ERROR assertion for the affected message. For normal response to the next command, this bit must be reset before that command’s Status Word bit 0 is transmitted.
12	CLKSEL	Selects the frequency of the HI-6110 external CLK input: CLKSEL — Value 0 — 24 MHz 1 — 12 MHz
11	Reserved	This bit must be reset to “0”
10 - 7	RA3:0	Register Address for HI-6110 register and data read / write operations. The register address is defined by the logical OR of these bits and their corresponding input pins. Setting Control Register bits 10:7 to 0000 ensures that only the input pins are used for addressing registers.
6	RERR	Reset ERROR. If RERR is low, the ERROR output pin can only be reset by asserting MR, master reset. Writing RERR high causes the ERROR output to be reset (rising edge). If the RERR is left high, the ERROR output will automatically reset after 3 to 4 microseconds. For normal operation, this bit is set to “1”.
5 - 4	TRB, TRA	Setting either TRA or TRB to "1" enables transmission on MIL-STD-1553 BUS A or BUS B. Setting both TRA and TRB selects neither bus. The RT protocol engine connects to the selected, active bus. The 1553 receiver, Manchester decoder and RCV output signal are still operational on the inactive bus. This is useful when the remote terminal receives a command on the inactive bus, indicated by RCV signal output. The RT must switch active buses to service the command. Valid words received on the inactive bus can be read without changing active bus by reading the Bus A Word or Bus B Word register, but the terminal cannot respond as transmit is disabled. NOTE: the TXINHA and TXINHB input pins can override bus enablement.
3 - 2	RTMODE, BCMODE	HI-6110 mode select. These Control Register bits are logically OR'ed with their corresponding input pins, allowing the user to select 1553 operating mode under either hardware or software control: RTMODE — BCMODE — 1553 OPERATING MODE 0 — 0 — Bus Monitor (MT), with assigned RT address 0 — 1 — Bus Controller (BC) 1 — 0 — Remote Terminal (RT) 1 — 1 — Bus Monitor (MT), without assigned RT address
1	-	Not used in RT mode.
!0	MR	Master Reset. Writing "1" and then “0” to this bit performs the same function as pulsing the MR pin. All register and data FIFOs are cleared when master reset is asserted. The Control Register is the exception; it is not affected by Master Reset.

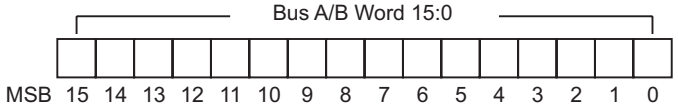
TRANSMIT DATA FIFO (Write only) Write Address: X011
RESET TRANSMIT DATA FIFO Write Address: X010



The Transmit Data FIFO is 32-words deep and holds MIL-STD-1553 message data. The FIFO is cleared on Master Reset or by any write to register address X010.

Any data word to be transmitted by the RT must be loaded into the TRANSMIT DATA FIFO before the mid-parity bit for the preceding MIL-STD-1553 word. Words are transmitted in the order they are loaded.

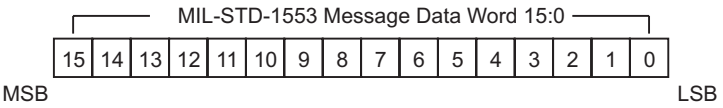
BUS A WORD REGISTER (Read only) Read Address: 1001
BUS B WORD REGISTER (Read only) Read Address: 1010



In RT mode, the Bus A Word register holds the last valid MIL-STD-1553 word received on Bus A. The Bus B Word register holds the last valid MIL-STD-1553 word received on Bus B.

RT OPERATION

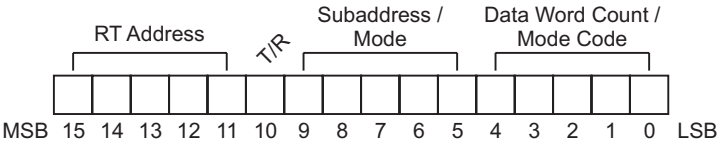
RECEIVE DATA FIFO (Read only) Read Address: 0100



The Receive Data FIFO is 32-words deep and holds MIL-STD-1553 data words received by the RT. The FIFO is cleared on Master Reset or after all words have been read by the host.

A low FFEMPTY flag (pin or Status register) means FIFO data is available to be read by the host. Successive data reads cause FFEMPTY to go high when the last data word is read.

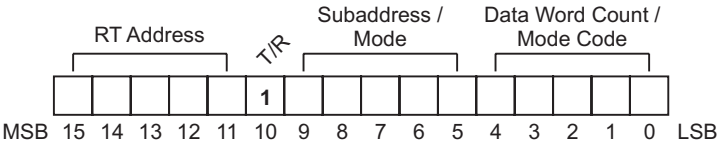
COMMAND WORD 1 REGISTER (Read only) Read Address: 0000



For all commands except RT to RT, the Command Word 1 register contains the last valid Command Word received.

If the last valid command received was RT to RT, the Command Word 1 register holds the first (receive) command word and the Command Word 2 Register holds the second (transmit) command word. Then if Message Register bits 3 and 9 are both 0, the Command Word 1 register contains the valid command.

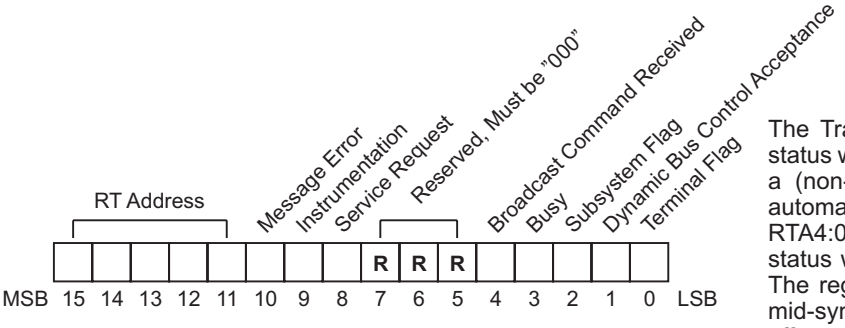
COMMAND WORD 2 REGISTER (Read only) Read Address: 0001



If the last valid command received was RT to RT, the Command Word 2 register contains the second (transmit) command word. (See note above for Command Word 1.) Whenever Message Register bit 3 or bit 9 is set, the valid command is contained in the Command Word 2 register.

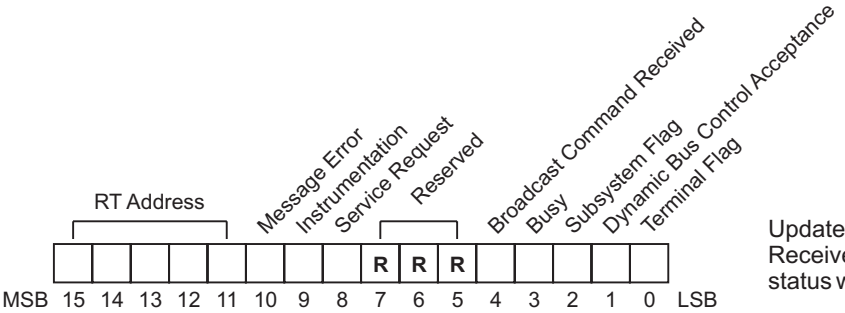
Whenever RCV is asserted, the active Command Word register can always be determined by checking Message Register bits 3 and 9.

TRANSMIT STATUS WORD REGISTER (Write only) Write Address: X000



The Transmit Status Word register holds bits 10:0 for the status word transmitted by the remote terminal in response to a (non-broadcast) command. Status word bits 15:11 are automatically set to match the RT Address present at the RTA4:0 input pins. The HI-6110 automatically transmits a status word in response to valid non-broadcast commands. The register may be changed anytime prior to status word mid-sync bit. The Transmit Status Word register is not affected by MR, master reset.

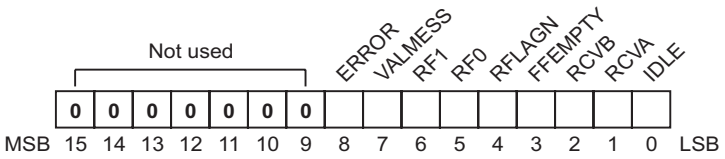
RECEIVED STATUS WORD REGISTER (Read only) Read Address: 0011



Updated only during RT to RT transmit messages, the Received Status Word register captures the MIL-STD-1553 status word transmitted by the receiving remote terminal.

RT OPERATION

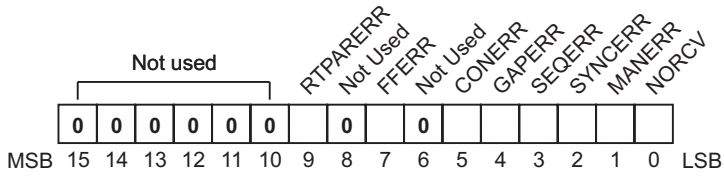
STATUS REGISTER (Read only) Read Address: 0101



The Status Register may be interrogated by the host at any time. It provides information that allows the user to determine whether the HI-6110 is busy executing a MIL-STD-1553 message and its progress. After a message sequence has completed, the Status register indicates whether an error was detected or if the message sequence was successful.

BIT	NAME	FUNCTION
15- 9	-	Not used. These bits are set to "0".
8	ERROR	This bit is reset to "0" after MR, and will automatically reset 2 to 3 uS after assertion if Control register RERR bit is set. ERROR is set to a "1" if the last sequence had an error. The nature of the message error can be determined by examining the Error Register. The ERROR output pin reflects the state of this bit.
7	VALMESS	This bit is a "0" after reset or after a MIL-STD-1553 message containing an error. VALMESS goes high upon completion of an error-free MIL-STD-1553 message sequence. VALMESS is reset to a zero each time a valid command is received on the active bus. The VALMESS output pin mirrors the state of this bit.
6	RF1	This bit goes high when a valid Receive Command arrives on Bus B. It is reset by the RCV B flag.
5	RF0	This bit goes high when a valid Receive Command arrives on Bus A. It is reset by the RCV A flag.
4	RFLAGN	During a message sequence this bit goes low at the arrival of a Command Word, Status Word, or Mode Data Word. For consecutive words, this bit will momentarily go high between words. The $\overline{\text{RFLAG}}$ output reflects the state of this bit.
3	FFEMPTY	If "0", the receive Data FIFO contains at least one unread data word. This bit is set to "1" upon master reset, or when the user has read all available received data words from the receiver Data FIFO. The FFEMPTY output pin reflects the state of this bit.
2	RCVB	Set to "1" upon receipt of a valid Command Word on Bus B except for RT-to-RT receive commands when it is set after the second Command Word is received. The RCVB output pin mirrors the state of this bit.
1	RCVA	Set to "1" upon receipt of a valid Command Word on Bus A except for RT-toRT receive commands when it is set after the second Command Word is received. The RCVA output pin mirrors the state of this bit.
0	IDLE	If "1", the RT is idle. This bit is “0” throughout the time the RT is processing a valid MIL-STD-1553 Command message. The bit returns to a "1" when the message is completed.

ERROR REGISTER (Read only) Read Address: 0111

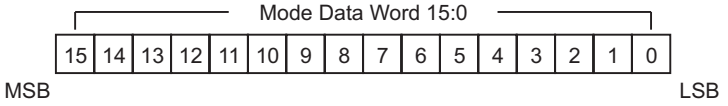


The RT Error Register is cleared at Master Reset and error flags are automatically reset if Control Register bit 6 = “1”. If an error is encountered during message execution, the ERROR pin goes high, the ERROR bit is set in the Status Register, and one or more bits are set in the Error Register to specify the type of error detected.

BIT	NAME	FUNCTION
15 - 10	-	Not used. These bits are set to "0".
9	RTPARERR	RT Parity Error in the pin-programmed RT address. RT address parity is checked only at Master Reset, and once this bit is set, the host controller must perform a subsequent Master Reset to update parity status.
8	-	Not used. This bit is set to "0".
7	FFERR	Data was not available in the Transmit Data FIFO.
6	-	Not used. This bit is set to "0".
5	CONERR	Contiguous Message Error: Transmission was not contiguous.
4	GAPERR	Bus activity was detected in the 4.0 uS gap after a valid message was completed.
3	SEQERR	The next event after a Command Word was erroneous. For example, a gap following a valid receive Command Word, or a contiguous Data Word following a transmit Command Word.
2	SYNCERR	Sync Error: Expected Command Sync and got Data Sync, or vice versa.
1	MANERR	Manchester Encoding Error: The decoder detected an error in Manchester encoding, bit count or parity.
0	NORCV	This bit is set when a data word is expected while processing a receive command, but a gap is detected. It is also set when an RT-to-RT "No Response Timeout" occurs, as defined per MIL-HDBK-1553, Figure 8 "RT-RT Timeout Measurement". The HI-6110 asserts this error when the bus dead-time between the RT-RT command pair and the transmit RT Status Word exceeds 15 uS.

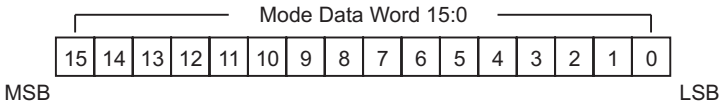
RT OPERATION

TRANSMIT MODE DATA WORD REGISTER (Write only) Write Address: X001



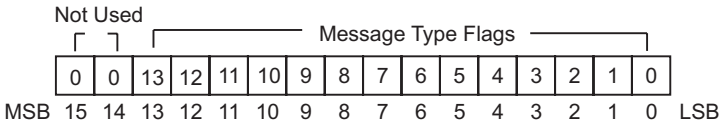
The write-only Transmit Mode Data Word register is loaded by the host with the Mode Data word to be transmitted by the remote terminal in response to a mode code with mode data word (transmit) command. The Transmit Mode Data Word register is not affected by MR, master reset.

RECEIVE MODE DATA WORD REGISTER (Read only) Read Address: 0010



The read-only Receive Mode Data Word register holds the value of the last mode data word received during a mode code with data word (receive) command addressed to this RT. This register is reset only by MR master reset.

MESSAGE REGISTER (Read only) Read Address: 0110



The Message Register identifies command type when a new valid command is received from the MIL-STD-1553 bus controller. When a valid command is received, message type is decoded and appropriate Message Register bit(s) are set. Two bit pairs are mirrored: Bit pair 3 and 12, Bit pair 5 and 13.

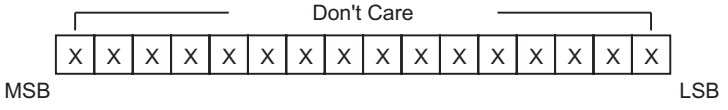
In the table below, "RTA" indicates assigned Remote Terminal address. Broadcast command occurs when address = 11111. Bit 10 is set for mode code or non-RT-RT transmit commands where bits 15:11 equal RTA or 11111. Bit 10 enables detection and "illegalization" for three undefined mode code command types listed in the table below.

Hex	Last Valid Command Decoded	Command Word 1 Bit Fields				Command Word 2 Bit Fields			
	NON-MODE COMMANDS	15:11	10	9:5	4:0	15:11	10	9:5	4:0
0001	Receive command from BC, not broadcast	RTA	0	00001-11110	XXXXX				
0080	Receive command from BC, broadcast	11111	0	00001-11110	XXXXX				
0004	Receive command, RT-RT, not broadcast	RTA	0	00001-11110	XXXXX	XXXXX	1	00001-11110	XXXXX
0100	Receive command, RT-RT, broadcast	11111	0	00001-11110	XXXXX	not RTA	1	00001-11110	XXXXX
0402	Transmit command, RT to BC	RTA	1	00001-11110	XXXXX				
1008	Transmit command, RT-RT, not broadcast	not 11111	0	00001-11110	XXXXX	RTA	1	00001-11110	XXXXX
0200	Transmit command, RT-RT, broadcast	11111	0	00001-11110	XXXXX	RTA	1	00001-11110	XXXXX
	MODE CODE COMMANDS								
0410	MC0 - MC15 T/R=1 no mode data, not broadcast	RTA	1	0000 or 11111	0XXXX				
0400 *	MC0 - MC15 T/R=1 no mode data, broadcast	11111	1	0000 or 11111	0XXXX				
0410	MC0 - MC15 T/R=0 not broadcast, UNDEFINED	RTA	0	0000 or 11111	0XXXX				
0400	MC0 - MC15 T/R=0 broadcast, UNDEFINED	11111	0	0000 or 11111	0XXXX				
2420	MC16 - MC31 T/R=1 mode data, not broadcast	RTA	1	0000 or 11111	1XXXX				
0400 *	MC16 - MC31 T/R=1 broadcast, UNDEFINED	11111	1	0000 or 11111	1XXXX				
0040	MC16 - MC31 T/R=0 mode data, not broadcast	RTA	0	0000 or 11111	1XXXX				
0800	MC16 - MC31 T/R=0 mode data, broadcast	11111	0	0000 or 11111	1XXXX				

Command Word 2 only applies for RT-RT commands

* Two cases where 0400 is reset 550nS after RCV

RESET TRANSMIT DATA FIFO (Write Only) Write Address: X010



Performing a host write cycle to register address X010 causes the Transmit Data FIFO to be cleared. New data may be loaded into the FIFO by writing to register address X011 as described above.

Note that no data is stored when performing a write cycle to register address X010 and the actual data presented on the databus is not used (don't care).

REMOTE TERMINAL OPERATION

The HI-6110 remote terminal (RT) address is set by wiring the RTA4:RTA0 input pins to the desired address. RTA0 is the least significant address input. The RTAP input must be set/reset to reflect odd parity for the RA4:0 address inputs. Upon Master Reset, the HI-6110 reads the RT address inputs and checks for correct parity. If a parity error is detected, the PARERR bit is set in the Error Register and the HI-6110 RT will not respond to MIL-STD-1553 Command Words. The host controller must correct the RT address-parity mismatch, then reassert Master Reset to enable bus operations.

When configured as a Remote Terminal, the HI-6110 continuously monitors both MIL-STD-1553 buses. Each received Command Word is checked for validity. The RCVA and RCVB outputs are asserted only when a received command is valid. Valid is defined as having an RT address matching the pin-programmed RT address or the command is a broadcast command. If a valid command is received on Bus A, the RCVA signal goes high to notify the host. Similarly, when a valid command arrives on Bus B, the RCVB signal goes high.

The received command may be read from the appropriate Command Word register, or the Message register may be read to quickly determine the type of response needed. The RT protocol sequencer will initiate a response in accordance with the requirements of MIL-STD-1553. If the message type requires a Status Word response and the bus TR bit is set in the Control Register, the HI-6110 RT will automatically transmit its Status Word approxinmately 7 to 9 5uS after RCVA or RCVB goes high. The Status Word register can be modified up to 1.3 uS past mid-sync, occurring when the Status Word is transmitted.

If transmit data words are part of the command response, the automatic response delay provides time for the host to load the Transmit Data FIFO. The first data word must be written to the FIFO not later than 20 uS after Status Word mid-sync. All data words must be written before mid-sync occurring within its transmission window. All data words may be written in rapid succession once RCVA or RCVB goes high.

Upon error-free completion of the message, VALMESS goes high. (One exception: broadcast mode code commands without mode data word do not generate VALMESS.) If an error is detected, VALMESS remains low and the ERROR signal goes high. The ERROR register can be read to determine error type.

In applications requiring illegal command detection, the HI-6110 readily handles command “illegalization”. Upon detecting an illegal command, the host microcontroller takes steps to (a) send the Remote Terminal Status Word with the Message Error (ME) bit set (non-broadcast commands only), and (b) suppress transmission of any data words associated with the normal response to the command. For part (a), the Status Word register is modified by setting the ME bit. This is done first to make sure the change is effective before Status Word transmission begins. For part (b), bit 13 in the Control Register is set to suppress data word transmission.

NOTE: Once bit 13 is set in the Control register, the affected message will NOT conclude with VALMESS or ERROR assertion. Control Register bit 13 should be written to a zero before the next message is processed. The host might perform the Control Register write as part of the RCV flag service routine in order to restore normal operation for legal commands.

The Receive Data FIFO is cleared at Master Reset, or by performing a series of FIFO read operations until FFEMPTY goes high. The Receive Data FIFO will not accept new receive data when full.

When the Control Register is written to change the active bus, the HI-6110 automatically resets any message in process on the former bus and begins a new message sequence on the new bus. To comply with RT response time limits, it is typically necessary to write the Control Register within 2 uS of the rising edge of the RCV flag on the alternate bus. Note that when the active bus is switched, the RT message sequencer retrieves and responds to the last valid command word received on the previously inactive bus. This applies regardless of when the command word was received. For this reason, bus switching should only occur in response to a current RCV or RCVCMD signal or otherwise be followed by a master reset.

The HI-6110 readily handles superseding commands. For superseding commands on the same bus as described in 5.2.1.4 of the RT Validation test, the 6110 will generate a new RCV flag upon receiving a valid command after a 4 uS gap. The message sequencer is automatically reset and the new sequence initiated.

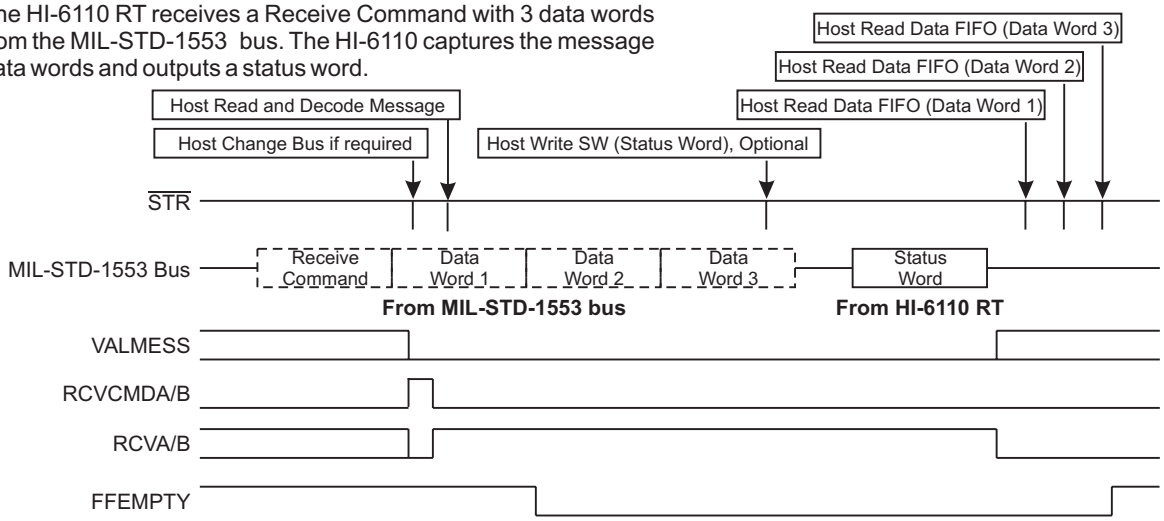
RT validation section 5.2.1.8 “Bus Switching” tests a condition otherwise prohibited by the 1553 standard: overlapping valid commands on the two buses. To meet the requirements of this test, certain steps are required: (a) When switching buses for the superseding command, reset Control Register TRA and TRB bits for 200 nS minimum before setting the TRx bit for the newly active bus. This resets transmission for an in-process command response. To simplify the software, the example software does this for all bus switching. (b) The RT should always respond to the command occurring last. A potential problem occurs when an RT-RT receive command is interrupted by a valid command on the other bus. Although CW1 is valid for the remote terminal, RCV for all RT-RT commands occurs after CW1 and CW2 are both received. When a valid command that overlaps CW1 occurs on the other bus, its RCV will go high before the RT-RT RCV. The overlapping command occurs later, although its RCV precedes the RT-RT RCV. The RT-RT RCV must be ignored. To correctly respond to the overlapping command, the software must utilize the RCVCMDA and RCVCMDB signals as described below. Please refer to the software example in the reference design for a working implementation.

The RCVCMDA output goes high when a valid non-mode receive command is decoded on Bus A. The RCVCMDB signal performs the same function for Bus B. Successful compliance with RT validation 5.2.1.8 “Bus Switching” requires host interaction when RCVCMD is asserted for the inactive bus. When this occurs, the host should immediately make that bus active. If an ordinary receive command is coming from the Bus Controller, RCV for the newly-active bus will go high about 4 uS after RCVCMD. If an RT-RT receive command, RCV follows RCVCMD by 20 uS. In either case once RCV is asserted, the RT can begin polling FFEMPTY to acquire received data words as they arrive.

EXAMPLE RT MIL-STD-1553 MESSAGE SEQUENCES

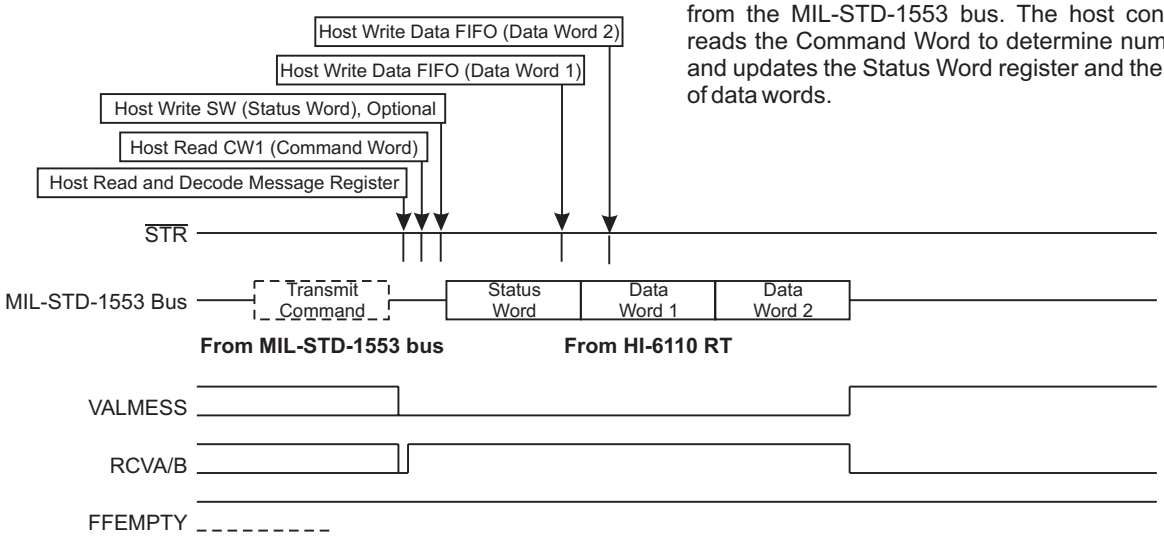
Example 1. BC TO RT Transfer

The HI-6110 RT receives a Receive Command with 3 data words from the MIL-STD-1553 bus. The HI-6110 captures the message data words and outputs a status word.



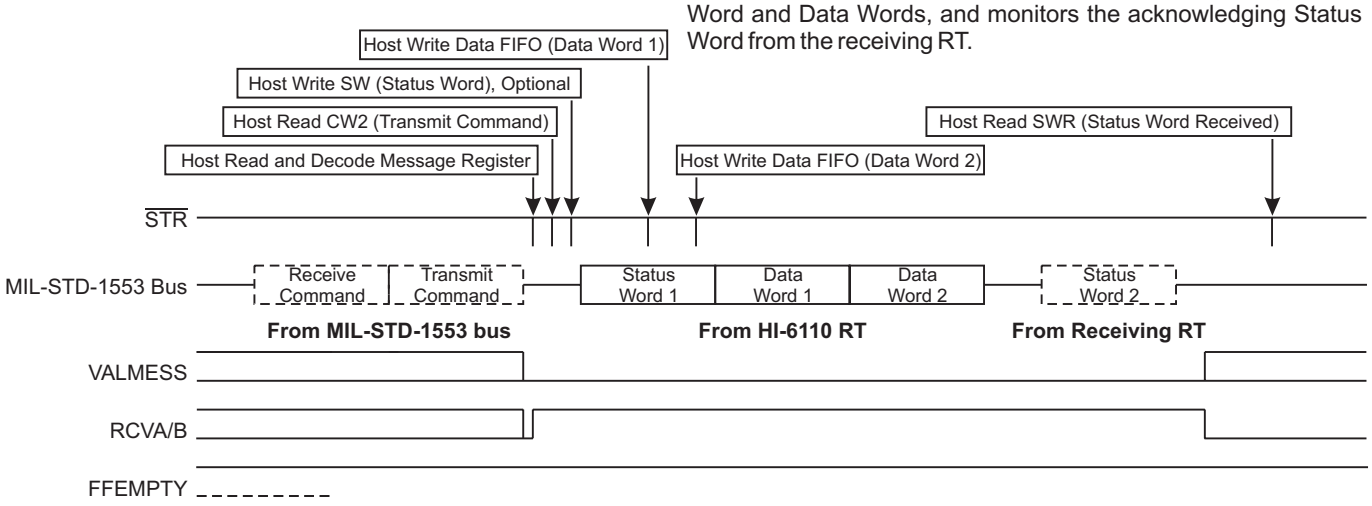
Example 2. RT TO BC Transfer

The HI-6110 RT receives a Transmit Command with 2 data words from the MIL-STD-1553 bus. The host controller HI-6110 RT reads the Command Word to determine number of data words, and updates the Status Word register and the requested number of data words.



Example 3. RT to RT Transfer, HI-6110 is the transmitting RT

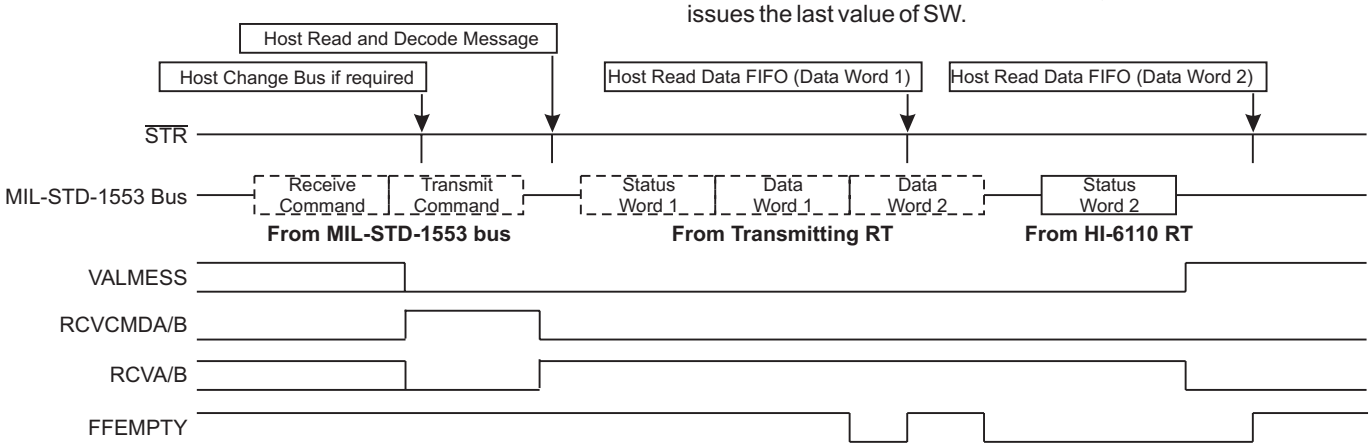
The HI-6110 RT receives an RT to RT transfer with 2 data words command from the MIL-STD-1553 bus. In this case, the HI-6110 is the transmitting RT. The HI-6110 issues the necessary Status Word and Data Words, and monitors the acknowledging Status Word from the receiving RT.



EXAMPLE RT MIL-STD-1553 MESSAGE SEQUENCES

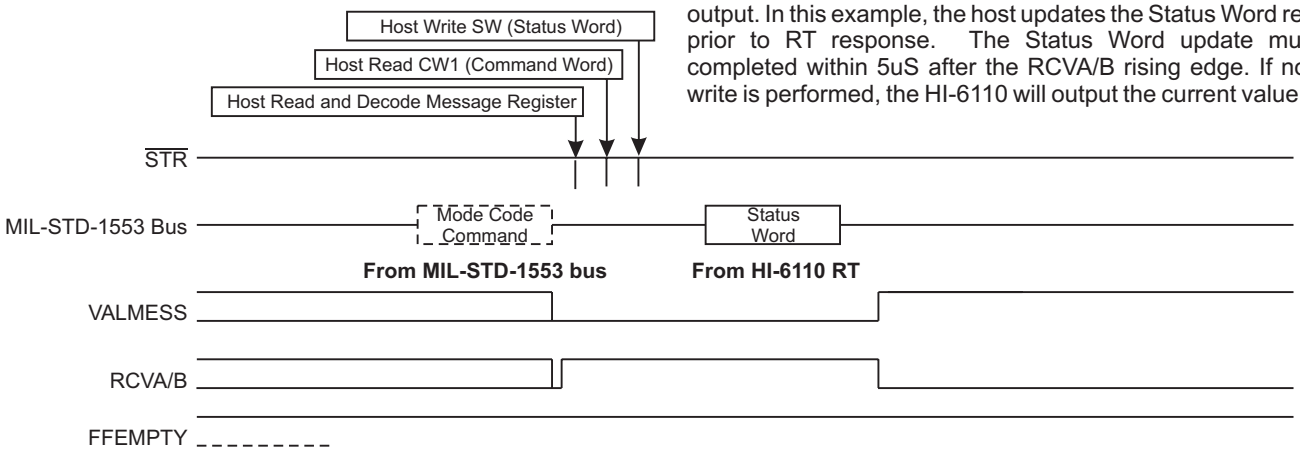
Example 4. RT to RT Transfer, HI-6110 is the receiving RT

The HI-6110 RT receives an RT to RT transfer with 2 data words command from the MIL-STD-1553 bus. In this case, the HI-6110 is the receiving RT. The HI-6110 captures the message data and issues the necessary Status Word. In this particular example, the host did not update the Status Word Register and the HI-6110 re-issues the last value of SW.



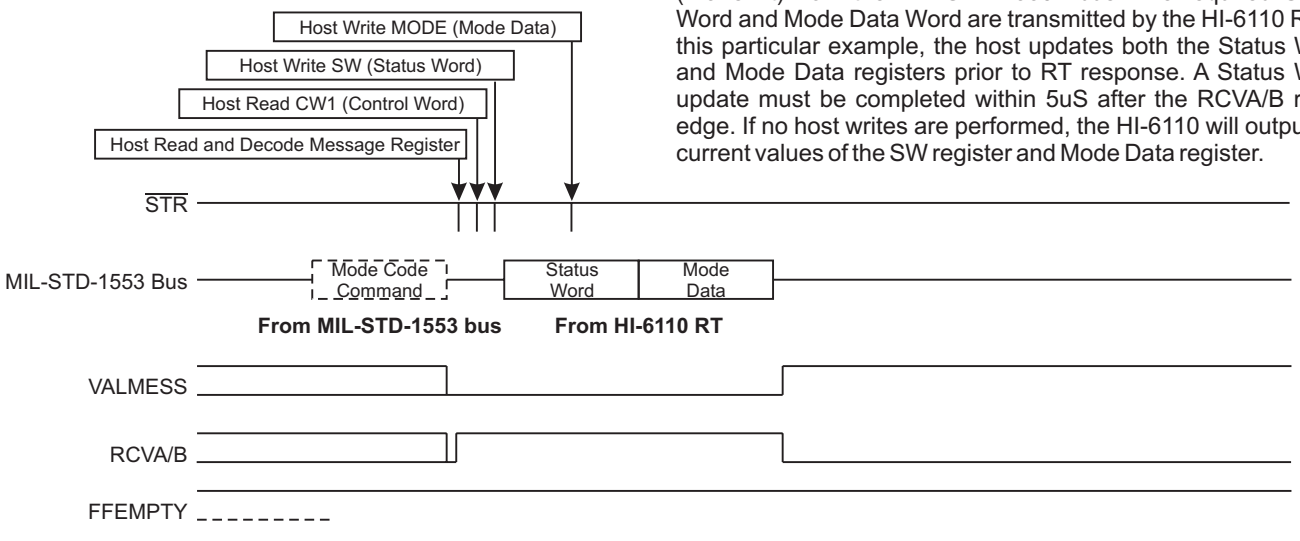
Example 5. Mode Code Command without Data Word

The HI-6110 RT receives a Mode Code Command without Data Word from the MIL-STD-1553 bus. The correct Status Word is output. In this example, the host updates the Status Word register prior to RT response. The Status Word update must be completed within 5uS after the RCVA/B rising edge. If no host write is performed, the HI-6110 will output the current value of the



Example 6. Mode Code with Data Word (Transmit)

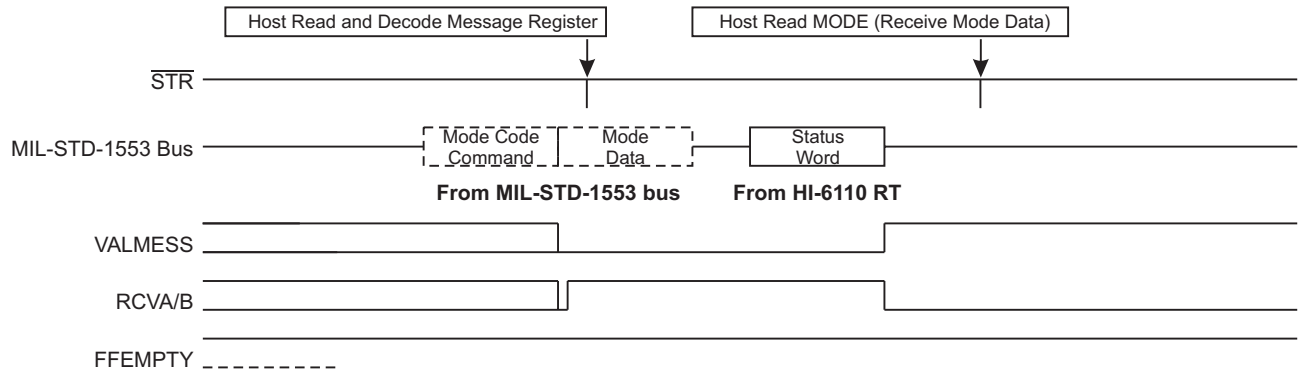
The HI-6110 RT receives a Mode Command with Data Word (Transmit) from the MIL-STD-1553 bus. The required Status Word and Mode Data Word are transmitted by the HI-6110 RT. In this particular example, the host updates both the Status Word and Mode Data registers prior to RT response. A Status Word update must be completed within 5uS after the RCVA/B rising edge. If no host writes are performed, the HI-6110 will output the current values of the SW register and Mode Data register.



EXAMPLE RT MIL-STD-1553 MESSAGE SEQUENCES

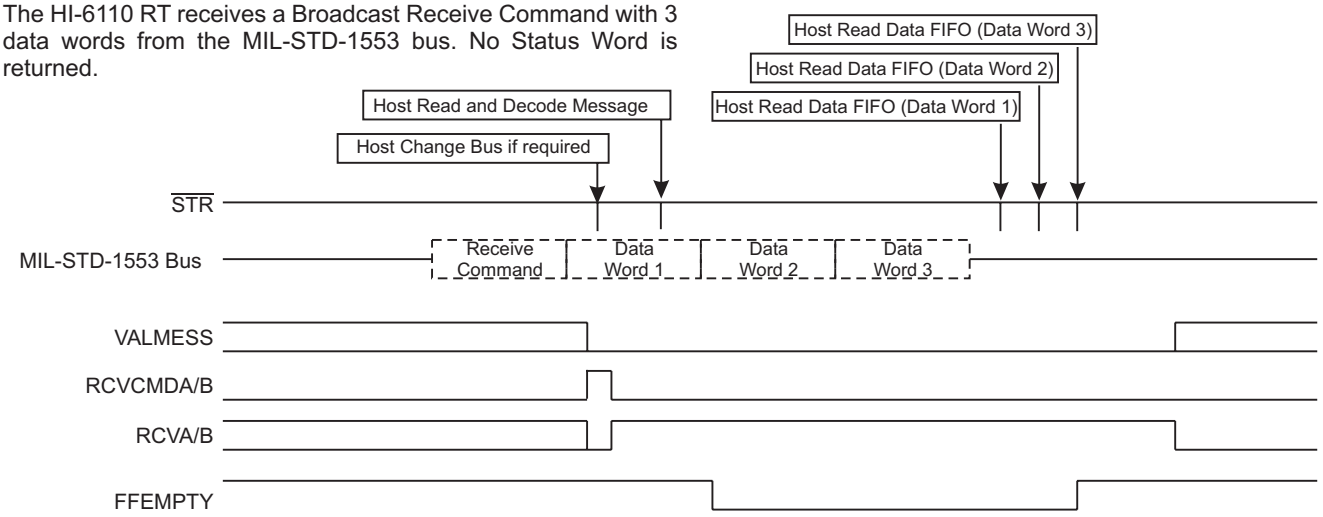
Example 7. Mode Code with Data Word (Receive)

The HI-6110 RT receives a Mode Command with Data word (Receive) from the MIL-STD-1553 bus. The correct Status Word is returned and the host reads the Mode Data value. In this particular example, the host reads the Message Register to determine what type of MIL-STD-1553 command was received. A default value is used for the Status Word response.



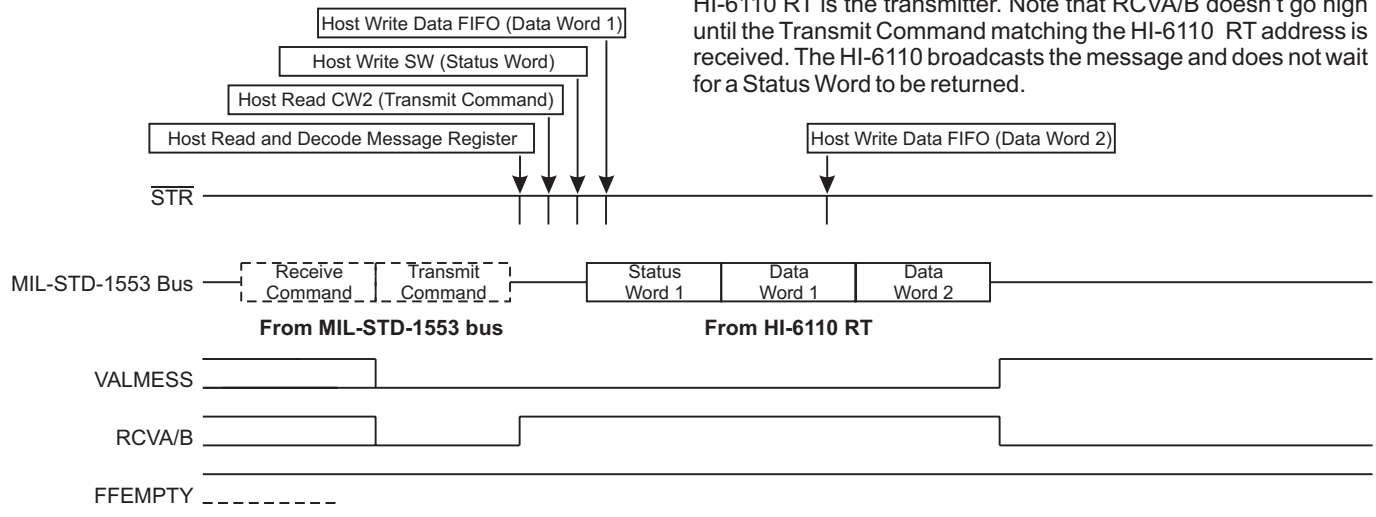
Example 8. Broadcast BC to RT Transfer

The HI-6110 RT receives a Broadcast Receive Command with 3 data words from the MIL-STD-1553 bus. No Status Word is returned.



Example 9. Broadcast RT to RT Transfer HI-6110 is the transmitting RT

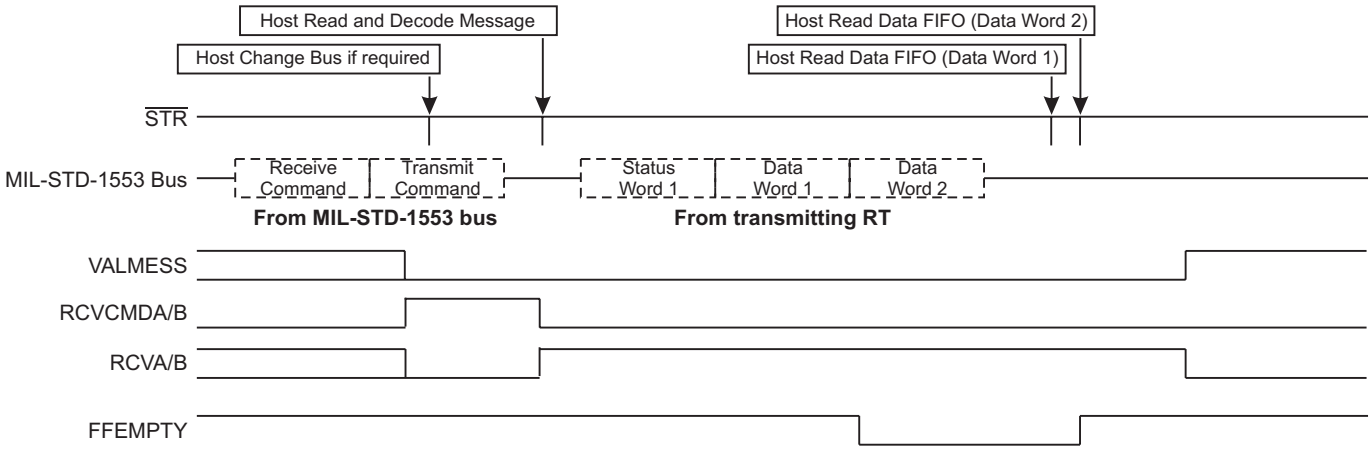
The HI-6110 RT receives a Broadcast RT to RT transfer Command with 2 data words from the MIL-STD-1553 bus. The HI-6110 RT is the transmitter. Note that RCVA/B doesn't go high until the Transmit Command matching the HI-6110 RT address is received. The HI-6110 broadcasts the message and does not wait for a Status Word to be returned.



EXAMPLE RT MIL-STD-1553 MESSAGE SEQUENCES

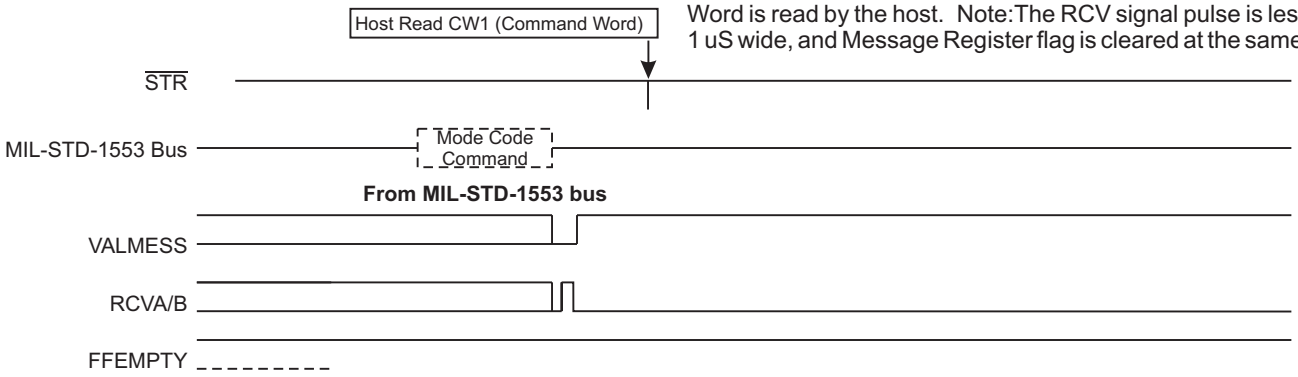
Example 10. Broadcast RT to RT Transfer, HI-6110 is the receiving RT

The HI-6110 RT receives a Broadcast RT to RT transfer Command with 2 data words from the MIL-STD-1553 bus. The HI-6110 RT is the receiver. The HI-6110 captures the message which is read by the host. A Status Word is not transmitted.



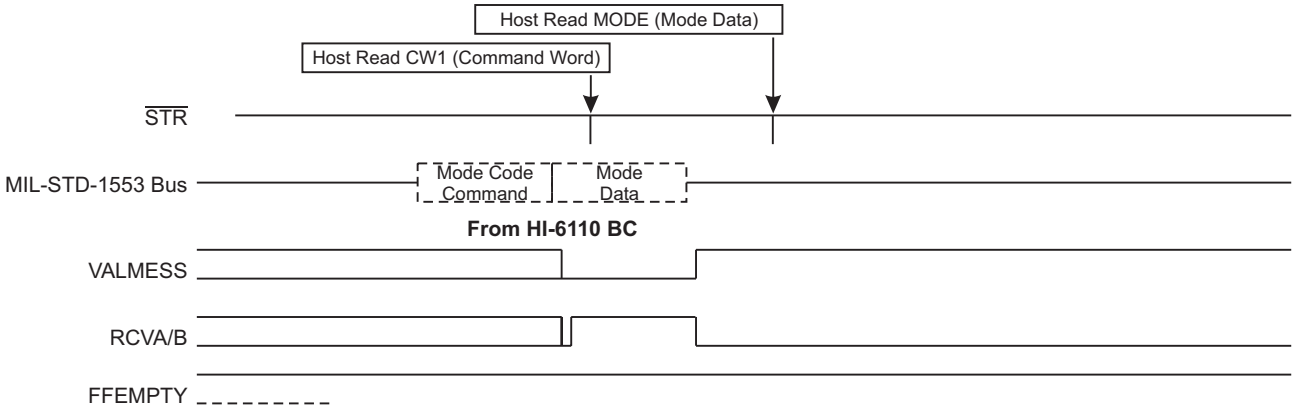
Example 11. Broadcast Mode Code without Data Word

The HI-6110 RT receives a Broadcast Mode Command without Data word from the MIL-STD-1553 bus. The Mode Command Word is read by the host. Note:The RCV signal pulse is less than 1 uS wide, and Message Register flag is cleared at the same time.



Example 12. Broadcast Mode Code with Data Word

The HI-6110 RT receives a Broadcast Mode Command with Data word from the MIL-STD-1553 bus. The host reads the Mode Data word received.



BUS MONITOR

The HI-6110 may be configured as Bus Monitor with or without an assigned RT address. Resetting both BCMODE and RTMODE to "0" configures the HI-6110 as a Bus Monitor with assigned RT address (MT/RT mode). Setting both BCMODE and RTMODE to "1" configures the HI-6110 as a Bus Monitor without an RT address (MT mode). In either Mode, the HI-6110 captures all information that occurs on the selected MIL-STD-1553 bus. All bus transactions are checked for errors. If a message sequence is good, the VALMESS signal is asserted at the end of the message. If an error occurs, ERROR is asserted. The host may interrogate the ERROR Register to determine the nature of the error. Command Words, Status Words, Message Data and Mode Words are captured for all bus transactions and may be read by the host.

In MT/RT mode, the HI-6110 will respond to all MIL-STD-1553 messages with assigned RT address matching the pin-programmed RT address. All conditions pertinent to RT responses are described in the previous Remote Terminal Mode section of this document.

In MT mode (no assigned RT address), the HI-6110 does not transmit information to the MIL-STD-1553 bus and acts as a passive monitor as described by the MIL-STD-1553 specification.

Figure 3 represents the HI-6110 in MT mode.

INITIALIZATION

In Bus Monitor mode, the user must first perform a Master Reset to initialize the MT protocol engine and clear all message registers and data FIFOs. This may be achieved by pulsing the MR input high, or writing a "1" to Control Register bit 0. The user must select a master clock (CLK) frequency by programming Control Register bits 11 and 12. Refer to the MT Register Formats section for a full description of available registers and their functions in Bus Monitor Mode.

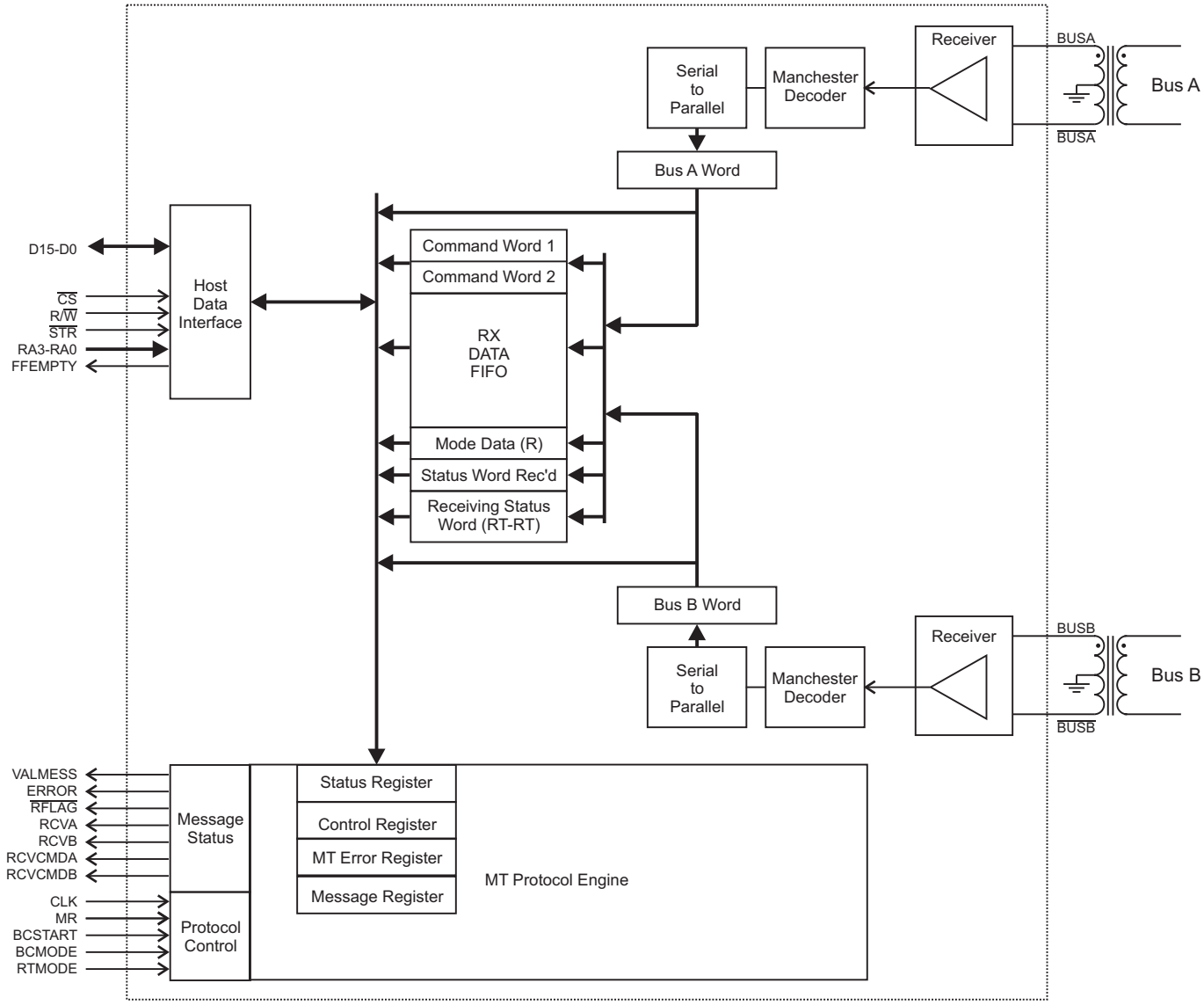
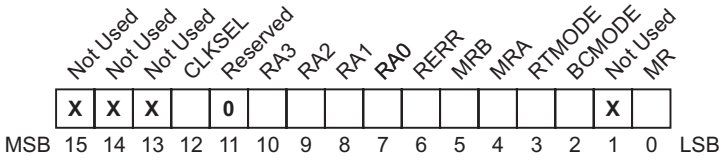


Figure 3. Block Diagram - Bus Monitor (without assigned RT address) Mode

REGISTER FORMATS (MT Mode)

CONTROL REGISTER (R/W) Write Address: X1XX, Read Address: 1100



The Control Register value specifies HI-6110 operating mode, clock frequency and specifies which bus is enabled for monitoring. Control Register bits can also be used for addressing registers in read/write operations, or to assert master reset.

BIT	NAME	FUNCTION
15-13	-	Not used in MT mode.
12	CLKSEL	Selects the frequency of the HI-6110 external CLK input, as follows:

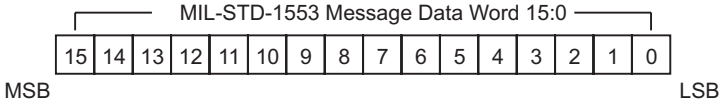
CLKSEL	Value
0	24 MHz
1	12 MHz

11	Reserved	Must be reset to “0”
10 - 7	RA3:0	Register Address for HI-6110 register and data read / write operations. The register address is defined by the logical OR of these bits and their corresponding input pins. Setting Control Register bits 10:7 to 0000 ensures that just the address input pins control register addressing.
6	RERR	Reset ERROR. If RERR is low the ERROR output signal is only reset on reception of a new valid command. Setting RERR high (rising edge) resets a high ERROR output . If the RERR bit is left high, ERROR outputs will automatically reset after 3 to 4 microseconds. For normal operation, this bit is set to “1”.
5 - 4	MRB, MRA	Setting either MRA or MRB to "1"connects the protocol engine to Monitor BUS A or Monitor BUS B. Setting both MRA and MRB selects neither bus. The 1553 receiver, Manchester decoder and RCV output signal remain operational on the inactive bus. When the monitor terminal receives a command on the inactive bus, its RCV signal output goes high. The MT must switch active buses so received data words, message results, etc. will be stored in the proper registers. Valid words received on the inactive bus can be read without changing active bus by reading the Bus A Word or Bus B Word Register, but any received message words, errors, message results etc. are not updated if the bus is not enabled by setting the appropriate MRA or MRB bit.
3 - 2	RTMODE, BCMODE	HI-6110 mode select. These Control Register bits are logically OR'ed with their corresponding input pins. The user can select 1553 operating mode under either hardware or software control:

RTMODE	BCMODE	1553 OPERATING MODE
0	1	Bus Controller (BC)
1	0	Remote Terminal (RT)
1	1	Bus Monitor without assigned RT address (MT)
0	0	Bus Monitor with assigned RT address (RT-MT) in which Control Register bits 5:4 enable transmit for valid commands for which command terminal address matches the assigned Remote Terminal address. See the RT mode section.

1	-	Not used in MT mode.
0	MR	Master Reset. Writing "1" and then “0” to this bit performs the same function as pulsing the MR pin. All register and data FIFOs are cleared when master reset is asserted. The Control Register is the exception; it is not affected by Master Reset.

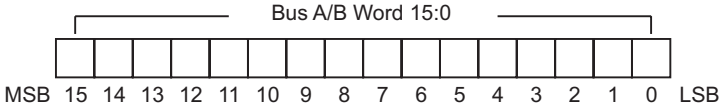
RECEIVE DATA FIFO (Read only) Read Address: 0100



The Receive Data FIFO is 32-words deep and holds all MIL-STD-1553 received data words. The FIFO is cleared at Master Reset.

A low FFEMPTY flag (output pin or Status register bit) means FIFO data is available to be read by the host. Successive data word fetches will cause FFEMPTY to go high when the last data word is read.

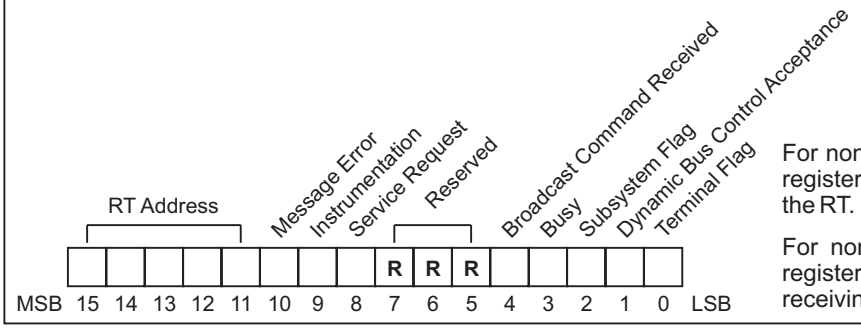
BUS A WORD REGISTER (Read only) Read Address: 1001
BUS B WORD REGISTER (Read only) Read Address: 1010



In MT mode, the Bus A Word register holds the last valid MIL-STD-1553 word received on Bus A. The Bus B Word register holds the last valid MIL-STD-1553 word received on Bus B.

MT OPERATION

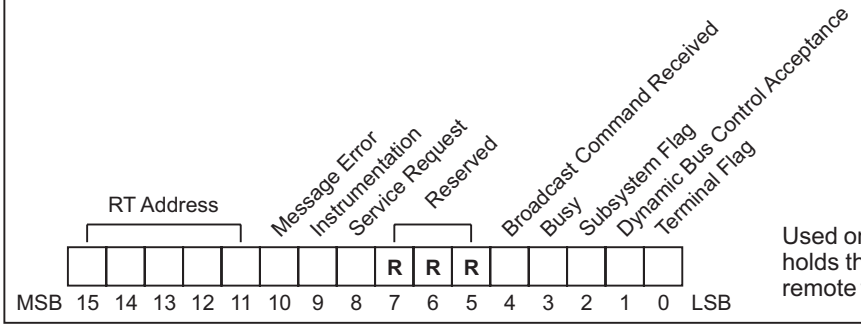
STATUS WORD 1 REGISTER (Read only) Read Address: 1000



For non-broadcast single-RT commands, the Status Word 1 register holds the MIL-STD-1553 Status Word transmitted by the RT.

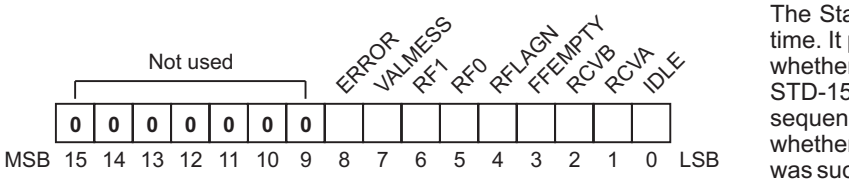
For non-broadcast RT-RT commands, the Status Word 1 register holds the MIL-STD-1553 status word send by the receiving remote terminal.

STATUS WORD 2 REGISTER (Read only) Read Address: 0011



Used only for RT to RT messages, the Status Word 2 register holds the MIL-STD-1553 status word sent by the transmitting remote terminal.

STATUS REGISTER (Read only) Read Address: 0101

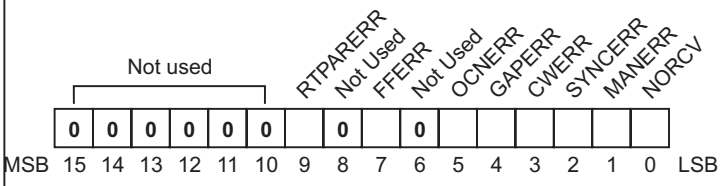


The Status Register may be interrogated by the host at any time. It provides information that allows the user to determine whether the HI-6110 MT is busy monitoring an active MIL-STD-1553 message and its progress. After a message sequence has completed, the Status register indicates whether an error was detected or if the message sequence was successful.

BIT	NAME	FUNCTION
15- 9	-	Not used. These bits are set to "0".
8	ERROR	This bit is set to "0" after reset or when the last MIL-STD-1553 message sequence was valid. ERROR is set to a "1" if the last sequence had an error. The nature of the message error can be determined by examining the Error Register. The ERROR output pin reflects the state of this bit.
7	VALMESS	This bit is a "0" after reset or the last MIL-STD-1553 message contained an error. VALMESS goes high on the completion of an error-free MIL-STD-1553 message sequence. VALMESS is reset to a zero each time new valid Command Word is received by the RT. The VALMESS output pin reflects the state of this bit.
6	RF1	Register address bit 1 for the last written word register.
5	RF0	Register address bit 0 for the last written word register.
4	RFLAGN	Goes low when a new MIL-STD-1553 Command Word is received by the RT, or a Status Word is received from the receiving RT during an RT - to - RT transfer. RFLAGN returns high momentarily upon the receipt of any new 1553 word. The $\overline{\text{RFLAG}}$ output reflects the state of this bit.
3	FFEMPTY	If "0" then the receive Data FIFO contains at least one word of data. This bit is set to a "1" on reset, or when the user has read all available received data words from the receiver Data FIFO. The FFEMPTY output pin reflects the state of this bit.
2	RCVB	Set to a "1" upon receipt of a valid Command Word. The RCVB output pin mirrors the state of this bit.
1	RCVA	Set to a "1" upon receipt of a valid Command Word. The RCVA output pin mirrors the state of this bit.
0	IDLE	If "1" then the RT is idle. This bit is a zero throughout the time the RT is processing a valid MIL-STD-1553 Command. message. The bit returns to a "1" when the message is completed.

MT OPERATION

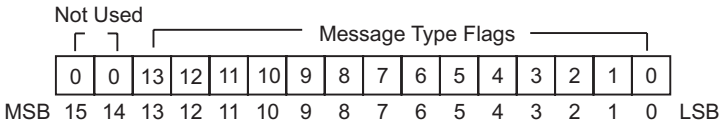
ERROR REGISTER (Read only) Read Address: 0111



The RT Error Register is cleared at reset and on receipt of a valid MIL-STD-1553 Command Word. If an error is encountered during message execution, the ERROR pin goes high, the ERROR bit is set in the Status Register, and one or more bits are set in the Error Register. The host may interrogate the Error register at any time to determine the type of error encountered.

BIT	NAME	FUNCTION
15- 10	-	Not used. These bits are set to "0".
9	RTPARERR	RT Parity Error: There is a parity error in the pin-programmed RT address of this RT.
8	-	Not used. This bit is set to "0".
7	FFERR	Data was not available in the Transmit Data FIFO.
6	-	Not used. This bit is set to "0".
5	CONERR	Contiguous Message Error: Transmission was not contiguous.
4	GAPERR	Bus activity was detected in the 4.0 uS gap after a valid message was completed.
3	WCERR	Word Count Error.
2	SYNCERR	Sync Error: Expected Command Sync and got Data Sync, or vice versa.
1	MANERR	Manchester Encoding Error: The decoder detected an error in Manchester encoding, bit count or parity.
0	NORCV	This bit is set when a data word is expected while processing a receive command, but a gap is detected. It is also set when an RT-to-RT "No Response Timeout" occurs, as defined per MIL-HDBK-1553, Figure 8 "RT-RT Timeout Measurement". The HI-6110 asserts this error when the bus dead-time between the RT-RT command pair and the transmit RT Status Word exceeds 15 uS.

MESSAGE REGISTER (Read only) Read Address: 0110



The Message Register identifies command type when a new valid command is received from the MIL-STD-1553 bus controller. When a valid command is received, message type is decoded and appropriate Message Register bit(s) are set. Register bits 5 and 13 are mirrored.

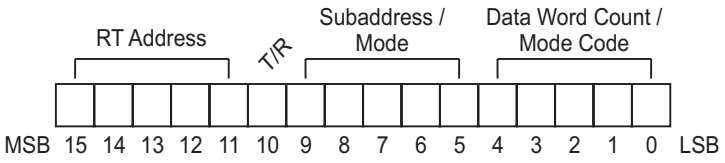
Broadcast commands occur when Command Word bits 15:11 = 11111. Values other than 11111 indicate the Remote Terminal address for a non-broadcast command. Message Register bit 10 is set for any mode code or transmit command. This enables detection of the three undefined mode code command types listed under Bit 10 below.

Hex	Last Valid Command Decoded			Command Word 1 Bit Fields				Command Word 2 Bit Fields			
	NON-MODE COMMANDS			15:11	10	9:5	4:0	15:11	10	9:5	4:0
0001	Receive command from BC, not broadcast			RTA	0	00001-11110	XXXXX				
0080	Receive command from BC, broadcast			11111	0	00001-11110	XXXXX				
0004	RT-RT command, not broadcast			RTA	0	00001-11110	XXXXX	XXXXX	1	00001-11110	XXXXX
0100	RT-RT command, broadcast			11111	0	00001-11110	XXXXX	not RTA	1	00001-11110	XXXXX
0402	Transmit command, RT to BC			RTA	1	00001-11110	XXXXX				
	MODE CODE COMMANDS										
0410	MC0 - MC15	T/R=1	no mode data, not broadcast	RTA	1	0000 or 11111	0XXXX	Command Word 2			
0400 *	MC0 - MC15	T/R=1	no mode data, broadcast	11111	1	0000 or 11111	0XXXX	only applies for			
0410	MC0 - MC15	T/R=0	not broadcast, UNDEFINED	RTA	0	0000 or 11111	0XXXX	RT-RT commands			
0400	MC0 - MC15	T/R=0	broadcast , UNDEFINED	11111	0	0000 or 11111	0XXXX				
2420	MC16 - MC31	T/R=1	mode data, not broadcast	RTA	1	0000 or 11111	1XXXX				
0400 *	MC16 - MC31	T/R=1	broadcast , UNDEFINED	11111	1	0000 or 11111	1XXXX				
0040	MC16 - MC31	T/R=0	mode Data, not broadcast	RTA	0	0000 or 11111	1XXXX				
0800	MC16 - MC31	T/R=0	mode data, broadcast	11111	0	0000 or 11111	1XXXX				

* Two cases where 0400 is reset 550nS after RCV

MT OPERATION

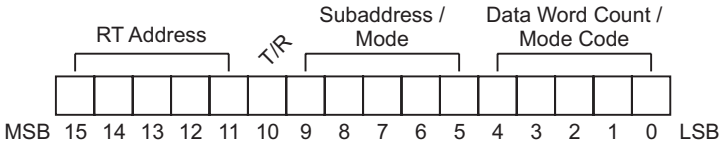
COMMAND WORD 1 REGISTER (Read only) Read Address: 0000



For all commands except RT to RT, the Command Word 1 register contains the last valid Command Word received.

When RCV is asserted, if Message Register bit 2 or bit 8 is set, the new message is RT to RT. The Command Word 1 register holds the first (receive) command and the Command Word 2 Register holds the second (transmit) command.

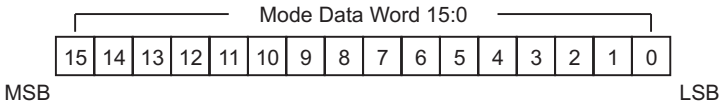
COMMAND WORD 2 REGISTER (Read only) Read Address: 0001



The Command Word 2 register contains the second (transmit) command word from the last RT-RT message. (See note above for Command Word 1.)

Whenever RCV is asserted, RT-RT messages can be detected by checking Message Register bits 2 and 8.

RECEIVE MODE DATA REGISTER (Read only) Read Address: 0010



The read-only Receive Mode Data Register holds the Mode Code Data Word received during a Mode Code with Data Word (Receive) Command.

BUS MONITOR OPERATION (MT mode)

When configured as a Bus Monitor with no assigned RT address, the HI-6110 continuously monitors the selected MIL-STD-1553 bus and passively captures all bus traffic. The HI-6110 never transmits information onto the bus. When a Command Word is received, a validation check is performed. If the Command Word contains no errors, the $\overline{\text{RFLAG}}$ pin goes low and the HI-6110 MT captures the complete message in its internal registers and Receiver Data FIFO as appropriate.

If the valid Command Word was received on Bus A, the RCVA signal goes high to notify the host that a new message has commenced. The RCVB pin is asserted when the valid Command Word arrived on Bus B.

The Command Word may be read from the Command Word 1 register, or the Message register can be read to directly learn the type of command received.

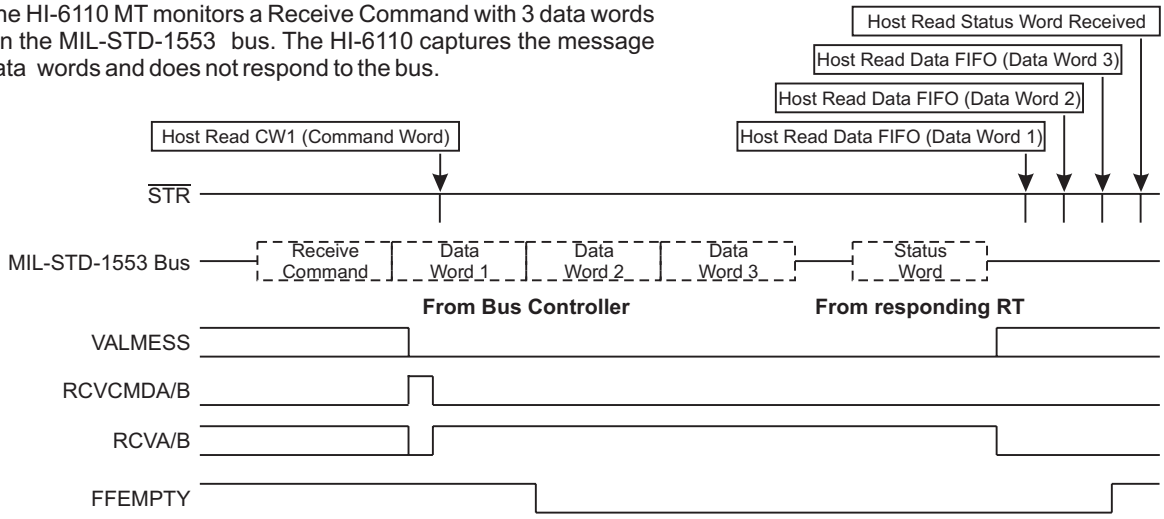
BUS MONITOR OPERATION (MT/RT mode)

When configured as a Monitor with assigned RT address, the HI-6110 responds to all commands that match its hard-wired RT address as described in the RT section of this data sheet. All other bus traffic is monitored as described in this MT section.

EXAMPLE MT MIL-STD-1553 MESSAGE SEQUENCES

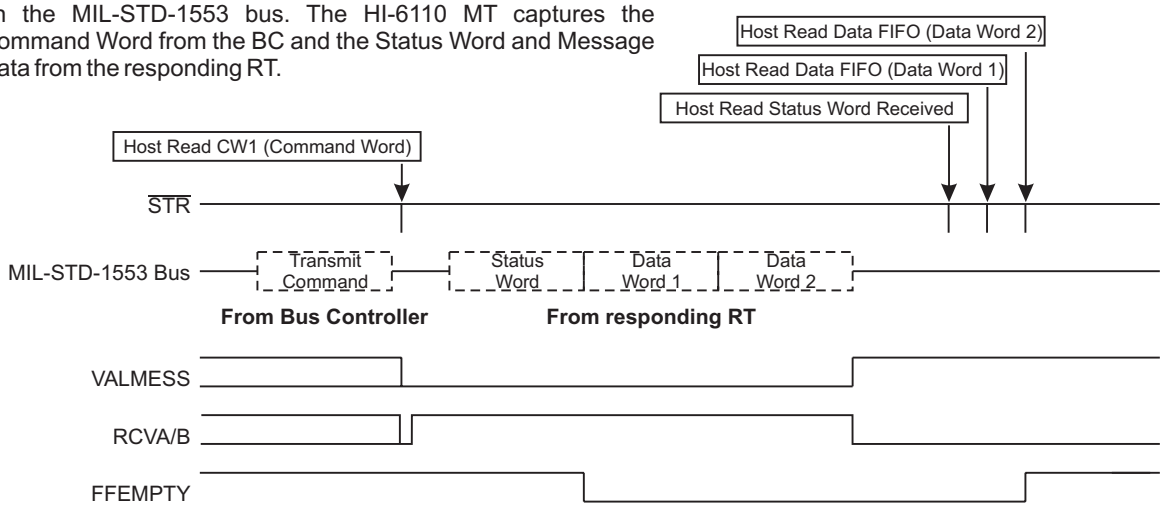
Example 1. BC TO RT Transfer

The HI-6110 MT monitors a Receive Command with 3 data words fon the MIL-STD-1553 bus. The HI-6110 captures the message data words and does not respond to the bus.



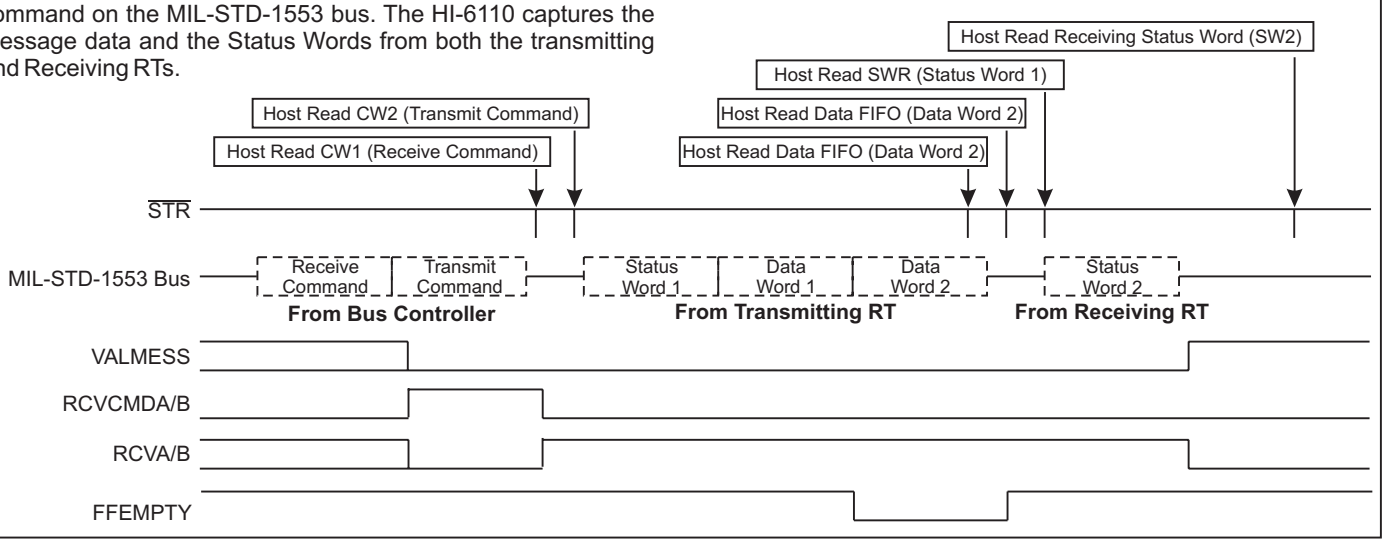
Example 2. RT TO BC Transfer

The HI-6110 MT monitors a Transmit Command with 2 data words on the MIL-STD-1553 bus. The HI-6110 MT captures the Command Word from the BC and the Status Word and Message Data from the responding RT.



Example 3. RT TO RT Transfer

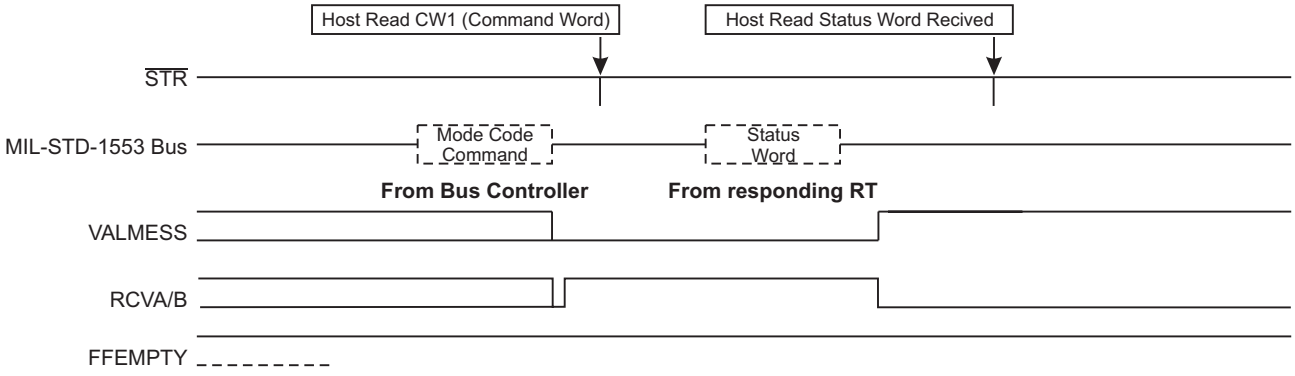
The HI-6110 MT monitors an RT to RT transfer with 2 data words command on the MIL-STD-1553 bus. The HI-6110 captures the message data and the Status Words from both the transmitting and Receiving RTs.



EXAMPLE MT MIL-STD-1553 MESSAGE SEQUENCES

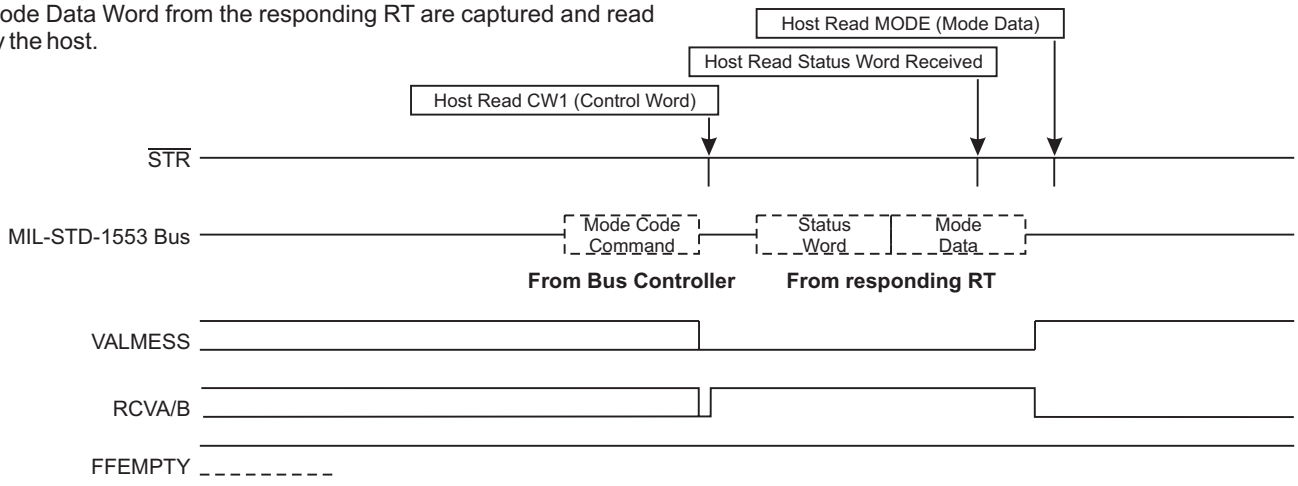
Example 4. Mode Code Command without Data Word

The HI-6110 MT monitors a Mode Code Command on the MIL-STD-1553 bus. The responding RT's correct Status Word is captured.



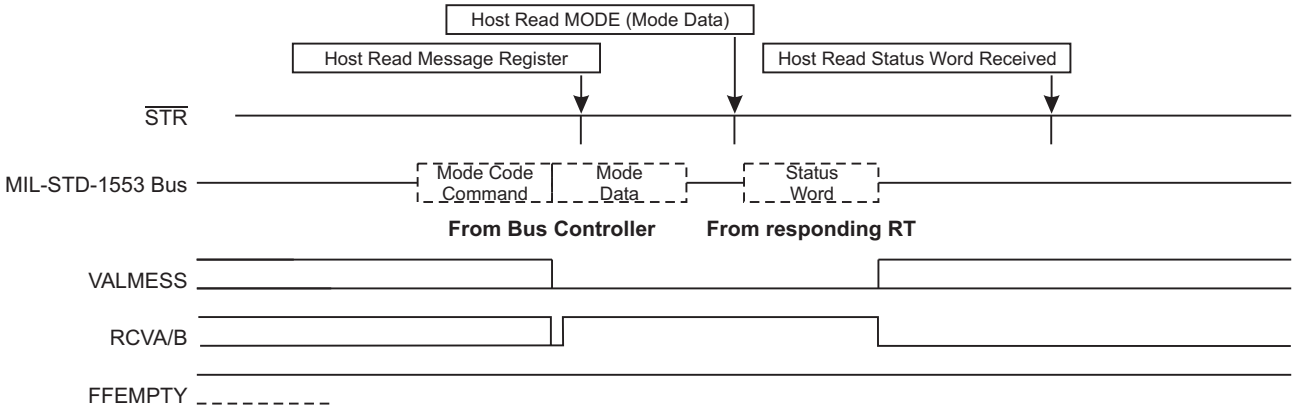
Example 5. Mode Code with Data Word (Transmit)

The HI-6110 MT monitors a Mode Command with Data word (Transmit) on the MIL-STD-1553 bus. The Status Word and Mode Data Word from the responding RT are captured and read by the host.



Example 6. Mode Code with Data Word (Receive)

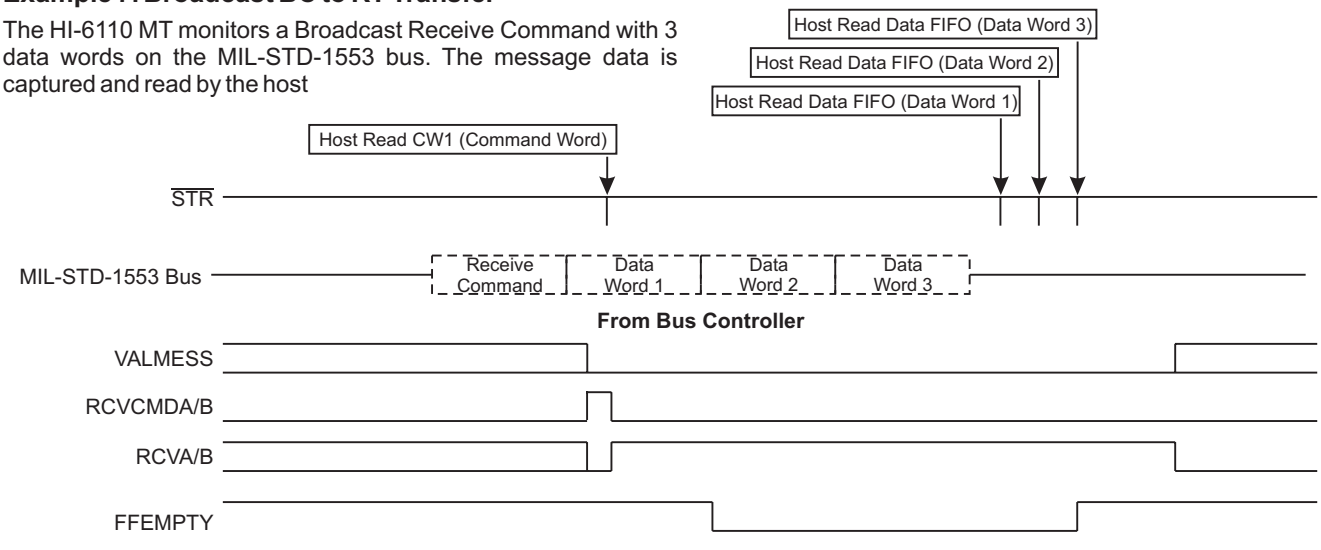
The HI-6110 MT monitors a Mode Command with Data word (Receive) on the MIL-STD-1553 bus. The Mode Data Word from the BC and the Status Word from the responding RT are captured by the HI-6110 MT and read by the host.



EXAMPLE MT MIL-STD-1553 MESSAGE SEQUENCES

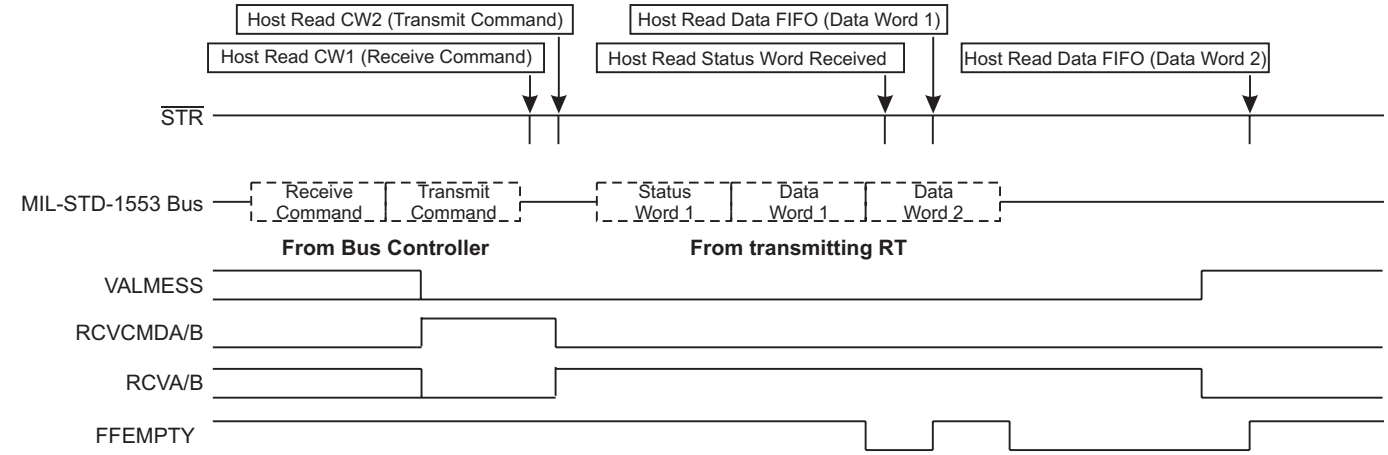
Example 7. Broadcast BC to RT Transfer

The HI-6110 MT monitors a Broadcast Receive Command with 3 data words on the MIL-STD-1553 bus. The message data is captured and read by the host



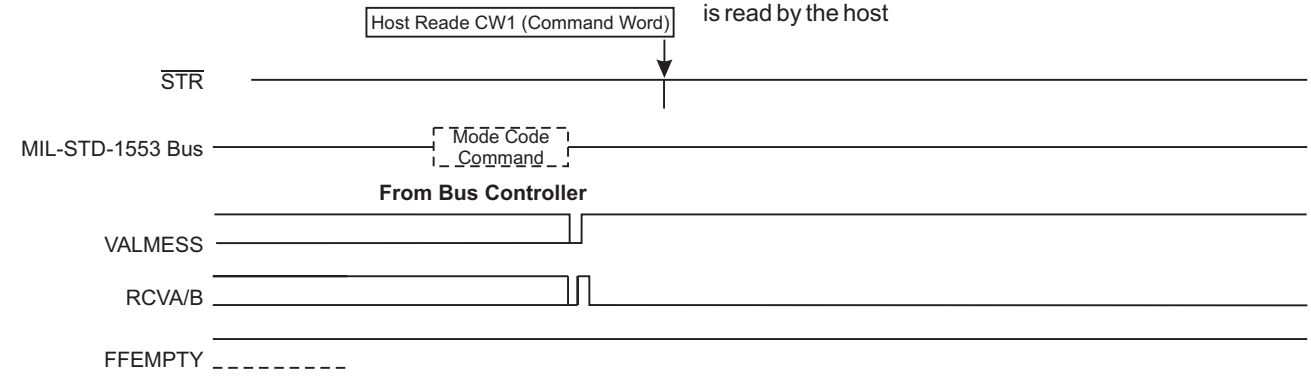
Example 8. Broadcast RT to RT Transfer

The HI-6110 MT monitors a Broadcast RT to RT transfer Command with 2 data words on the MIL-STD-1553 bus. The HI-6110 MT captures the message data and the Status Word from the transmitting RT. Note the behavior of the FFEMPTY signal when the first data word is read, temporarily emptying the FIFO, before message completion.



Example 9. Broadcast Mode Code without Data Word

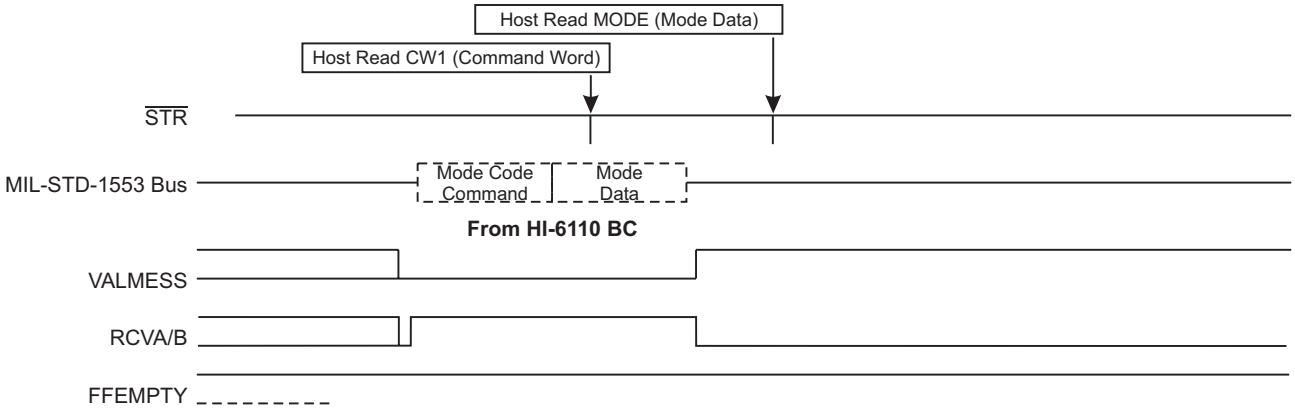
The HI-6110 MT monitors a Broadcast Mode Command without Data word on the MIL-STD-1553 bus. The Mode Command Word is read by the host



EXAMPLE MT MIL-STD-1553 MESSAGE SEQUENCES

Example 11. Broadcast Mode Code with Data Word

The HI-6110 RT receives a Broadcast Mode Command with Data word from the MIL-STD-1553 bus. The host reads the Mode Data word received.



DATA BUS TIMING DIAGRAMS

DATA BUS TIMING - WRITE

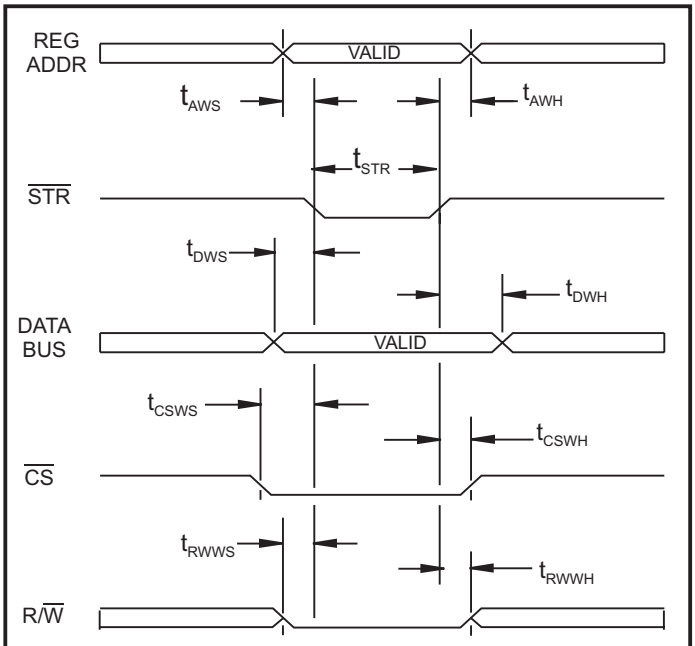


Figure 4.
Refer to AC Electrical Characteristics Table

DATA BUS TIMING - READ

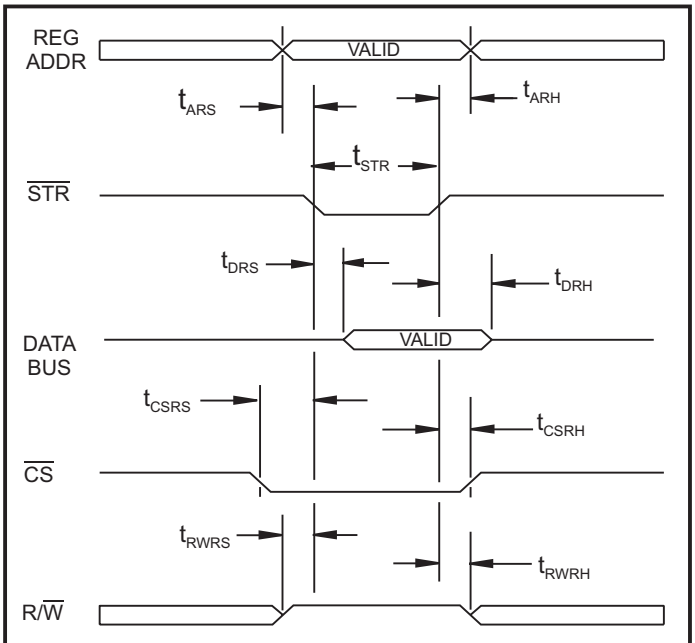


Figure 5.
Refer to AC Electrical Characteristics Table

ABSOLUTE MAXIMUM RATINGS

Supply voltage (VDD)	-0.3 V to +5 V
Logic input voltage range	-0.3 V DC to +3.6 V
Receiver differential voltage	10 Vp-p
Driver peak output current	+1.0 A
Power dissipation at 25°C	1.0 W
Solder Temperature	275°C for 10 sec.
Junction Temperature	175°C
Storage Temperature	-65°C to +150°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage

VDD..... 3.3V... ±5%

Temperature Range

Industrial Screening.....-40°C to +85°C
Hi-Temp Screening.....-55°C to +125°C

NOTE: Stresses above absolute maximum ratings or outside recommended operating conditions may cause permanent damage to the device. These are stress ratings only. Operation at the limits is not recommended.

DC ELECTRICAL CHARACTERISTICS

VDD = 3.3 V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified).

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Voltage	VDD		3.15	3.30	3.45	V
Total Supply Current	ICC1	Not Transmitting		4	10	mA
	ICC2	Transmit one channel @ 50% duty cycle		225	250	mA
	ICC3	Transmit one channel @ 100% duty cycle		425	500	mA
Power Dissipation	PD1	Not Transmitting			0.06	W
	PD2	Transmit one channel @ 100% duty cycle		0.3	0.5	W
Min. Input Voltage (HI)	V_{IH}	Digital inputs	70%			VDD
Max. Input Voltage (LO)	V_{IL}	Digital inputs			30%	VDD
Min. Input Current (HI)	I_{IH}	Digital inputs			20	µA
Max. Input Current (LO)	I_{IL}	Digital inputs	-20			µA
Pull-Up / Pull-Down Current	I_{PUD}	Digital inputs and data bus		275		µA
Min. Output Voltage (HI)	V_{OH}	I_{OUT} = -1.0mA, Digital outputs	90%			VDD
Max. Output Voltage (LO)	V_{IH}	I_{OUT} = 1.0mA, Digital outputs			10%	VDD
RECEIVER (Measured at Point "A_D" in Figure 6 unless otherwise specified)						
Input resistance	R_{IN}	Differential	20			Kohm
Input capacitance	C_{IN}	Differential			5	pF
Common mode rejection ratio	CMRR		40			dB
Input Level	V_{IN}	Differential			9	Vp-p
Input common mode voltage	V_{ICM}		-5.0		5.0	V-pk
Threshold Voltage - Direct-coupled Detect	V_{THD}	1 Mhz Sine Wave (Measured at Point "A_D" in Figure 6)	1.15		20.0	Vp-p
No Detect	V_{THND}				0.28	Vp-p
Theshold Voltage - Transformer-coupled Detect	V_{THD}	1 MHz Sine Wave (Measured at Point "A_T" in Figure 7)	0.86		14.0	Vp-p
No Detect	V_{THND}				0.20	Vp-p

DC ELECTRICAL CHARACTERISTICS (cont.)

VDD = 3.3 V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified)

PARAMETER		SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
TRANSMITTER (Measured at Point "A_D" in Figure 6 unless otherwise specified)							
Output Voltage	Direct coupled	V_{OUT}	35 ohm load	6.0		9.0	Vp-p
	Transformer coupled	V_{OUT}	70 ohm load (Measured at Point "A_T" in Figure 7)	18.0		27.0	Vp-p
Output Noise		V_{ON}	Differential, inhibited			10.0	mVp-p
Output Dynamic Offset Voltage	Direct coupled	V_{DYN}	35 ohm load	-90		90	mV
	Transformer coupled	V_{DYN}	70 ohm load (Measured at Point "A_T" in Figure 7)	-250		250	mV
Output Resistance		R_{OUT}	Differential, not transmitting	10			Kohm
Output Capacitance		C_{OUT}	1 MHz sine wave			15	pF

AC ELECTRICAL CHARACTERISTICS

VDD = 3.3 V, GND = 0V, T_A = Operating Temperature Range (unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMITTER (Measured at Point "A_D" in Figure 6)						
Rise time	tr	35 ohm load	100	--	300	ns
Fall Time	tf	35 ohm load	100	--	300	ns
Inhibit Delay	tDI-H	Inhibited output		--	100	ns
	tDI-L	Active output		--	150	ns

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DATA BUS TIMING - WRITE (See Figure 4)					
Strobe $\overline{STR}$ Pulse Width	t_{STR}	50	--	--	ns
Address Write Setup Time	t_{AWS}	0	--	--	ns
Address Write Hold Time	t_{AWH}	30	--	--	ns
Data Write Setup Time	t_{DWS}	30	--	--	ns
Data Write Hold Time	t_{DWH}	30	--	--	ns
$\overline{CS}$ Write Setup Time	t_{CSWS}	50	--	--	ns
$\overline{CS}$ Write Hold Time	t_{CSWH}	30	--	--	ns
R/$\overline{W}$ Write Setup Time	t_{RWWS}	0	--	--	ns
R/$\overline{W}$ Write Hold Time	t_{RWWH}	30	--	--	ns
DATA BUS TIMING - READ (See Figure 5)					
Strobe $\overline{STR}$ Pulse Width	t_{STR}	80	--	--	ns
Address Read Setup Time	t_{ARS}	0	--	--	ns
Address Read Hold Time	t_{ARH}	30	--	--	ns
Data Read Setup Time	t_{DRS}	--	--	120	ns
Data Read Hold Time	t_{DRH}	--	60	--	ns
$\overline{CS}$ Read Setup Time	t_{CSRS}	0	--	--	ns
$\overline{CS}$ Read Hold Time	t_{CSRH}	30	--	--	ns
R/$\overline{W}$ Read Setup Time	t_{RWRS}	0	--	--	ns
R/$\overline{W}$ Read Hold Time	t_{RWRH}	30	--	--	ns

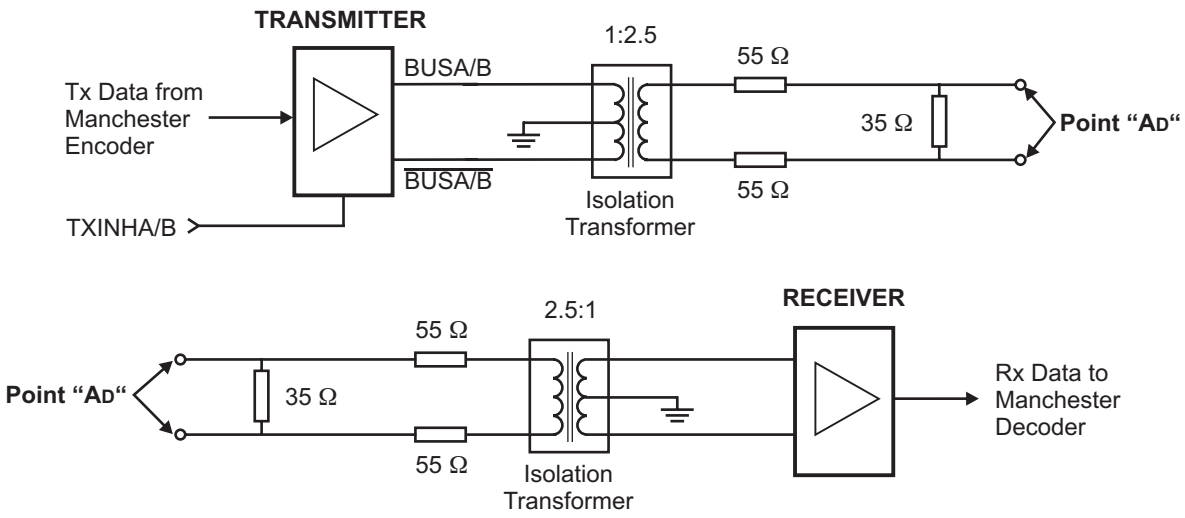


Figure 6. Direct Coupled Test Circuits

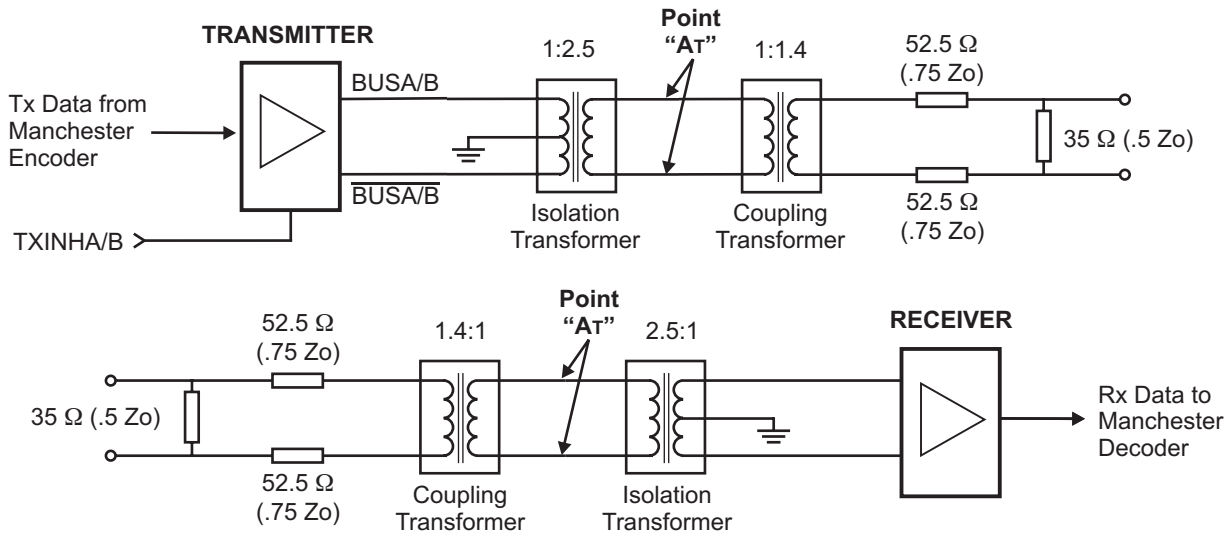


Figure 7. Transformer Coupled Test Circuits

HEAT SINKING THE LEADLESS PLASTIC CHIP CARRIER PACKAGE

The HI-6110PCI/T/M is packaged in a 64 pin leadless plastic chip carrier (LPCC). This package has a metal heat sink pad on its bottom surface, which should be soldered to the printed circuit board for optimum thermal dissipation. The package heat sink is electrically isolated and may be soldered to any convenient power plane or ground plane. Redundant "vias" between the exposed board surface and buried power or ground plane will enhance thermal conductivity.

APPLICATIONS NOTE

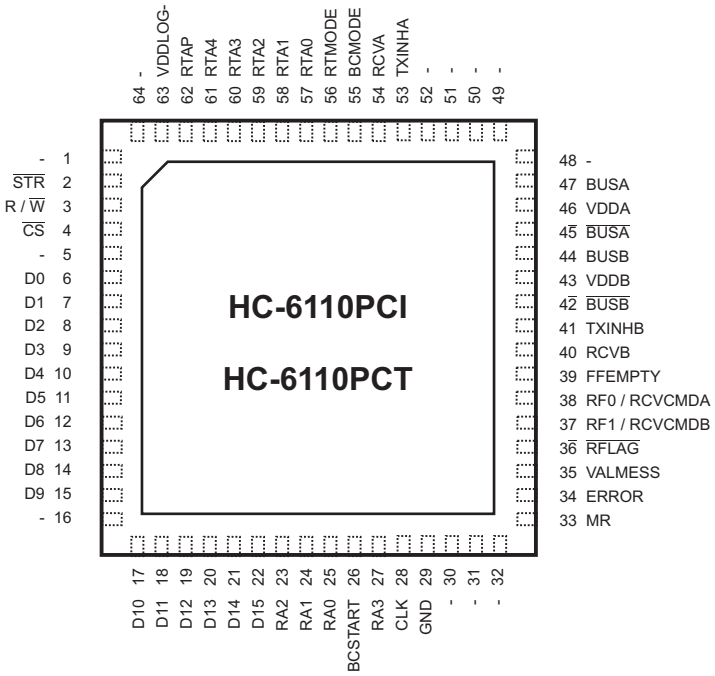
Holt Applications Note AN-500 provides circuit design notes regarding the use of Holt MIL-STD-1553 data communications devices. Layout considerations, as well as recommended interface and protection components are included.

THERMAL CHARACTERISTICS

Data taken at VDD = 3.3V, continuous data transmission at 1 Mbit/s, single transmitter enabled.

PART NUMBER	PACKAGE STYLE	CONDITION	θ_{JA}	JUNCTION TEMPERATURE		
				T_A= 25°C	T_A= 85°C	T_A= 125°C
HI-6110PQI / T	52 pin PQFP	Mounted on circuit board	60.9 °C / W	56°C	116°C	156°C
HI-6110PCI / T	64 pin LPCC	Heat sink pad unsoldered	31.1 °C / W	41°C	101°C	141°C
		Heat sink pad soldered	22.8 °C / W	37°C	97°C	137°C

PIN CONFIGURATION (Top View)



64 Pin Leadless Plastic Chip Carrier (LPCC)

See page 1 for 52-pin PQFP Pin Configuration

ORDERING INFORMATION

HI - 6110 xx x x

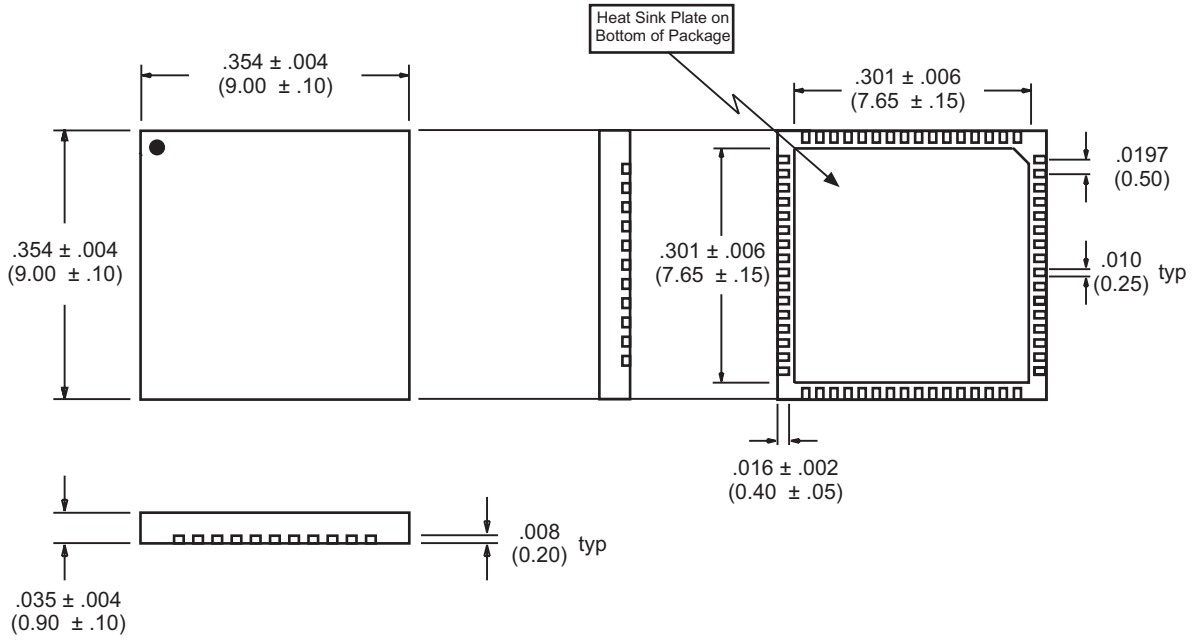
PART NUMBER	
Blank	Tin / Lead (Sn / Pb) Solder
F	100% Matte Tin (Pb-free, RoHS compliant)

PART NUMBER	TEMPERATURE RANGE	FLOW	BURN IN
I	-40°C TO +85°C	I	NO
T	-55°C TO +125°C	T	NO
M	-55°C TO +125°C	M	YES

PART NUMBER	PACKAGE DESCRIPTION
PC	64 PIN PLASTIC 9 x 9 mm CHIP SCALE (not available with “M” flow)
PQ	52 PIN PLASTIC QUAD FLAT PACK (PQFP)

HI-6110 PACKAGE DIMENSIONS *inches (millimeters)*

64-PIN PLASTIC CHIP-SCALE PACKAGE



52-PIN PLASTIC QUAD FLAT PACK (PQFP)

Package Type: 52PQS