IT6663

1-to-2 HDMI2.0/MHL Dual in Active Splitter with EDID RAM

Preliminary Datasheet 0.91

ITE TECH. INC.

General Description

The IT6663 is a one-to-two HDMI2/MHL dual-in, HDMI2 out active splitter that supports a signaling rate up to 6.0Gbps per channel. It is compatible with the latest HDMI 2.0a, MHL 2.2, and HDCP2.2 specifications. The 6.0Gbps bandwidth capability of IT6663 allows it to support content stream such as the popular ultra-high definition 4Kx2K 60Hz format, 3D video with 4Kx2K@30Hz, and so on. SCDC data structure is contained in both TX and RX side of IT6663 such that HDMI2.0 content could be properly received and transmitted to downstream side.

To facilitate system design, IT6663 integrates on-chip CSC conversion (including YCbCr 420/422/444 up or down and RGB/YCbCr conversion), and 4:1 down-sampling function, such that proper video stream could be output to each of the connected display device according to its EDID and cable length.

The installed HDCP2.2 engines and keys on both receiving and transmitting side make IT6663 possible to act as an HDCP2.2/1.x Repeater or an HDCP2.2 to 1.x/HDCP1.x to 2.2 converter, eliminating HDCP compatibility issue. (Note: the HDCP2.2 to 1.x conversion is restricted for closed system application.)

To achieve a friendly remote control environment, the IT6663 provides a complete solution of HDMI CEC function and MHL RCP function as well. With IT6663's embedded CEC/RCP hardware, developers could use high-level software API to implement all the necessary remote control commands easily.

The IT6663 equalizes incoming TMDS signal to optimal and outputs retimed data to downstream sinks. The highly acclaimed equalization technology of ITE TECH. INC. provides for support of long or low-quality HDMI cables at even the highest speeds. Input terminations of the TMDS inputs and output current levels are both programmable.

An EDID RAM is embedded in IT6663 to save the cost of the external EDID ROMs. The process of downloading the EDID data into the RAM is simplified by firmware programming.

The IT6663 operates in software mode that allows the system to control it via a two-line serial interface, PCSCL/PCSDA. Two serial programming addresses can be selected by PCADR.

Features

- Compliant with HDMI2.0, MHL2.2, and HDCP2.2 standards
- Backward compliant with HDMI1.4, HDCP1.X, and MHL1.x standards
- Support RGB and YCbCr 444/422/420 format
- Support CSC (color space conversion) matrix and 420/422/444 conversion(1:1;1:2;2:1)
- Support 4:1 Down-scaling for 4K2K content to 1080P display on legacy display.
- Bypass, CSC-processed, down-scaled content can be selected on each of the 2 output ports individually.
- Serial data rate at up to 6.0Gbps, capable of supporting HDMI 2D video up to 4Kx2K@60Hz and 3D up to 4K2K@30Hz
- Support MHL 24-bit mode and PackedPixel mode up to 1080P@60Hz
- Support Deep Color Mode at up to 36 bits (12 bits/color)
- Support HDMI2 and HDMI1.4 3D format with frame packing/Top and Bottom/side by side mode
- Support HDCP2.2/1.x TX/RX/Repeater function, and also HDCP2.2 to 1.x conversion for legacy HDCP devices on closed system application.
- Integrated pre-programmed HDCP keys
- Pure hardware HDCP2.2 and 1.x engine increasing the robustness and security of HDCP operation
- Embedded EDID RAM saves external EDID ROM costs
- Active source and sink detection for auto low power state implementation
- Embedded CEC/RCP hardware
- Disconnectable input terminations with auto-calibrated impedances
- Adaptive input equalization supporting long and short cables at the same time
- Programmable TMDS output current level
- Programmable source terminations compliant with HDMI 2.0 standard, providing optimal source data eyes at high speeds
- 88-Pin QFN package
- RoHS Compliant (100% Green available)

Pin Diagram

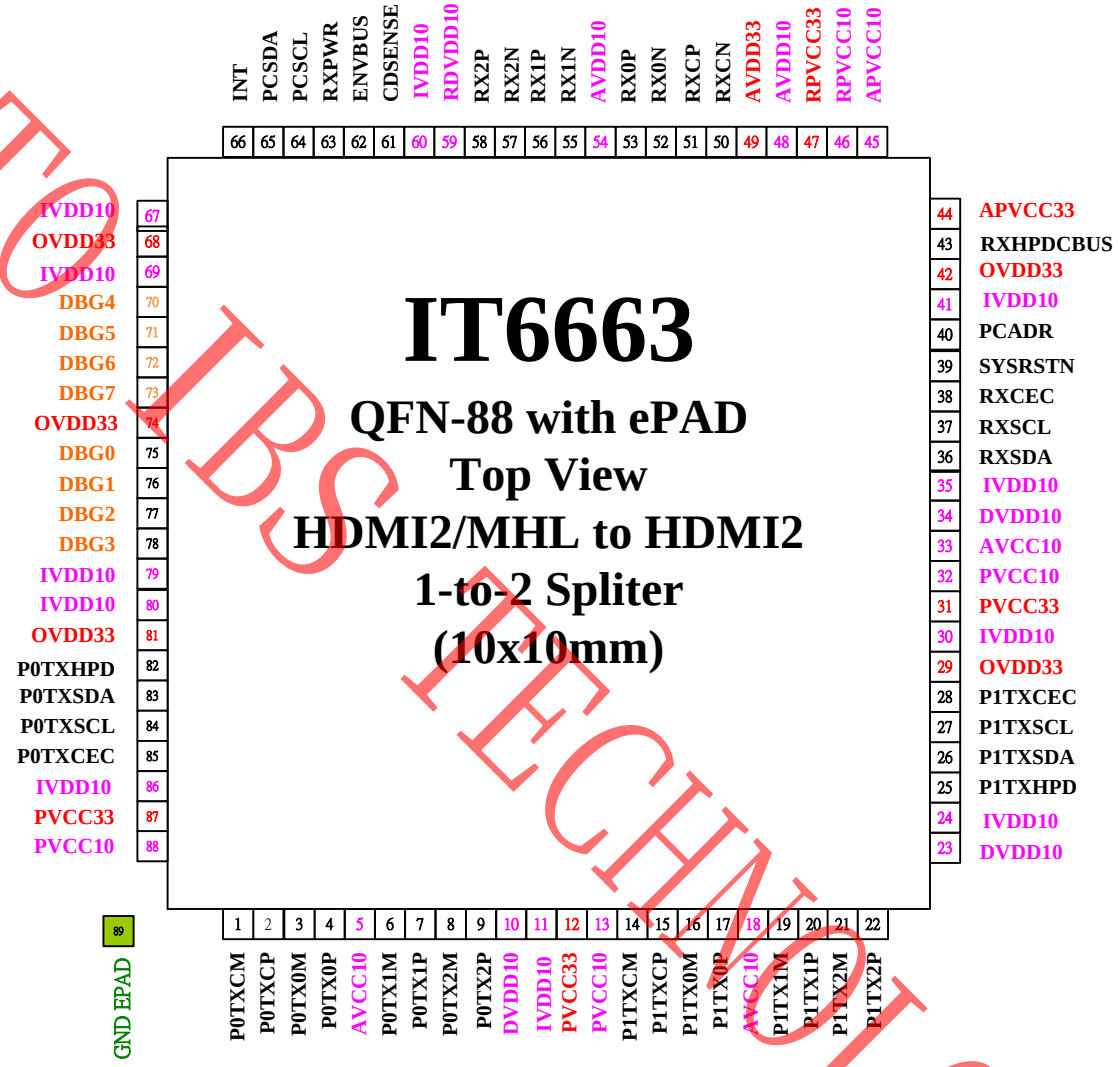


Figure 1. IT6663 pin diagram

Pin Description

TMDS High Speed Differential Input Pins

Pin Name	Direction	Description	Type	Pin No.
RX2P	Input	Channel 2 positive input of input port	TMDS	58
RX2N	Input	Channel 2 negative input of input port	TMDS	57
RX1P	Input	Channel 1 positive input of input port	TMDS	56
RX1N	Input	Channel 1 negative input of input port	TMDS	55
RX0P	Input	Channel 0 positive input of input port	TMDS	53
RX0N	Input	Channel 0 negative input of input port	TMDS	52
RXCP	Input	Clock channel positive input of input port	TMDS	51
RXCN	Input	Clock channel negative input of input port	TMDS	50

TMDS High Speed Differential Output Pins

Pin Name	Direction	Description	Type	Pin No.
P1TX2P	Output	Channel 2 positive output of output port 1	TMDS	22
P1TX2M	Output	Channel 2 negative output of output port 1	TMDS	21
P1TX1P	Output	Channel 1 positive output of output port 1	TMDS	20
P1TX1M	Output	Channel 1 negative output of output port 1	TMDS	19
P1TX0P	Output	Channel 0 positive output of output port 1	TMDS	17
P1TX0M	Output	Channel 0 negative output of output port 1	TMDS	16
P1TXCP	Output	Clock channel positive output of output port 1	TMDS	15
P1TXCM	Output	Clock channel negative output of output port 1	TMDS	14
P0TX2P	Output	Channel 2 positive output of output port 0	TMDS	9
P0TX2M	Output	Channel 2 negative output of output port 0	TMDS	8
P0TX1P	Output	Channel 1 positive output of output port 0	TMDS	7
P0TX1M	Output	Channel 1 negative output of output port 0	TMDS	6
P0TX0P	Output	Channel 0 positive output of output port 0	TMDS	4
P0TX0M	Output	Channel 0 negative output of output port 0	TMDS	3
P0TXCP	Output	Clock channel positive output of output port 0	TMDS	2
P0TXCM	Output	Clock channel negative output of output port 0	TMDS	1

DDC, HPD and PWR5V Control Pins

Pin Name	Direction	Description	Type	Pin No.
RXSCL	I/O	DDC bus clock line of input port	LVTTL 5V-Tol.	37
RXSDA	I/O	DDC bus data line of input port	5V-Tol.	36

P1TXSCL	I/O	DDC bus clock line of Output Port 1	LVTTL 5V-Tol.	27
P1TXSDA	I/O	DDC bus data line of Output Port 1	LVTTL 5V-Tol.	26
P0TXSCL	I/O	DDC bus clock line of Output Port 0	LVTTL 5V-Tol.	84
P0TXSDA	I/O	DDC bus data line of Output Port 0	LVTTL 5V-Tol.	83
P1TXHPD	Input	HPD signal from downstream HDMI Sink to port 1	Schmitt 5V-Tol.	25
P0TXHPD	Input	HPD signal from downstream HDMI Sink to port 0	Schmitt 5V-Tol.	82
RXHPDCBUS	Output/ I/O	HPD signal to be sent back to Source connected to input port. When input port is configured as MHL mode, this is CBUS signal used to communicate with MHL Source connected to input port	LVTTL 5V-Tol.	43
RXPWR	Input	PWR5V of RX input port for detection	Schmitt 5V-Tol.	63

Other Control and Configuration Pins

Pin Name	Direction	Description	Type	Pin No.
SYSRSTN	Input	Hardware reset pin. Active LOW	Schmitt 5V-Tol.	39
PCSCL	Input	Serial programming Clock for chip programming (5V-tolerant)	LVTTL 5V-Tol.	64
PCSDA	I/O	Serial programming Data for chip programming (5V-tolerant)	LVTTL 5V-Tol.	65
PCADR	Input	Control of serial programming device address: '0': 0x58 '1': 0x5A	Schmitt 5V-Tol.	40
INT	Output	Interrupt signal	LVTTL 5V-Tol	66
RXCEC	I/O	CEC signal of input port	LVTTL	38

			5V-Tol	
P1TXCEC	I/O	CEC signal of output port 1	LVTTL 5V-Tol	28
P0TXCEC	I/O	CEC signal of output port 0	LVTTL 5V-Tol	85
CDSENSE	Input	MHL CD sense detection signal	LVTTL 5V-Tol	61
ENVBUS#	Output	Enable MHL VBUS 5V output control signal	LVTTL	62
DBG# (# :0,1,2,3,4,5,6,7)	Output	Debug ports	LVTTL	75, 76, 77, 78, 70, 71, 72, 73

Power and Ground Pins

Pin Name	Description	Type	Pin No.
AVCC10	HDMI analog frontend power (1.0V)	Power	5, 18 , 33
DVDD10	HDMI AFE digital supply power (1.0V)	Power	10, 23, 34
IVDD10	Digital logic power	Power	11, 24, 30, 35, 41, 60, 67, 69, 79, 80 , 86
OVDD33	I/O Pin power and SIPROM power	Power	29, 42, 68, 74, 81
PVCC10	HDMI TX core PLL supply voltage (1.0V)	Power	13, 32, 88
PVCC33	HDMI TX core PLL supply voltage (3.3V)	Power	12, 31, 87
APVCC33	HDMI RX core PLL supply voltage (3.3V)	Power	44
APVCC10	HDMI RX core PLL supply voltage (1.0V)	Power	45
RPVCC33	HDMI RX core PLL supply voltage (3.3V)	Power	47
RPVCC10	HDMI RX core PLL supply voltage (1.0V)	Power	46
RDVDD10	HDMI AFE digital supply voltage (1.0V)	Power	59
AVDD33	HDMI frontend supply voltage (3.3V)	Power	49
AVDD10	HDMI frontend supply voltage (1.0V)	Power	48, 54
GND	Chip ground	Ground	89

Functional Block

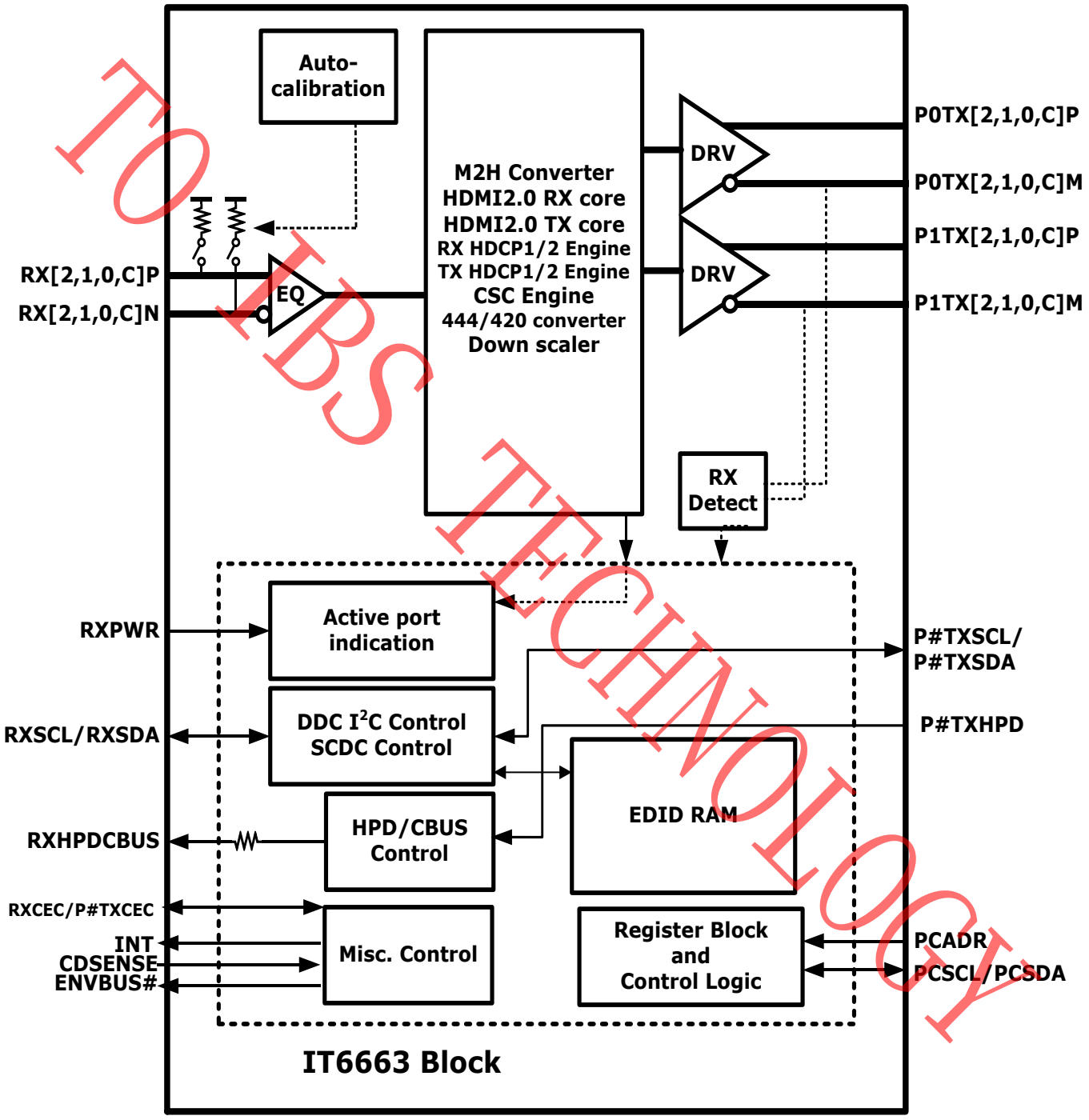


Figure 2. Functional block diagram of IT6663

Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ	Max	Unit
IVDD10	Core logic supply voltage	-0.5		1.2	V
DVDD10	HDMI AFE digital supply power (1.0V)	-0.5		1.2	V
RDVDD10	HDMI AFE digital supply power (1.0V)	-0.5		1.2	V
PVCC10	HDMI core PLL supply voltage (1.0V)	-0.5		1.2	V
APVCC10	HDMI core PLL supply voltage (1.0V)	-0.5		1.2	V
RPVCC10	HDMI core PLL supply voltage (1.0V)	-0.5		1.2	V
AVDD10	HDMI TX analog frontend power (1.0V)	-0.5		1.2	V
AVCC10	HDMI RX analog frontend power (1.0V)	-0.5		1.2	V
PVCC33	HDMI TX core PLL supply voltage (3.3V)	-0.3		4.0	V
APVCC33	HDMI RX core PLL supply voltage (3.3V)	-0.3		4.0	V
RPVCC33	HDMI RX core PLL supply voltage (3.3V)	-0.3		4.0	V
AVDD33	HDMI analog frontend supply voltage (3.3V)	-0.3		4.0	V
OVDD33	I/O pins supply voltage	-0.3		4.0	V
V_I	Input voltage	-0.3		OVDD33+0.3 (normal) 5.5 (5V-tol)	V
V_O	Output voltage	-0.3		OVDD33+0.3	V
T_J	Junction Temperature			125	°C
T_{STG}	Storage Temperature	-65		150	°C
ESD_HB[3]	Human body mode ESD sensitivity	3000			V
ESD_MM[3]	Machine mode ESD sensitivity	200			V

Notes:
1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.
2. Refer to Functional Operation Conditions for normal operation.
3. all signal pins

Functional Operation Conditions

Symbol	Parameter	Min.	Typ	Max	Unit
Power					
IVDD10	Core logic supply voltage	0.95	1.0	1.05	V
DVDD10	HDMI AFE digital supply power (1.0V)	0.95	1.0	1.05	V
RDVDD10	HDMI AFE digital supply power (1.0V)	0.95	1.0	1.05	V
PVCC10	HDMI core PLL supply voltage (1.0V)	0.95	1.0	1.05	V
APVCC10	HDMI core PLL supply voltage (1.0V)	0.95	1.0	1.05	V
RPVCC10	HDMI core PLL supply voltage (1.0V)	0.95	1.0	1.05	V
AVDD10	HDMI TX analog frontend power (1.0V)	0.95	1.0	1.05	V
AVCC10	HDMI RX analog frontend power (1.0V)	0.95	1.0	1.05	V
PVCC33	HDMI TX core PLL supply voltage (3.3V)	3.0	3.3	3.6	V
APVCC33	HDMI RX core PLL supply voltage (3.3V)	3.0	3.3	3.6	V
RPVCC33	HDMI RX core PLL supply voltage (3.3V)	3.0	3.3	3.6	V
AVDD33	HDMI analog frontend supply voltage (3.3V)	3.0	3.3	3.6	V
OVDD33	I/O pins supply voltage	3.0	3.3	3.6	V
$V_{CCNOISE}$	Supply noise			100	mV_{pp}
T_A	Ambient temperature	-20	25	70	°C
Θ_{ja}	Junction to ambient thermal resistance			20.4	°C/W

TMDS Differential Pins					
V_{IDIFF}	TMDS differential input swing (peak-to-peak)	150		1560	mV
V_{TERM}	TMDS output termination voltage[1]	3.135	3.3	3.465	V
T_{bit}	Average bit time of the TMDS data stream	0.166		40	Ns
R_{bit}	Signaling rate of the serial TMDS data stream	250		6000	Mbps
DDC I/O Pins (RXSCL/RXSDA, TXSCL/TXSDA)					
V_{IDDC}	DDC input voltage	0		5.5	V

Notes:

1. PVCC10, APVCC10, RPVCC10, AVDD10, AVCC10, PVCC33, APVCC33, RPVCC33, and AVDD33 should be regulated.

2. See System Design Consideration for supply decoupling and regulation.

DC Electrical Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min.	Typ	Max	Unit
TMDS Differential Output Pins (P[1:0]TX2P/M, P[1:0]TX1P/M, P[1:0]TX0P/M, P[1:0]TXCP/M)						
V_{OHTMDS}	TMDS output high voltage[3]	R_{LOAD}=50Ω	V_{CC}-10		V_{CC}+10	mV
V_{OLTMDS}	TMDS output low voltage[3]	V_{CC}=V_{TERM}=3.3V	V_{CC}-700		V_{CC}-400	mV
V_{swing}	TMDS data output single-ended swing[3]		400		600	mV
V_{swing_C}	TMDS clock output single-ended swing[4]		200		600	mV
I_{OFF}	Single-ended standby output current[3]	V_{OUT}=0			10	μA
$T_{Rxintra}$	Receiver intra-pair skew tolerance	<=2.25GHz			0.4	T_{bit}
		>2.25GHz			0.15T_b+ 112ps	
$T_{Rxinter}$	Receiver inter-pair skew tolerance				1	T_{sym}
$T_{Txintra}$	Transmitter intra-pair skew				0.15	T_{bit}
$T_{Txinter}$	Transmitter inter-pair skew				0.2	T_{sym}
T_{Txcjit}	Transmitter clock jitter[5,6]	<=3GHz			0.25	T_{bit}
		>3GHz			0.3	
T_{Txdjit}	Transmitter data jitter[5,6]	<=3GHz			0.3	T_{bit}
		>3GHz			1-H	
Logic I/O Pins (LVTTL)						
V_{IH}	Input high voltage[1]		2.2		OVDD33	V
V_{IL}	Input low voltage[1]		GND		0.8	V
V_T	Switching threshold[1]			1.5		V
V_{OL}	Output low voltage[1]	I_{OL}=2~16mA			0.4	V
V_{OH}	Output high voltage[1]	I_{OH}=-2~-16mA	2.4			V
V_{T-}	Schmitt trigger negative going threshold voltage[1]		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage[1]			1.6	2.0	V
I_{IN}	Input leakage current[1]	V_{IN}=OVDD33 or 0		±10		μA
I_{OZ}	Tri-state output leakage current[1]	V_{IN}=OVDD33 or 0		±10		μA
I_{OL}	Serial programming output sink current[2]	V_{OUT}=0.2V	4		16	mA
Logic I/O Pins (5V-Tolerant)						
V_{IH}	Input high voltage[1]		2.5		5.5	V
V_{IL}	Input low voltage[1]		GND		0.8	V

V_T	Switching threshold[1]			1.5		V
V_{OL}	Output low voltage[1]	I_{OL}=2~16mA			0.4	V
V_{OH}	Output high voltage[1]	I_{OH}=-2~-16mA	2.4			V
I_{IN}	Input leakage current[1]	V_{IN}=5.5 or 0		±10		μA
I_{OZ}	Tri-state output leakage current[1]	V_{IN}=5.5 or 0		±10		μA
I_{OL}	Serial programming output sink current[2]	V_{OUT}=0.2V	4		16	mA

Notes:
1. Guaranteed by I/O design.
2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real serial programming environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of IT6663 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to the IT6663 Register Table for proper register setting.
3. Limits defined by HDMI 1.4 standard.
4. Limits defined by HDMI 2.0 standard.
5. IT6663's Rx input jitter tolerance capability meets HDMI 1.4 and 2.0 CTS requirement.
   IT6663's Tx output jitter performance meets HDMI1.4 and 2.0 CTS spec if the input of IT6663 meets the spec.
6. Please refer to HDMI2.0 spec. for the definition of H.

Operation Supply Current Specification

Normal Operation(typical)

Vic	Format	TMDS Rate	Audio	HDCP	Total 1.0V (mA)	Total 3.3V (mA)	Total Power (mW)
2	480p	27MHz	2ch192k	1.4	170	58.8	364.04
4	720p	74.25MHz	2ch192k	1.4	192.5	67.8	416.24
16	1080p	148.5MHz	8ch192k	1.4	234	62.4	439.92
100	4k2k 30Hz	297MHz	8ch192k	1.4	342.4	87.7	631.81
100	4k2k 30Hz	297MHz	8ch192k	2.2	432.4	87.7	721.81
97	4k2k 60Hz	594MHz	8ch192k	2.2	647.8	125.4	1061.62

1. The current is tested on the situation that all ports are turned on(1 Rx and 2 Tx), and HDCP1.4 or HDCP2.2 are enabled for each RX and TX port.
2. All input and outputs are with RGB444 8 bit format.

Standby mode(typical)

Total 1.0V (mA)	Total 3.3V (mA)	Total Power (mW)
26	4	39.2

1. Standby mode is entered when no input data is detected on RX side

System Design Consideration

As a high-performance receiver/transmitter, ITE's RX/TX is capable of receiving/transmitting those signals that are attenuated and degraded by the HDMI cables. These signals are usually very small in amplitudes in addition to the distortion that the cable inflicts on them. The analog front-end of ITE's RX/TX is designed to combat environment noises as well as interference to some degree. However, to get the optimum performance the system designers should follow the guideline when designing the application circuits and PCB layout.

Please refer to document "IT6663_HW_Guidelines.doc" for detail description.

Power Sequence

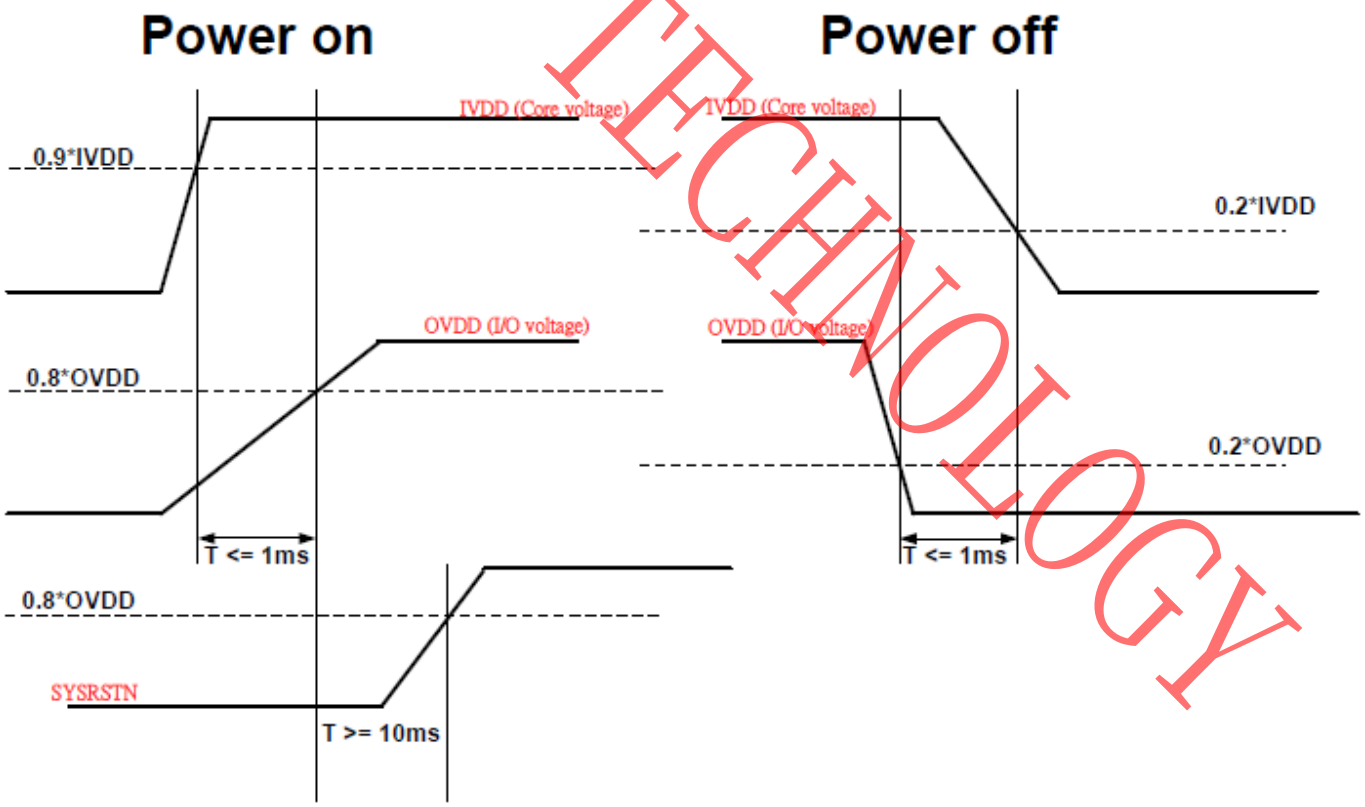
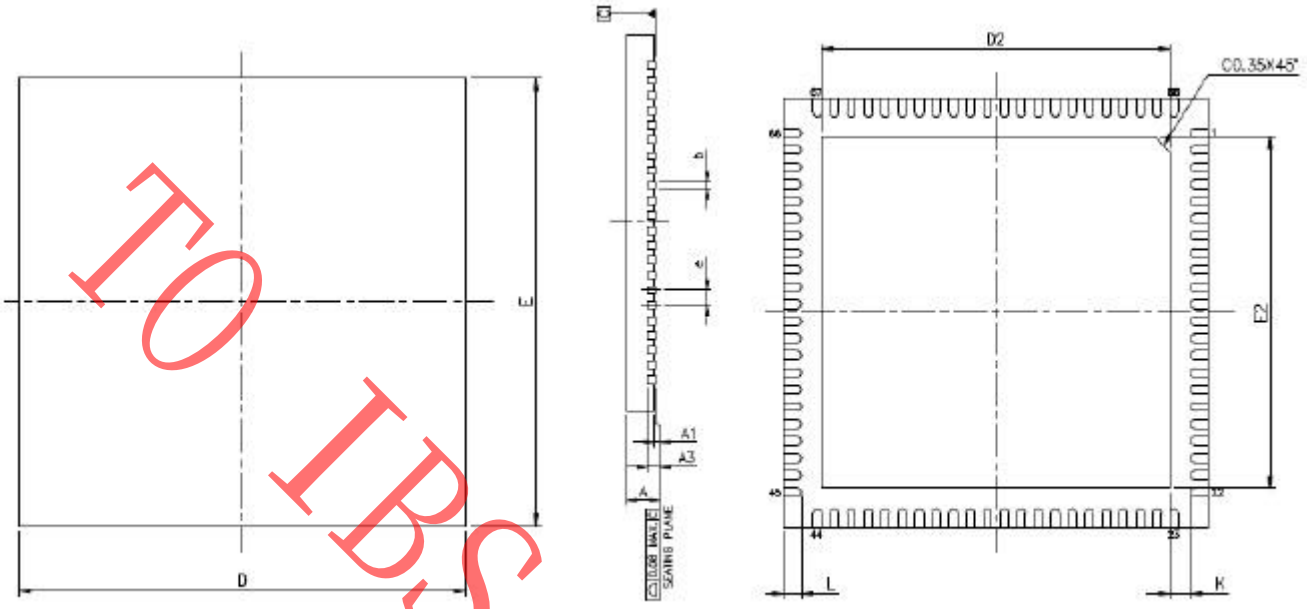


Figure 3. IT6663 Power Sequence

*When power on, please keep IVDD go 0.9*IVDD before OVDD go 0.8*OVDD (IVDD must supply earlier than or equal to OVDD). And please keep the time interval between IVDD and OVDD shorter than 1ms when power on or power off.

Package Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	0.031	0.033	0.035	0.80	0.85	0.90
A1	0.000	—	0.002	0.00	---	0.05
A3	0.007	0.008	0.009	0.183	0.203	0.223
b	0.006	0.008	0.010	0.15	0.20	0.25
D/E	0.390	0.394	0.398	9.90	10.00	10.10
D2/E2	0.315	—	0.325	8.00	---	8.25
e	0.012	0.016	0.020	0.30	0.40	0.50
K	0.008	—	---	0.20	---	—
L	0.012	0.016	0.020	0.30	0.40	0.50

Notes:

1. Controlling dimensions: Millimeter
2. Reference document: JEDEC MO-220
3. Take SMT into consideration, please use the minimum number of D2's and E2's dimensions.

Figure 3. 88-pin LQFP Package Dimensions
(dimension: 10*10*0.9mm, Exposed Area: 8.25*8.25mm)

Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6663	-20~70	88-pin QFN	Green