TECHNICAL INFORMATION

PARASITIC INDUCTANCE OF MULTILAYER CERAMIC CAPACITORS

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Abstract:

The parasitic inductance of multilayer ceramic capacitors (MLCCs) is becoming more important in the decoupling of high speed digital systems. There exists conflicting data and statements on the parasitic inductance of the MLCC. This work shows the measurement techniques of the inductance parameters, focusing mainly on the fixturing needed to accurately measure the chips. The effects of various compensation and calibration methods will also be demonstrated. A comprehensive table will be shown that includes the parasitic inductance for a range of MLCCs from 0402 through 1210.

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I. Introduction

The simplest equivalent circuit model of MLCCs, described in [1] is the series model. The circuit is shown in Figure 1.

Figure 1. Equivalent circuit model of MLCC.

The three elements being the capacitor, the parasitic inductance and series resistance. This paper will focus on the inductance and the methodology used to calculate it.

The parasitic inductance of MLCCs is becoming more and more important in the decoupling of today's high speed digital systems. The relationship between the inductance and the ripple voltage induced on the DC voltage line can be seen from the simple inductance equation:

$$V = L\frac{di}{dt} \qquad [1]$$

The $\frac{di}{dt}$ seen in current microprocessors can be as high as 0.3A/ns [2], with future generations looking at 10A/ns. At 0.3A/ns, 100pH of parasitic inductance can cause a voltage spike of 30mV. While this does not sound very drastic, with the Vcc for microprocessors decreasing at the current rate, this can be a fairly large percentage.

Another important, often overlooked, reason for knowing the parasitic inductance is the calculation of the resonant frequency. This can be important for high frequency, by-pass capacitors, as the resonant point will give the most signal attenuation. The resonant frequency is calculated from the simple equation

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \qquad [2]$$

This paper will discuss the measurement technique used to calculate the inductance, as well as different available methods. A comprehensive table will be given showing the various capacitor case sizes and a curve fit based on the lengths and widths will be derived.

II. Measurement

For this paper, the Hewlett-Packard impedance analyzer, HP4291A, was used exclusively. This analyzer has a frequency range from 1 MHz to 1.8 GHz. Perhaps even more important is the fixture, which was a HP16192A, SMD fixture. This fixture is rated for the entire frequency range of the HP4291A.

Calibration and fixture compensation are the most important procedures for generating relevant data. Open, short and load calibration must be done for the cables and test head, using the devices supplied by HP. Then the fixture compensation must be done, again using open, short and load. Using the pre-programmed compensations is not recommended, as environmental conditions can change day to day.

This compensation and calibration sequence is straight forward, until it comes to the shorting of the fixture. There are two techniques that can be used on the HP16192A. One is to use shorting blocks and the other is to slide the pins together and short them, both shown in Figure 2.
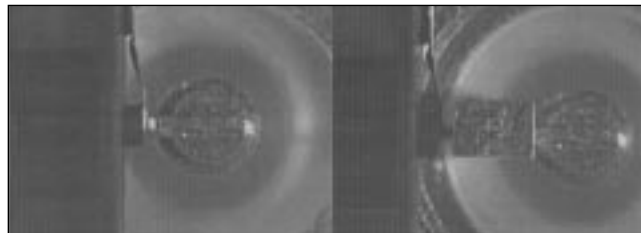

Figure 2. Photograph demonstrating the two shorting techniques for the 16192A fixture.

For an inductance measurement, the shorting blocks should not be used. The inherent inductance of the path length, of say and 0805 chip, is compensated out of the system. This is demonstrated in Figure 3 for an 0805, 0.1μF capacitor. Notice that the resonant frequency is shifted by 4.63 MHz, or 23%. Since the capacitance is identical, using equation [2]

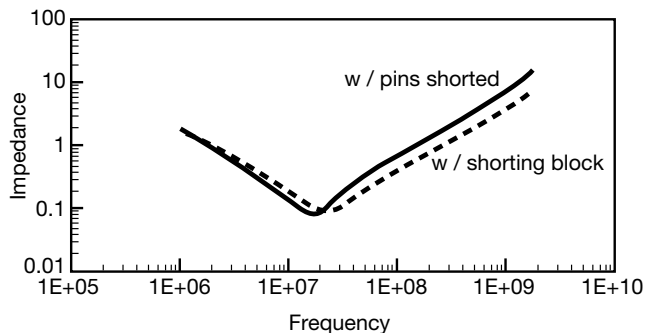$$\omega_1 = \frac{1}{\sqrt{L_1 C}} \ , \ \omega_2 = \frac{1}{\sqrt{L_2 C}} \qquad [3a]$$

Figure 3. Shift in resonant frequency caused by using a shorting block in fixture compensation of HP16192A.

$$\frac{L_1}{L_2} = \frac{\omega_2^2}{\omega_1^2} \qquad [3b]$$

This implies that the ratio of L_1:L_2 is 0.59. That is to say, if the inductance measured by shorting the pins of the HP16192A is 1nH, using the shorting block for compensation will give an inductance value of 600pH! This is quite significant and cannot be ignored. For this paper, all data is generated by shorting the pins of the HP16192A together.

One more thing to consider, the HP4291 is an impedance analyzer which measures phase and magnitude. Only the real and imaginary part of the impedance can be calculated exactly. Referring to Figure 1, the impedance of a MLCC is

$$Z = R + j\left(\omega L - \frac{1}{\omega C}\right) \qquad [4]$$

The real part being R and the imaginary part $\omega L - \frac{1}{\omega C}$. One cannot possibly separate the inductance and capacitance from the reactance, one equation, two unknowns. Fortunately, one of the terms, inductive or capacitive, becomes much smaller than the other as the frequency moves away from resonance. That is to say as

$$\omega > \omega_{res}, \ \omega L >> \frac{1}{\omega C} \qquad [5]$$

For this paper, all inductance numbers cited are taken from the 1 GHz measurement point. This frequency is far enough from resonance that the capacitive term is much smaller than the inductive term.

III. Results

All data was taken in one sitting, with the same calibration. This was done to ensure that even if the calibration was off, the relative change in inductance from case size to case size would remain intact. Figure 4 shows the impedance curves of four different case sizes with the same capacitance values of 0.1µF.
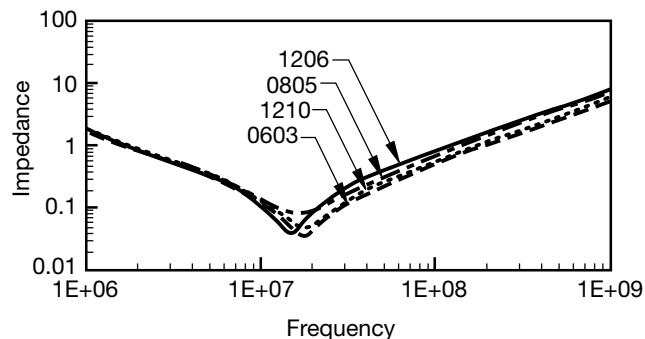

Figure 4. Impedance curves for 0.1µF capacitors.

Using the data from Figure 4, the typical inductance values are calculated to be:

MLCC Chip Size	Inductance (pH)
0603	870
0805	1050
1206	1200
1210	980

Table 1. Inductance values for 0.1µF MLCC.

It should be noted that error on a 10 piece sample run was ±7.4% across the entire range of chip sizes.

The next measurement set was to determine if the inductance value changed when more electrodes were used in a given package. In other words, is the inductance constant for different values of capacitance. Figure 5 shows the results for a 1206 package. All one needs to do is examine the impedance lines at the upper frequency limit to notice that the inductance does not vary by package type. After running 10 pieces of each value, the inductance number never differentiated by more than ±10%.
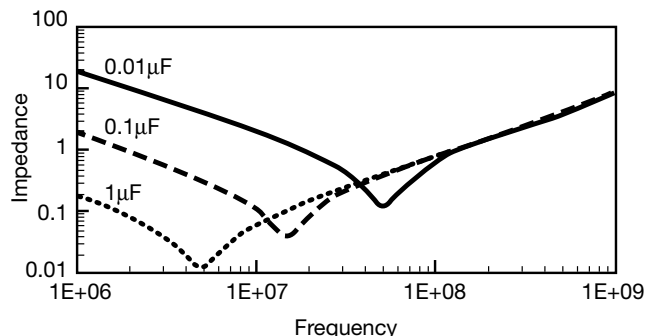

Figure 5. 1206, X7R impedance curves for a variety of capacitance values.

A variety of techniques have been employed to lower the parasitic inductance of MLCCs. The first method used was to terminate the MLCC along the long edges, thus turning a 1206 into an 0612. Figure 6 shows the comparison of a 0.1µF capacitors in both the 1206 and 0612 forms. Table 2 list the measured inductance values for both the 0612 and 0508.
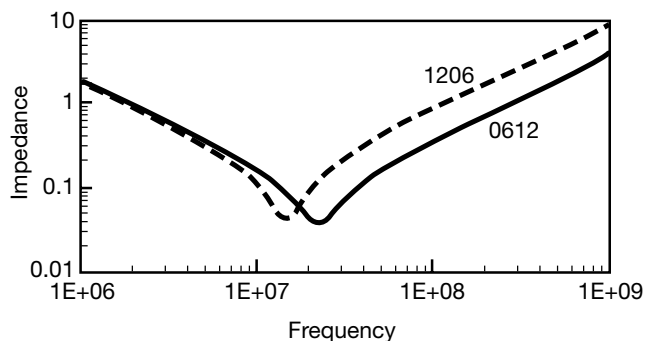
Figure 6. Impedance comparison of 1206 and 0612 form factors.

Chip Style	Inductance (pH)
0612	610
0508	600

Table 2. Inductance values of low inductance chips.

Once all of this information was compiled, an exponential curve fit was performed. The fit was centered around two x variables, namely the length to width ratio (L/W) and the length from one termination to the next. The following equation was derived:

$$L = 394.727 \times 1.052^{\wedge}L \times 1.317^{\wedge}(L/W) \quad [6]$$

Table 3 shows the difference between the curve fit and the measured data. The error is never greater than 12.4%, with the worst case being the 0805.

Chip Style	L/W	L	Fit	Measured
1210	1.2	12	1010	980
1206	2	12	1255	1250
0805	1.6	8	920	1050
0603	2	6	925	870
0612	0.5	6	615	610
0508	0.625	5	605	600

Table 3. Comparison of measured and fitted inductance values.

The model allows us to consider the inductance of future devices, such as an 0306, which yields an inductance value of 527 pH.

IV. Conclusions

This paper emphasizes the importance of a proper calibration method when attempting to calculate the parasitic inductance of surface mount capacitors. A curve fitting scheme is also highlighted as an aide to predetermine inductance values for various dimensions of MLCCs.