Am25LS23

8-Bit Shift/Storage Register with Synchronous Clear

DISTINCTIVE CHARACTERISTICS

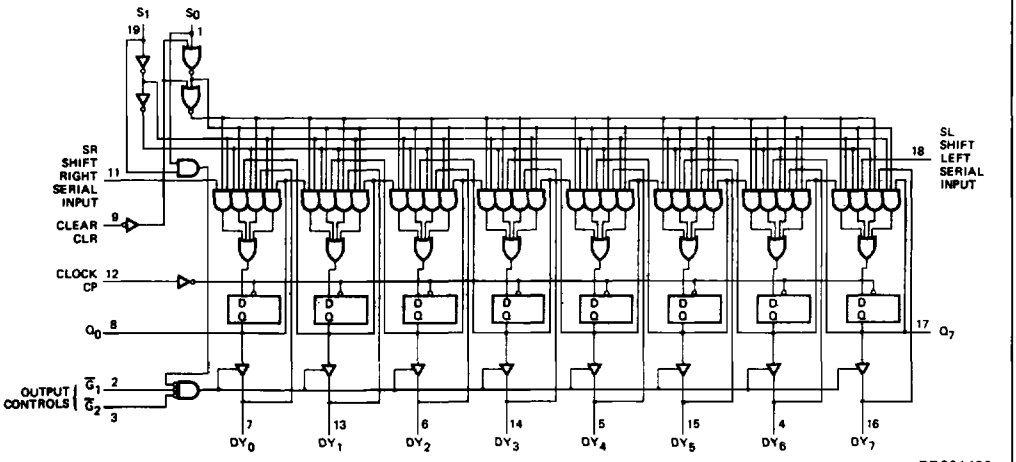
- Synchronous clear
- Three-state outputs
- Common input/output pins
- Cascadable shifting
- Second sourced by T.I. as 54LS/74LS323

GENERAL DESCRIPTION

The Am25LS23 is an 8-bit universal shift/storage register with 3-state outputs. The function is similar to the Am25LS299 with the exception of a synchronous clear function. Parallel load inputs and register outputs are multiplexed to allow the use of a 20-pin package. Separate continuous outputs are also provided for flip-flops Q_0 and Q_7.

Four modes of operation are possible – Hold (store), Shift-left, Shift-right and Load Data. The Am25LS23 has a typical shift frequency of 50MHz. The Am25LS23 is packaged in a standard 20-pin package.

BLOCK DIAGRAM



BD001480

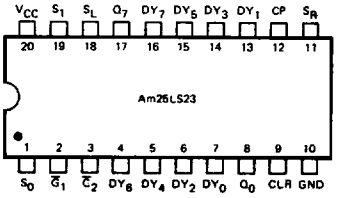
RELATED PRODUCTS

Part No.	Description
Am25LS22	8-Bit Serial/Parallel Register

03661B

Refer to Page 13-1 for Essential Information on Military Devices

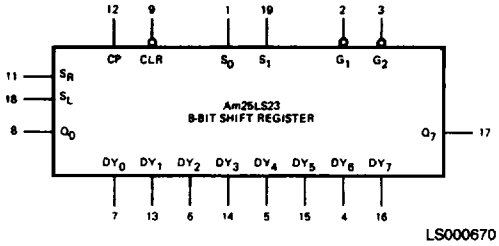
CONNECTION DIAGRAM
Top View



CD001760

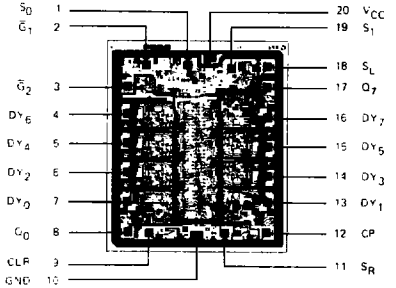
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



LS000670

METALLIZATION AND PAD LAYOUT



DIE SIZE: 0.096" x 0.112"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

Am25LS23 **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D – 20-pin CERDIP
  - F – 20-pin flatpak
  - P – 20-pin plastic DIP
  - X – Dice
- **Am25LS23** — Device type
  - 8-Bit Shift Storage Register
  - With Synchronous Clear

Valid Combinations	
Am25LS23	PC DC, DM FM XC, XM

Valid Combinations

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

9

PIN DESCRIPTION

Pin No.	Name	I/O	Description
11	S_R	I	Shift right data input to Q_7.
18	S_L	I	Shift left data input to Q_0.
9	Clear	I	Active LOW synchronous input forcing the Q_0 through Q_7 register to see LOW conditions, visable only if outputs are enabled.
12	Clock	I	A LOW-to-HIGH transition will result in the register changing state to next state as described by mode and input data condition.
1, 19	S_0, S_1	I	Mode selection control lines used to control input (output during load) conditions.
2, 3	$\overline{G}_1$, $\overline{G}_2$	I	Active LOW input to control three-state output in active LOW AND configuration.
8, 17	Q_0, Q_7	O	The only two direct outputs; used to cascade shift operations.
7, 13, 6, 14, 5, 15, 4, 16	$DY_0 - DY_7$	I/O	Input/Output line dependent on mode and output control. Input only with mode select LOAD. Output in all other modes but subject to output select ($\overline{G}_1$, $\overline{G}_2$).

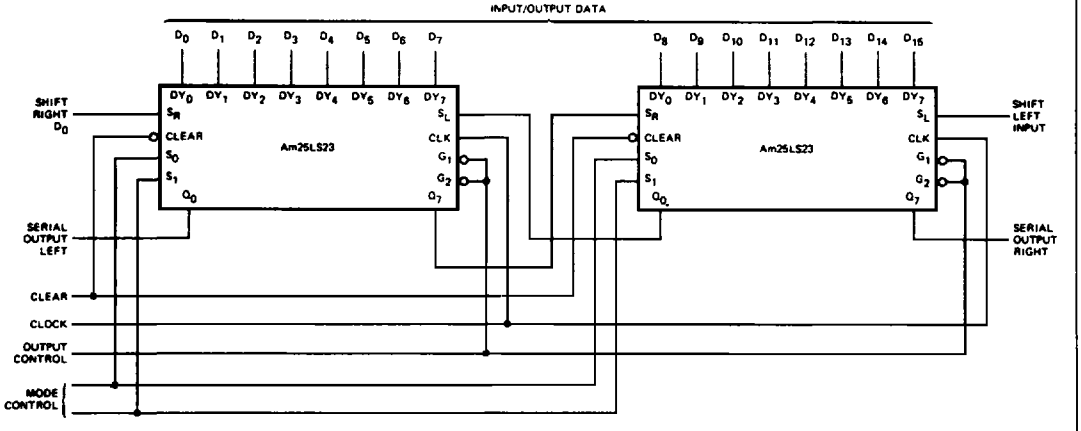
TRUTH TABLE

FUNCTION		INPUTS								OUTPUTS		INPUTS/OUTPUTS							
		S_R	S_L	CLEAR	CLOCK	S_0	S_1	$\overline{G}_1$	$\overline{G}_2$	Q_0	Q_7	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7
Clear		X	X	L	↑	(Note 1)		L	L	L	L	L	L	L	L	L	L	L	L
Output Control		X	X	X	X	X	X	H	L	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	L	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
		X	X	X	X	X	X	H	H	NC	NC	Z	Z	Z	Z	Z	Z	Z	Z
MODE	Hold	X	X	H	X	L	L	L	L	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC
	Load (Note 2)	X	X	H	↑	H	H	L	L	A	H	A	B	C	D	E	F	G	H
	Shift Right	L	X	H	↑	H	L	L	L	L	DY_6	L	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
	Shift Right	H	X	H	↑	H	L	L	L	H	DY_6	H	DY_0	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6
	Shift Left	X	L	H	↑	L	H	L	L	DY_1	L	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	L
	Shift Left	X	H	H	↑	L	H	L	L	DY_1	H	DY_1	DY_2	DY_3	DY_4	DY_5	DY_6	DY_7	H

L = LOW Z = High Impedance ↑ = Transition LOW-to-HIGH
H = HIGH X = Don't Care NC = No Change

Notes: 1. Either LOW to observe outputs.
2. In this mode DY_1 are inputs.

APPLICATION



AF001110

16-Bit Cascaded Parallel Load/Unload Shift Right/Left Register.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
(Ambient) Temperature Under Bias ... −55°C to +125°C
Supply Voltage to Ground Potential
Continuous ..... −0.5V to +7.0V
DC Voltage Applied to Outputs For
HIGH Output State ..... −0.5V to +V_{CC} max
DC Input Voltage S_0, S_1, $\overline{G}_1$, $\overline{G}_2$,
CLR, CP) ..... −0.5V to +7.0V
DC Input Voltage (Others) ..... −0.5V to +5.5V
DC Output Current, Into Outputs 30mA
DC Input Current ..... −30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameters	Description	Test Conditions (Note 2)				Min	Typ (Note 1)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{OL}	Q_0, Q_7	I_{OH} = −440μA	MIL	2.5			Volts
					COM'L	2.7			
			DY_0-DY_7	MIL, I_{OH} = −1.0mA		2.4			
				COM'L, I_{OH} = −2.6mA		2.4			
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OL} = 4.0mA			0.25	0.4	Volts
				I_{OL} = 8.0mA			0.35	0.45	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs				2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			MIL			0.7	Volts
					COM'L			0.8	
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA						−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V			S_0, S_1			−0.8	mA
					All others			−0.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V (Except DY_i)			S_0, S_1			40	μA
					All others			20	
I_I	Input HIGH Current	V_{CC} = MAX., (Except DY_i)	V_{IN} = 7V	S_0, S_1				0.2	mA
				$\overline{G}_1$, $\overline{G}_2$, CLR, CP				0.1	
			V_{IN} = 5.5V	Others				0.1	
I_{OZ}	Off-State (High Impedance) Output Current	V_{CC} = MAX.			V_O = 0.4V			−100	μA
					V_O = 2.4V			40	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = MAX.				−15		−85	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 4)					38	60	mA

Notes: 1. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
2. For conditions shown as MIN. or MAX., use the appropriate value specified under Operating Ranges for the applicable device type.
3. Not more than one output should be shorted at a time.
4. I_{CC}-measured with clock input HIGH and output controls HIGH.

SWITCHING CHARACTERISTICS (T_A = +25°C, V_{CC} = 5.0V)

Parameters	Description	Test Conditions	Min	Typ	Max	Units
t_{PLH}	Clock to Q_0 or Q_7	C_L = 15pF, R_L = 2.0kΩ		18	26	ns
t_{PHL}				23	28	
t_{PLH}	Clock to DY_i			18	26	ns
t_{PHL}				21	28	
t_s	S_1, S_0 Set-up Prior to Clock		12			ns
t_s	DY_i or S_R, S_L Set-up Prior to Clock		12			ns
t_{PW}	Pulse Width (Clock)		15			ns
t_s	Clear to Clock		15			ns
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i			18	30	ns
t_{ZL}				20	30	
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$, to DY_i	C_L = 5.0pF, R_L = 2.0kΩ		22	33	ns
t_{HZ}				16	23	
f_{max}	Maximum Clock Frequency (Note 1)		35	50		MHz

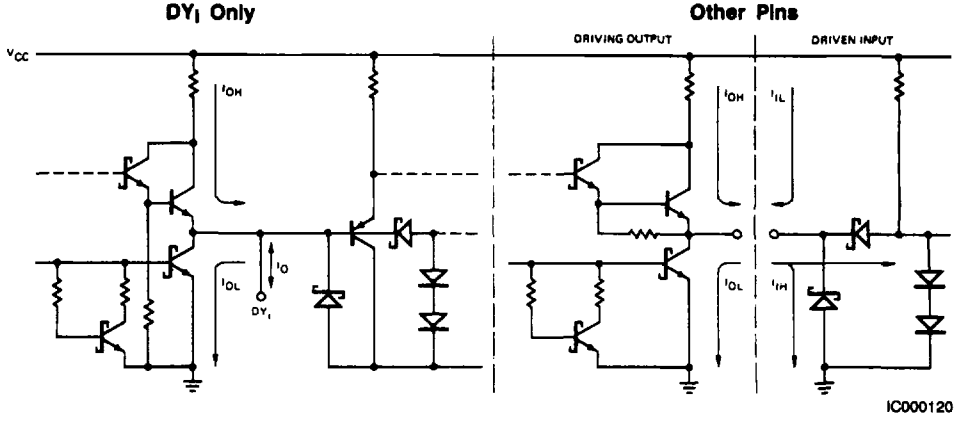
Note 1. Per industry convention, f_{max} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.

SWITCHING CHARACTERISTICS over operating range unless otherwise specified*

Parameters	Description	Test Conditions	COMMERCIAL Am25LS		MILITARY Am25LS		Units
			Min	Max	Min	Max	
t_{PLH}	Clock to Q_0 or Q_7	C_L = 50pF, R_L = 2.0KΩ		38		44	ns
t_{PHL}				40		47	
t_{PLH}	Clock to DY_i			38		44	ns
t_{PHL}				40		47	
t_s	S_1, S_0 Set-up Prior to Clock		20		23		ns
t_s	DY_i, or S_R, S_L Set-up Prior to Clock		20		23		ns
t_{pw}	Pulse Width (Clock)		24		27		ns
t_s	Clear to Clock		24		27		ns
t_{ZH}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i			43		50	ns
t_{ZL}				43		50	
t_{LZ}	S_1, S_0, $\overline{G}_1$, $\overline{G}_2$ to DY_i	C_L = 5.0pF, R_L = 2.0KΩ		43		50	ns
t_{HZ}				30		35	
f_{max}	Maximum Clock Frequency (Note 1)		26		23		MHz

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.