IGLOO2 FPGAs

Microsemi's IGLOO®2 FPGAs integrate fourth generation flash-based FPGA fabric and high-performance communications interfaces on a single chip. The IGLOO2 family is the industry's lowest power, most reliable and highest security programmable logic solution. This next generation IGLOO2 architecture offers up to 3.6X gate count implemented with 4-input look-up table (LUT) fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and mathblocks for digital signal processing (DSP). High speed serial interfaces include PCI EXPRESS® (PCIe®), 10 Gbps attachment unit interface (XAUI) / XGMII extended sublayer (XGXS) plus native serialization/deserialization (SERDES) communication, while double data rate 2 (DDR2)/DDR3 memory controllers provide high speed memory interfaces.

IGLOO2 Family

High-Performance FPGA

- Efficient 4-Input LUTs with Carry Chains for High-Performance and Low Power
- Up to 236 Blocks of Dual-Port 18 Kbit SRAM (Large SRAM) with 400 MHz Synchronous Performance (512 x 36, 512 x 32, 1kbit x 18, 1kbit x 16, 2kbit x 9, 2kbit x 8, 4kbit x 4, 8kbit x 2, or 16kbit x 1)
- Up to 240 Blocks of Three-Port 1 Kbit SRAM with 2 Read Ports and 1 Write Port (micro SRAM)
- High-Performance DSP Signal Processing
  - Up to 240 Fast Mathblocks with 18 x 18 Signed Multiplication, 17 x 17 Unsigned Multiplication and 44-Bit Accumulator

High Speed Serial Interfaces

- Up to 16 SERDES Lanes, Each Supporting:
  - XGXS/XAUI Extension (To Implement a 10 Gbps (XGMII) Ethernet PHY Interface)
  - Native SERDES Interface Facilitates Implementation of Serial RapidIO in Fabric or an SGMII Interface to a soft Ethernet MAC
  - PCI Express (PCIe) Endpoint Controller
    - x1, x2, x4 Lane PCI Express Core
    - Up to 2 Kbytes Maximum Payload Size
    - 64-/32-Bit AXI/AHB Master and Slave Interfaces to the Application Layer

High Speed Memory Interfaces

- Up to 2 High Speed DDRx Memory Controllers
  - HPMS DDR (MDDR) and Fabric DDR (FDDR) Controllers
  - Supports LPDDR/DDR2/DDR3
  - Maximum 333 MHz Clock Rate
  - SECDED Enable/Disable Feature
  - Supports Various DRAM Bus Width Modes, x8, x9, x16, x18, x32, x36
  - Supports Command Reordering to Optimize Memory Efficiency
  - Supports Data Reordering, Returning Critical Word First for Each Command
- SDRAM Support through a Soft SDRAM Memory Controller

High-Performance Memory Subsystem

- 64 KB Embedded SRAM (eSRAM)
- Up to 512 KB Embedded Nonvolatile Memory (eNVM)
- One SPI/COMM_BLK
- DDR Bridge (2 Port Data R/W Buffering Bridge to DDR Memory) with 64-Bit AXI Interface
- Non-Blocking, Multi-Layer AHB Bus Matrix Allowing Multi-Master Scheme Supporting 5 Masters and 7 Slaves

- Two AHB/APB Interfaces to FPGA Fabric (Master/Slave Capable)
- Two DMA Controllers to Offload Data Transactions
  - 8-Channel Peripheral DMA (PDMA) for Data Transfer Between HPMS Peripherals and Memory
- High-Performance DMA (HPDMA) for Data Transfer Between eSRAM and DDR Memories

Clocking Resources

- Clock Sources
  - High Precision 32 KHz to 20 MHz Main Crystal Oscillator
  - 1 MHz Embedded RC Oscillator
  - 50 MHz Embedded RC Oscillator
- Up to 8 Clock Conditioning Circuits (CCCs) with Up to 8 Integrated Analog PLLs
  - Output Clock with 8 Output Phases and 45° Phase Difference (Multiply/Divide, and Delay Capabilities)
- Frequency: Input 1 to 200 MHz, Output 20 to 400 MHz

Operating Voltage and I/Os

- 1.2 V Core Voltage
- Multi-Standard User I/Os (MSIO/MSIOD)
  - LVTTL/LVCMOS 3.3 V (MSIO only)
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
  - DDR (SSTL2_1, SSTL2_2)
  - DDR2 (SSTL18_1, SSTL18_2)
  - LVDS, MLVDS, Mini-LVDS, RSDS Differential Standards
  - PCI
  - LVPECL (receiver only)
- DDR I/Os (DDRIO)
  - DDR, DDR2, DDR3, LPDDR, SSTL2, SSTL18, HSTL
  - LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V
- Market Leading Number of User I/Os with 5G SERDES

Security

- Design Security Features (available on all devices)
  - Intellectual Property (IP) Protection through Unique Security Features and Use Models New to the PLD Industry
  - Encrypted User Key and Bitstream Loading, Enabling Programming in Less-Trusted Locations
  - Supply-Chain Assurance Device Certificate
  - Enhanced Anti-Tamper Features
  - Zeroization
- Data Security Features (available on premium devices)
  - Non-Deterministic Random Bit Generator (NRBG)
  - User Cryptographic Services (AES-256, SHA-256, Elliptical Curve Cryptographic (ECC) Engine)
  - User Physically Unclonable Function (PUF) Key Enrollment and Regeneration
  - CRI Pass-Through DPA Patent Portfolio License
  - Hardware Firewalls Protecting Microcontroller Subsystem (HPMS) Memories

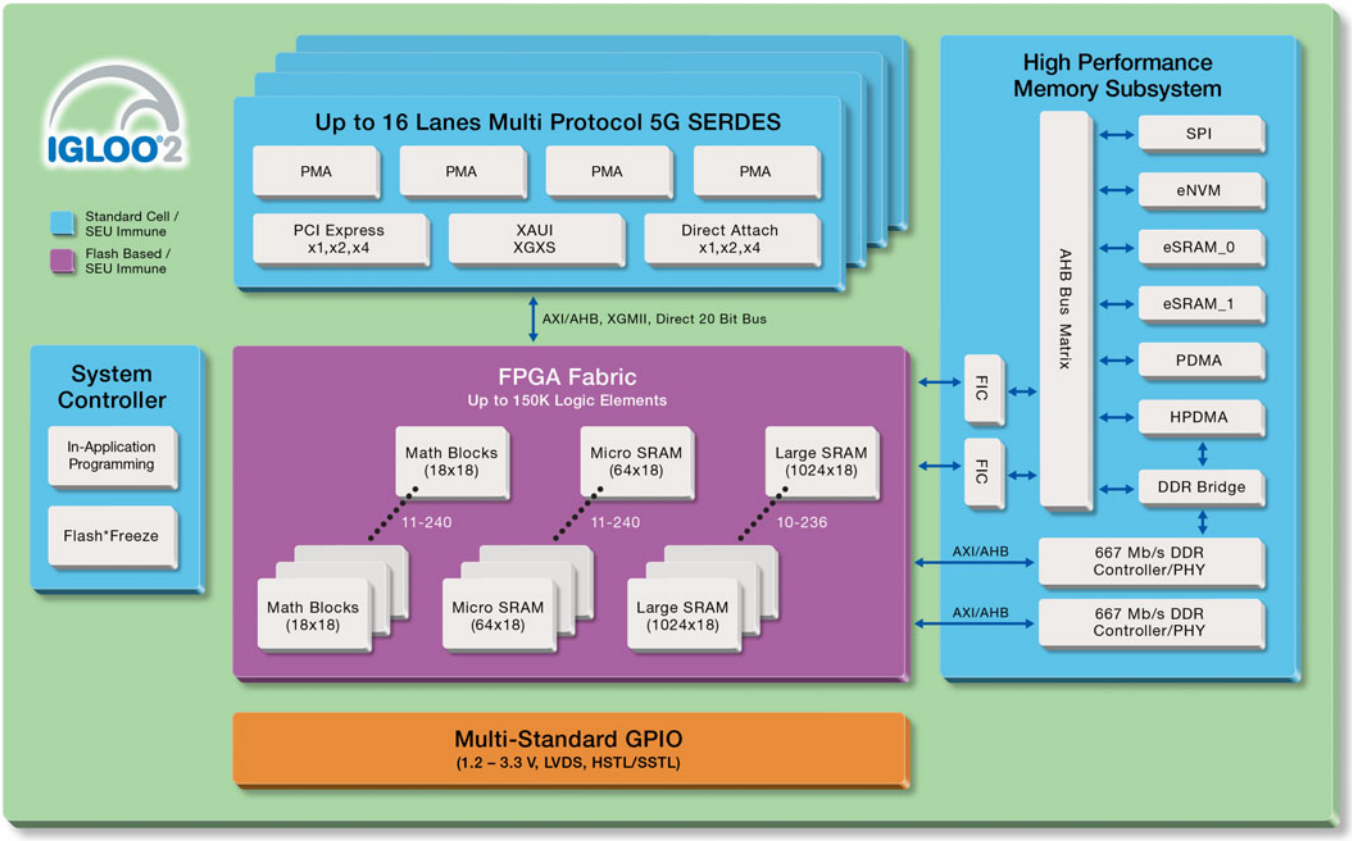
Reliability

- Single Event Upset (SEU) Immune
  - Zero FIT FPGA Configuration Cells
- Junction Temperature: 125°C – Military Temperature, 100°C – Industrial Temperature, 85°C – Commercial Temperature
- Single Error Correct Double Error Detect (SECDED) Protection on the Following:
  - Embedded Memory (eSRAMs)
  - PCIe Buffer
  - DDR Memory Controllers with Optional SECDED Modes
- Buffers Implemented with SEU Resistant Latches on the Following:
  - DDR Bridges (HPMS, MDDR, FDDR)
  - SPI FIFO
- NVM Integrity Check at Power-Up and On-Demand
- No External Configuration Memory Required—Instant-On, Retains Configuration When Powered Off

Low Power

- Low Static and Dynamic Power
  - Flash*Freeze Mode for Fabric
- Power as low as 13 mW/Gbps per lane for SERDES devices
- Up to 25% lower total power than competing devices

IGLOO2 FPGA Block Diagram



Acronyms

AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AXI	Advanced eXtensible Interface
COMM_BLK	Communication Block
DDR	Double Data Rate
DPA	Differential Power Analysis
ECC	Elliptical Curve Cryptography
EDAC	Error Detection And Correction
FDDR	DDR2/3 Controller in FPGA Fabric
FIC	Fabric Interface Controller
HPMS	High-Performance Memory Subsystem
IAP	In-Application Programming
MACC	Multiply-Accumulate
MDDR	DDR2/3 Controller in HPMS
SECDED	Single Error Correct Double Error Detect
SEU	Single Event Upset
SHA	Secure Hashing Algorithm
XAUI	10 Gbps Attachment Unit Interface
XGMII	10 Gigabit Media Independent Interface
XGXS	XGMII Extended Sublayer

Table 1 • IGLOO2 FPGA Product Family

Features		M2GL005	M2GL010(T)	M2GL025(T)	M2GL050(T)	M2GL090(T)	M2GL100(T)	M2GL150(T)
Logic/DSP	Maximum Logic Elements (4LUT + DEF)*	6,060	12,084	27,696	56,340	86,316	99,512	146,124
	Mathblocks (18x18)	11	22	34	72	84	160	240
	PLLs and CCCs	2		6			8	
	SPI/HPDMA/PDMA	1 each						
	Fabric Interface Controllers (FIC)	1			2			
Memory	eNVM (kbytes)	128	256			512		
	LSRAM 18K Blocks	10	21	31	69	109	160	236
	uSRAM 1K Blocks	11	22	34	72	112	160	240
	eSRAM (kbytes)	64						
	Total RAM (kbits)	703	912	1104	1826	2586	3552	5000
High Speed	DDR Controllers	1x18			2x36	1x18	2x36	
	SERDES Lanes (T)	0	4		8	4	8	16
	PCIe Endpoints	0	1		2			4
User I/O	MSIO (3.3 V)	115	123	157	139	309	292	292
	MSIOD (2.5 V)	28	40	40	62	40	106	106
	DDRIO (2.5 V)	66	70	70	176	76	176	176
	Total User I/Os	209	233	267	377	425	574	574

*Notes: *Total Logic may vary based on utilization of DSP and memories in your design. See the IGLOO2 Fabric UG for details.*
**Feature availability is package dependent, see Table 3.*

I/Os Per Package

Table 2 • I/Os per Package and Package Options

Package Options																		
Type	**FCS325**		**VF256**		**VF400**		**FCV484**		**VQ144**		**FG484**		**FG676**		**FG896**		**FC1152**	
Pitch (mm)	0.5		0.8		0.8		0.8		0.5		1.0		1.0		1.0		1.0	
Length x Width (mm)	11x11		14x14		17x17		19x19		20x20		23x23		27x27		31x31		35x35	
Device	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes	I/O	Lanes
M2GL005					171				83[1]		209							
M2GL010 (T)			148[1]	2[1]	195	4			75[1]		233	4						
M2GL025 (T)	180	2	148[1]	2[1]	207	4					267	4						
M2GL050 (T)	200	2			207	4					267	4			377	8		
M2GL090 (T)[2]	200[1]	4[1]									267	4	425	4				
M2GL100 (T)							273[1]	4[1]									574	8
M2GL150 (T)							273[1]	4[1]									574	16

Notes:
1. *Preliminary*
2. *090 FCS325 is 11x13.5 package dimension*

Features per Device and Package Combination

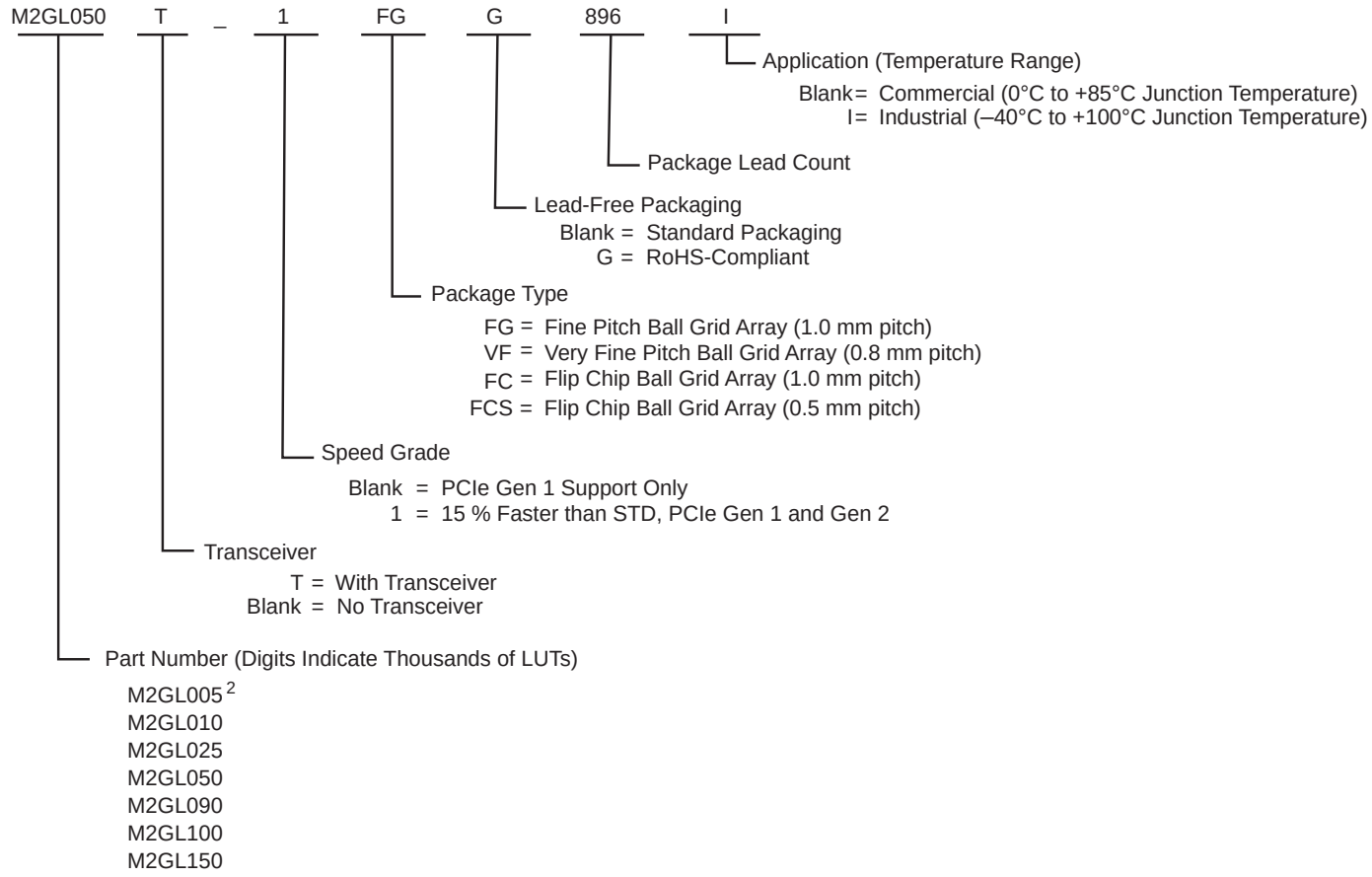
Table 3 • Features per Device/Package Combination

Features										
Package	**Devices**	**MDDR**	**FDDR**	**Crystal Oscillators**	**5G SERDES Lanes**	**PCIe Endpoints**	**MSIO (3.3 V Max)**	**MSIOD (2.5 V Max)**	**DDRIO (2.5 V Max)**	**Total User I/O**
VQ144[5]	M2GL005	-	-	2	-	-	TBD	TBD	TBD	83
	M2GL010	-	-	2	-	-	TBD	TBD	TBD	75
FCS325	M2GL025(T)	x18[1]	-	2	2	1	94	22	64	180
	M2GL050 (T)	x18[2]	-	1	2	1	90	22	88	200
VF400	M2GL005	x18[1]	-	2	-	-	79	28	64	171
	M2GL010 (T)	x18[1]	-	2	4	1	99	32	64	195
	M2GL025 (T)	x18[1]	-	2	4	1	111	32	64	207
	M2GL050 (T)	x18[2]	-	1	4	1	87	32	88	207
FCV484[5]	M2GL100 (T)	x18[1]	x18[1]	2	4	2	TBD	TBD	TBD	273
	M2GL150 (T)	x18[1]	x18[1]	2	4	2	TBD	TBD	TBD	273
FG484	M2GL005	x18[1]	-	2	-	-	115	28	66	209
	M2GL010 (T)	x18[1]	-	2	4	1	123	40	70	233
	M2GL025 (T)	x18[1]	-	2	4	1	157	40	70	267
	M2GL050 (T)	x18[2]	-	1	4	1	105	40	122	267
	M2GL090 (T)	x18[1]	-	2	4	2	157	40	70	267
FG676	M2GL090 (T)	x18[1]	-	2	4	2	309	40	76	425
FG896	M2GL050 (T)	x36[4]	x36[4]	1	8	2	139	62	176	377
FC1152	M2GL100 (T)	x36[3]	x36[3]	2	8	2	292	106	176	574
	M2GL150 (T)	x36[3]	x36[3]	2	16	4	292	106	176	574

Notes:

1. *DDR supports x18, x16, x9, and x8 modes*
2. *DDR supports x18 and x16 modes*
3. *DDR supports x36, x32, x18, x16, x9, and x8 modes*
4. *DDR supports x36, x32, x18, and x16 modes*
5. *Preliminary*

IGLOO2 Ordering Information



Notes:

1. *Design and Data Security Devices (S) are only available in -1 Industrial speed grades*
2. *M2GL005 device not available with Transceivers*

IGLOO2 Device Status

Refer to the IGLOO2 Datasheet for device status.

IGLOO2 Datasheet and Pin Descriptions

The datasheet and pin descriptions are published separately:

IGLOO2 Datasheet

IGLOO2 Pin Descriptions

1 – IGLOO2 Device Family Overview

Microsemi's IGLOO2 FPGAs integrate fourth generation flash-based FPGA fabric and high-performance communications interfaces on a single chip. The IGLOO2 family is the industry's lowest power, highest reliability and most secure programmable logic solution. This next generation IGLOO2 architecture offers up to 3.6X gate count, implemented with 4-input look-up table (LUT) fabric with carry chains, giving 2X performance, and includes multiple embedded memory options and mathblocks for DSP. High speed serial interfaces enable PCIe, XAUI / XGXS plus native SERDES communication while DDR2/DDR3 memory controllers provide high speed memory interfaces.

High-Performance FPGA Fabric

Built on 65 nm process technology, the IGLOO2 FPGA fabric is composed of four building blocks: the logic module, the large SRAM, the micro SRAM and the mathblock. The logic module is the basic logic element and has advanced features:

- A fully permutable 4-input LUT (look-up table) optimized for lowest power
- A dedicated carry chain based on carry look-ahead technique
- A separate flip-flop which can be used independently from the LUT

The 4-input look-up table can be configured either to implement any 4-input combinatorial function or to implement an arithmetic function where the LUT output is XORed with carry input to generate the sum output.

Dual-Port Large SRAM (LSRAM)

Large SRAM (RAM1Kx18) is targeted for storing large memory for use with various operations. Each LSRAM block can store up to 18,432 bits. Each RAM1Kx18 block contains two independent data ports: Port A and Port B. The LSRAM is synchronous for both Read and Write operations. Operations are triggered on the rising edge of the clock. The data output ports of the LSRAM have pipeline registers which have control signals that are independent of the SRAM's control signals.

Three-Port Micro SRAM (uSRAM)

Micro SRAM (RAM64x18) is the second type of SRAM which is embedded in the fabric of IGLOO2 devices. RAM64x18 uSRAM is a 3-port SRAM; it has two read ports (Port A and Port B) and one write port (Port C). The two read ports are independent of each other and can perform Read operations in both synchronous and asynchronous modes. The write port is always synchronous. The uSRAM block is approximately 1 KB 152 bits) in size. These uSRAM blocks are primarily targeted for building embedded FIFOs to be used by any embedded fabric masters.

Mathblocks for DSP Applications

The fundamental building block in any digital signal processing algorithm is the multiply-accumulate function. The IGLOO2 device implements a custom 18x18 Multiply-Accumulate (18x18 MACC) block for efficient implementation of complex DSP algorithms such as finite impulse response (FIR) filters, infinite impulse response (IIR) filters, and fast Fourier transform (FFT) for filtering and image processing applications.

Each mathblock has the following capabilities:

- Supports 18x18 signed multiplications natively (A[17:0] x B[17:0])
- Supports dot product; the multiplier computes:

  $(A[8:0] \times B[17:9] + A[17:9] \times B[8:0]) \times 2^9$
- Built-in addition, subtraction, and accumulation units to combine multiplication results efficiently

In addition to the basic MACC function, DSP algorithms typically need small amounts of RAM for coefficients and larger RAMs for data storage. IGLOO2 micro RAMs are ideally suited to serve the needs of coefficient storage while the large RAMs are used for data storage.

High Speed Serial Interfaces

SERDES Interface

IGLOO2 FPGA has up to four 5 Gbps SERDES transceivers, each supporting the following:

- 4 SERDES/PCS lanes
- The native SERDES interface facilitates implementation of Serial RapidIO (SRIO) in fabric or a SGMII interface for a soft Ethernet MAC

PCI Express (PCIe)

PCIe is a high speed, packet-based, point-to-point, low pin count, serial interconnect bus. The IGLOO2 family has two hard high-speed serial interface blocks. Each SERDES block contains a PCIe system block. The PCIe system is connected to the SERDES block and following are the main features supported:

- Supports x1, x2, and x4 lane configuration
- Endpoint configuration only
- PCI Express Base Specification Revision 2.0
- 2.5 and 5.0 Gbps compliant
- Embedded receive (2 KB), transmit (1 KB) and retry (1 KB) buffer dual-port RAM implementation
- Up to 2 kbytes maximum payload size
- 64-bit AXI or 32-bit/64-bit AHBL Master and Slave interface to the application layer
- 32-bit APB interface to access configuration and status registers of PCIe system
- Up to 3 x 64 bit base address registers
- 1 virtual channel (VC)

XAUI/XGXS Extension

The XAUI/XGXS extension allows the user to implement a 10 Gbps (XGMII) Ethernet PHY interface by connecting the XGMII fabric interface through an appropriate soft IP block in the fabric.

High Speed Memory Interfaces: DDRx Memory Controllers

There are up to two DDR subsystems, MDDR (HPMS DDR) and FDDR (fabric DDR) present in IGLOO2 devices. Each subsystem consists of a DDR controller, PHY, and a wrapper. The MDDR has an interface to/from the HPMS and fabric, and FDDR provides an interface to/from the fabric.

The following are the main features supported by the FDDR and MDDR:

- Support for LPDDR, DDR2, and DDR3 memories
- Simplified DDR command interface to standard AMBA AXI/AHB interface
- Up to 667 Mbps (333 MHz double data rate) performance
- Supports 1, 2, or 4 ranks of memory
- Supports different DRAM bus width modes: x8, x9, x16, x18, x32, and x36
- Supports DRAM burst length of 2, 4, or 8 in full bus-width mode; supports DRAM burst length of 2, 4, 8, or 16 in half bus-width mode
- Supports memory densities up to 4 GB
- Supports a maximum of 8 memory banks
- SECDED enable/disable feature
- Embedded physical interface (PHY)
- Read and Write buffers in fully associative CAMs, configurable in powers of 2, up to 64 Reads plus 64 Writes
- Support for dynamically changing clock frequency while in self-refresh
- Supports command reordering to optimize memory efficiency
- Supports data reordering, returning critical word first for each command

MDDR Subsystem

The MDDR subsystem has two interfaces to the DDR. One is an AXI 64-bit bus from the DDR bridge within the HPMS. The other is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the MDDR subsystem after reset. This APB configuration bus is mastered by a master in the FPGA fabric. Support for 3.3 V Single Data Rate DRAMs (SDRAM) can be obtained by instantiating a soft AHB or AXI SDRAM memory controller in the FPGA fabric and connecting I/O ports to 3.3 V MSIO.

FDDR Subsystem

The FDDR subsystem has one interface to the DDR. This is a multiplexed interface from the FPGA fabric, which can be configured as either a single AXI 64-bit bus or two 32-bit AHB-Lite buses. There is also a 16-bit APB configuration bus, which is used to initialize the majority of the internal registers within the FDDR subsystem after reset. This APB configuration bus can be mastered by a master in the FPGA fabric.

High-Performance Memory Subsystem (HPMS)

The high-performance memory subsystem (HPMS) embeds two separates 32 kbyte SRAM blocks that have optional SECDED capabilities (32 kbytes with SECDED enabled, 40 kbytes with SECDED disabled), up to two separate 256 kbyte eNVM (flash) blocks, and two separate DMA controllers for fast DMA user logic offloading. The HPMS provides multiple interfacing options to the FPGA fabric in order to facilitate tight integration between the HPMS and user logic in the fabric.

DDR Bridge

The DDR bridge is a data bridge between two AHB bus masters and a single AXI bus slave. The DDR bridge accumulates AHB writes into write combining buffers prior to bursting out to external DDR memory. The DDR bridge also includes read combining buffers, allowing AHB masters to efficiently read data from the external DDR memory from a local buffer. The DDR bridge optimizes reads and writes from multiple masters to a single external DDR memory. Data coherency rules between the masters and the external DDR memory are implemented in hardware. The DDR bridge contains two write combining / read buffers. All buffers within the DDR bridge are implemented with SEU tolerant latches and are not subject to the single event upsets (SEUs) that SRAM exhibits. IGLOO2 devices implement three DDR bridges in the HPMS, FDDR, and MDDR subsystems.

AHB Bus Matrix (ABM)

The AHB bus matrix (ABM) is a non-blocking, AHB-Lite multi-layer switch, supporting 4 master interfaces and 8 slave interfaces. The switch decodes access attempts by masters to various slaves, according to the memory map and security configurations. When multiple masters are attempting to access a particular slave simultaneously, an arbiter associated with that slave decides which master gains access, according to a configurable set of arbitration rules. These rules can be configured by the user to provide different usage patterns to each slave. For example, a number of consecutive access opportunities to the slave can be allocated to one particular master, to increase the likelihood of same type accesses (all reads or all writes), which makes more efficient usage of the bandwidth to the slave.

Fabric Interface Controller (FIC)

The FIC block provides two separate interfaces between the HPMS and the FPGA fabric: the HPMS master (MM) and fabric master (FM). Each of these interfaces can be configured to operate as AHB-Lite or APB3. Depending on device density, there are up to two FIC blocks present in the HPMS (FIC_0 and FIC_1).

Embedded SRAM (eSRAM)

The HPMS contains two blocks of 32 KB eSRAM, giving a total of 64 KB. Having the eSRAM arranged as two separate blocks allows the user to take advantage of the parallelism that exists in the HPMS.

The eSRAM is designed for Single Error Correct Double Error Detect (SECDED) protection. When SECDED is disabled, the SRAM usually used to store SECDED data may be reused as an extra 16 KB of eSRAM.

Embedded NVM (eNVM)

The HPMS contains up to 512 KB of eNVM (64 bits wide).

DMA Engines

Two DMA engines are present in the HPMS: high-performance DMA and peripheral DMA.

High-Performance DMA (HPDMA)

The high-performance DMA (HPDMA) engine provides efficient memory to memory data transfers between an external DDR memory and internal eSRAM. This engine has two separate AHB-Lite interfaces—one to the MDDR bridge and the other to the AHB bus matrix. All transfers by the HPDMA are full word transfers.

Peripheral DMA (PDMA)

The peripheral DMA engine (PDMA) is tuned for offloading byte-intensive operations, involving HPMS peripherals, to and from the internal eSRAMs. Data transfers can also be targeted to user logic/RAM in the FPGA fabric.

APB Configuration Bus

On every IGLOO2 device memory, an APB configuration bus is present to allow the user to initialize the SERDES ASIC blocks, the fabric DDR memory controller, and user instantiated peripherals in the FPGA fabric.

Peripherals

A large number of communications and general purpose peripherals are implemented in the HPMS.

Communication Block (COMM_BLK)

The COMM block provides a UART-like communications channel between the HPMS and the system controller. System services are initiated through the COMM block. System services such as *Enter Flash*Freeze Mode* are initiated though this block.

SPI

The serial peripheral interface controller is compliant with the Motorola SPI, Texas Instruments synchronous serial, and National Semiconductor MICROWIRE™ formats. In addition, the SPI supports interfacing to large SPI flash and EEPROM devices by way of the slave protocol engine. The SPI controller supports both Master and Slave modes of operation.

The SPI controller embeds two 4×32 (depth × width) FIFOs for receive and transmit. These FIFOs are accessible through RX data and TX data registers. Writing to the TX data register causes the data to be written to the transmit FIFO. This is emptied by transmit logic. Similarly, reading from the RX data register causes data to be read from the receive FIFO.

Clock Sources: On-Chip Oscillators, PLLs, and CCCs

IGLOO2 devices have two on-chip RC oscillators—a 1 MHz RC oscillator and a 50 MHz RC oscillator—and the main crystal oscillator (32 KHz–20 MHz). These are available to the user for generating clocks to the on-chip resources and the logic built on the FPGA fabric array. These oscillators can be used in conjunction with the integrated user phase-locked loops (PLLs) and FAB_CCCs to generate clocks of varying frequency and phase. In addition to being available to the user, these oscillators are also used by the system controller, power-on reset circuitry, and HPMS during the Flash*Freeze mode.

IGLOO2 devices have up to eight fabric CCC (FAB_CCC) blocks and a dedicated PLL associated with each CCC to provide flexible clocking to the FPGA fabric portion of the device. The user has the freedom to use any of the eight PLLs and CCCs to generate the fabric clocks and the internal HPMS clock from the base fabric clock (CLK_BASE). There is also a dedicated CCC block for the HPMS (HPMS_CCC) and an associated PLL (MPLL) for HPMS clocking and de-skewing the CLK_BASE clock. The fabric alignment clock controller (FACC), part of the HPMS CCC, is responsible for generating various aligned clocks required by the HPMS for correct operation of the HPMS blocks and synchronous communication with the user logic in the FPGA fabric.

Highest Security Devices

Building further on the intrinsic security benefits of flash nonvolatile memory technology, the IGLOO2 family incorporates essentially all the legacy security features that made the original SmartFusion®, Fusion®, IGLOO®, and ProASIC®3 third-generation flash FPGAs and cSoCs the gold standard for secure devices in the PLD industry. In addition, the fourth-generation flash-based SmartFusion2 and IGLOO2 FPGAs add many unique design and data security features and use models new to the PLD industry.

Design Security

Design security is protecting the intent of the owner of the design, such as keeping the design and associated bitstream keys confidential, preventing design changes (insertion of Trojan Horses, for example), and controlling the number of copies made throughout the device life cycle. Design security may also be known as intellectual property (IP) protection. It is one aspect of anti-tamper (AT) protection. Design security applies to the device from initial production, includes any updates such as in-the-field upgrades, and can include decommissioning of the device at the end of its life, if desired. Good design security is a prerequisite for good data security. The following are the main design security features supported:

***Table 1-1* • Design Security Features**

Feature	M2GL005 M2GL010 M2GL025 M2GL050	M2GL090 M2GL100 M2GL150
FlashLock™ Passcode Security (256-bit)	x	x
Flexible security settings using flash lock-bits	x	x
Encrypted/Authenticated Design Key Loading	x	x
Symmetric Key Design Security (256-bit)	x	x
Design Key Verification Protocol	x	x
Encrypted/Authenticated Configuration Loading	x	x
Certificate-of-Conformance (C-of-C)	x	x
Back-Tracking Prevention (also known as, Versioning)	x	x
Device Certificate(s) (Anti-Counterfeiting)	x	x
Support for Configuration Variations	x	x
Fabric NVM and eNVM Integrity Tests	x	x
Information Services (S/N, Cert., USERCODE, and others)	x	x
Tamper Detection	x	x
Tamper Response (includes Zeroization)	x	x
ECC Public Key Design Security (384-bit)		x
Hardware Intrinsic Design Key (SRAM-PUF)		x

Reliability

IGLOO2 flash-based fabric has zero FIT configuration rate due to its single event upset (SEU) immunity, which is critical in reliability applications. The flash fabric also has the advantage that no external configuration memory is required, making the device instant-on; it retains configuration when powered off. To complement this unique FPGA capability, IGLOO2 devices add reliability to many other aspects of the device. Single Error Correct Double Error Detect (SECDED) protection is implemented on the embedded SRAM (eSRAM), and is optional on the DDR memory controllers. This means that if a one-bit error is detected, it will be corrected. Errors of more than one bit are detected only and not corrected. SECDED error signals are brought to the FPGA fabric to allow the user to monitor the status of these protected internal memories. Other areas of the architecture are implemented with latches, which are not subject to SEUs. Therefore, no correction is needed in these locations: DDR bridges (HPMS, MDDR, FDDR), SPI, and PCIe FIFOs.

Low Power

Microsemi's flash-based FPGA fabric results in extremely low power design implementation with static power on the M2GL050 device as low as 10 mW. Flash*Freeze (F*F) technology provides an ultra-low power static mode (Flash*Freeze mode) for IGLOO2 devices, with power less than 1 mW. F*F mode entry retains all the SRAM and register information and the exit from F*F mode achieves rapid recovery to active mode.

2 – Product Brief Information

List of Changes

The following table lists critical changes that were made in each revision of IGLOO2 Product Brief.

Revision	Changes	Page
Revision 5 (Dec 2013)	Tables 3-6 were combined into Table 3. Fabric Interface Controller features were added to "IGLOO2 FPGA Product Family" table. Packages VQ144 and FCV484 were added to Table 2 and Table 3.	1-V,1-IV 1-IV, 1-V
Revision 4 (Nov 2013)	The Data Security Features section, table and the Device Status table were removed. "IGLOO2 FPGA Block Diagram" was updated.	N/A,1-III
Revision 3 (Oct 2013)	Packages FCS325 and VF256 were added to "I/Os Per Package". "IGLOO2 Ordering Information" was updated. Typo fixed on "IGLOO2 FPGA Block Diagram".	1-IV,1-III
Revision 2 (Sept 2013)	LSRAM x32/36 widths added. "IGLOO2 FPGA Product Family" table note added referring to updates in Table 3 – Table 6.	1-IV, 1-V – 1-VI
	"IGLOO2 Ordering Information" was updated. Part Numbers (tables 7 and 8) were removed. "IGLOO2 Device Status" table was updated.	1-VI, 1-VI
	M2GL090-FG676 and M2GL005-VF400 package pinouts finalized.	1-IV

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "IGLOO2 Device Status", is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

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