ISO1176 Isolated RS-485 Profibus Transceiver

1 Features

- Meets or Exceeds the Requirements of EN 50170 and TIA/EIA-485-A
- Signaling Rates up to 40 Mbps
- Differential Output Exceeds 2.1 V (54-Ω Load)
- Low Bus Capacitance – 10 pF (Maximum)
- Up to 160 Transceivers on a Bus
- 50 kV/μs Typical Transient Immunity
- Fail-Safe Receiver for Bus Open, Short, Idle
- 3.3-V Inputs are 5-V Tolerant
- Bus-Pin ESD Protection
  - 16-kV HBM Between Bus Pins and GND2
  - 6-kV HBM Between Bus Pins and GND1
- Safety and Regulatory Approvals
  - 4000-V_{PK} Isolation, 560-V_{PK} V_{IORM} per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 and DIN EN 61010-1
  - 2500 V_{RMS} Isolation Rating per UL 1577
  - 4000 V_{PK} Isolation Rating per CSA CA5A and IEC 60950-1

2 Applications

- Profibus
- Factory Automation
- Networked Sensors
- Motor and Motion Control
- HVA and Building Automation Networks
- Networked Security Stations

3 Description

The ISO1176 device is an isolated differential line transceiver designed for use in PROFIBUS applications. The device is ideal for long transmission lines because the ground loop is broken to provide for operation with a much larger common-mode voltage range. The symmetrical isolation barrier of each device is tested to provide 2500 V_{RMS} of isolation per UL between the line transceiver and the logic level interface.

The galvanically isolated differential bus transceiver is an integrated circuit designed for bidirectional data communication on multipoint bus-transmission lines. The transceiver combines a galvanically isolated differential line driver and differential input line receiver. The driver has an active-high enable with isolated enable-state output on the ISODE pin (pin 10) to facilitate direction control. The driver differential outputs and the receiver differential inputs connect internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus allowing up to 160 nodes.

The PV pin (pin 7) is provided as a full-chip enable option. All device outputs become high impedance when a logic low is applied to the PV pin. For more information, see the function tables in *Device Functional Modes*.

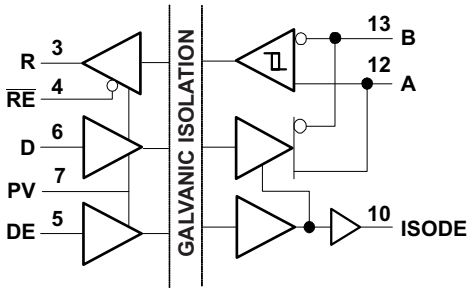
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO1176	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

ISO1176
Function Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2010) to Revision E — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- VDE standard changed to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ... 1
- Changed the IEC 60664-1 Ratings Table. Basic isolation group SPECIFICATION entry From: IIIa To: II ... 19

Changes from Revision C (October 2008) to Revision D — **Page**

- Added 560-Vpeak V_{IORM} to the first Features List ... 1
- Added UL 1577, IEC 60747-5-2 (VDE 0884, Rev. 2), to the Features List ... 1
- Added Input pulse width MIN = 10 ns to the RECOMMENDED OPERATING CONDITIONS table ... 5
- Added the CSA column to the Regulatory Information table ... 20
- Changed the ISO1176 “Sticky Bit” Issue section ... 26

Changes from Revision B (June 2008) to Revision C — **Page**

- Changed the text in the second paragraph of the DESCRIPTION From: "whenever the driver is disabled or V_{CC2} = 0" To: "allowing up to 160 nodes." ... 1

Changes from Revision A (May 2008) to Revision B — **Page**

- Changed L(IO1), Minimum air gap (Clearance) in the PACKAGE CHARACTERISTICS table From: MIN = 7.7mm To: 8.34mm ... 19

Changes from Original (March 2008) to Revision A **Page**

- Added 3.3-V Inputs are 5-V Tolerant to the Features List 1
- Added the Bus-Pin ESD Protection bullet and sub bullets to the Features List 1
- Added Bus pins to GND1 and Bus pins to GND2 to the ESD information in the Handling Rating table 5
- Added the APPLICATION INFORMATION section 24

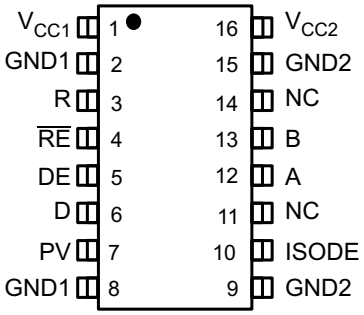
5 Description (continued)

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can cause damage to the transceiver and/or nearby sensitive circuitry if they are of sufficient magnitude and duration. The ISO1176 can significantly reduce the risk of data corruption and damage to expensive control circuits.

The device is characterized for operation over the ambient temperature range of –40°C to +85°C.

6 Pin Configuration and Functions

DW Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	12	I/O	Noninverting bus output
B	13	I/O	Inverting bus output
D	6	I	Driver input
DE	5	I	Driver logic-high enable
GND1	2, 8	—	Logic-side ground; internally connected
GND2	9, 15	—	Bus-side ground; internally connected
ISODE	10	—	Bus-side driver enable output
NC	11, 14	—	Not connected internally; may be left floating
PV	7	I	ISO1176 chip enable, logic high applied immediately after power up for device operation. A logic low 3-states all outputs.
R	3	O	Receiver output
$\overline{RE}$	4	I	Receiver logic-low enable
V_{CC1}	1	—	Logic side power supply
V_{CC2}	16	—	Bus side power supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range unless otherwise noted(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	V_{CC1}, V_{CC2}	–0.5	7	V
V_O	Voltage at any bus I/O pins		–9	14	V
V_I	Voltage input	D, DE or $\overline{RE}$	–0.5	7	V
I_O	Receiver output current		–10	10	mA
T_J	Maximum junction temperature			170	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) All voltage values except differential I/O bus voltages are with respect to the referenced network ground terminal and are peak voltage values.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Bus pins to 2, 8	±6000	V
			Bus pins to 9, 15	±16000	
			All pins	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		±1000	
		Machine model (MM), per ANSI/ESDS5.2-1996, all pins		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Logic-side supply voltage, V_{CC1} (with respect to GND1)		3.15		5.5	V
	Bus-side supply voltage, V_{CC2} (with respect to GND2)		4.75		5.25	
V_{CM}	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	PV, $\overline{RE}$	2		5.5	V
		D, DE	0.7 V_{CC1}			
V_{IL}	Low-level input voltage	PV, $\overline{RE}$	0		0.8	V
		D, DE			0.3 V_{CC1}	
V_{ID}	Differential input voltage	A with respect to B	–12		12	V
I_O	Output current	Driver	–70		70	mA
		Receiver	–8		8	
	Input pulse width		10			ns
T_A	Ambient temperature		–40	25	85	°C
T_J	Junction temperature				150	°C

7.4 Thermal Information

THERMAL METRIC[1]			ISO1176 DW [SOIC] 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	High-K board	81.4	°C/W
		Low-K board	168	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		41.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		46.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter		13.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter		45.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance		N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics: ISODE-Pin

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{CC2} – 0.8	4.6		V
		I_{OH} = –20 µA	V_{CC2} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 8 mA		0.2	0.4	V
		I_{OL} = 20 µA		0	0.1	

7.6 Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Logic-side RMS supply current	3 V	DE at 0 V		4	6	mA
			DE at V_{CC1}, 2 Mbps		5		
			DE at V_{CC1}, 25 Mbps		6		
		5.5 V	DE at 0 V		7	10	
			DE at V_{CC1}, 2 Mbps		8		
			DE at V_{CC1}, 25 Mbps		11		
I_{CC2}	Bus-side RMS supply current	5.25 V	DE at 0 V		15	18	mA
			DE at V_{CC1}, 2 Mbps, 54-Ω load		70		
			DE at V_{CC1}, 25 Mbps, 54-Ω load		75		

7.7 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OD}	Open-circuit differential output voltage	$\lvert V_A - V_B \rvert$, Figure 8		1.5		V_{CC2}	V
$\lvert V_{OD(SS)} \rvert$	Steady-state differential output voltage magnitude	See Figure 9 and Figure 13		2.1			V
		Common-mode loading with V_{test} from –7 V to 12 V, See Figure 10		2.1			
$\lvert \Delta V_{OD(SS)} \rvert$	Change in steady-state differential output voltage between logic states	R_L = 54 Ω, See Figure 11 and Figure 12		–0.2		0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	R_L = 54 Ω, See Figure 11 and Figure 12		2		3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage			–0.2		0.2	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage				0.5		
$V_{OD(RING)}$	Differential output voltage over- and undershoot	See Figure 13 and Figure 17				10%	$V_{OD(pp)}$
$V_{I(HYS)}$	Input voltage hysteresis	See Figure 14			150		mV
I_I	Input current	D, DE at 0 V or V_{CC1}		–10		10	μA
		PV[1] at 0 V or V_{CC1}				120	
$I_{O(OFF)}$	Output current with power off	V_{CC} ≤ 2.5 V		See receiver input current in *Electrical Characteristics: Receiver*			
I_{OZ}	High-impedance state output current	DE at 0 V					
$I_{OS(P)}$	Peak short-circuit output current	DE at V_{CC}, See Figure 15 and Figure 16	V_{OS} = –7 V to 12 V	–250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current		V_{OS} = 12 V, D at GND1			135	
			V_{OS} = –7 V, D at V_{CC1}	–135			
C_{OD}	Differential output capacitance			See receiver C_{IN} in *Electrical Characteristics: Receiver*			
CMTI	Common-mode transient immunity	See Figure 27		25			kV/μs

(1) The PV pin has a 50-kΩ pullup resistor and leakage current depends on supply voltage.

7.8 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{IT(+)}$	Positive-going differential input voltage threshold		See Figure 22	I_O = –8 mA		–80	–10	mV
$V_{IT(–)}$	Negative-going differential input voltage threshold			I_O = 8 mA	–200	–120		mV
V_{hys}	Hysteresis voltage ($V_{IT+} – V_{IT-}$)					40		mV
V_{OH}	High-level output voltage	V_{CC1} at 3.3 V and V_{CC2} at 5 V	V_{ID} = 200 mV, See Figure 22	I_{OH} = –8 mA	V_{CC1} –0.4	3		V
				$I_{O\ H}$ = –20 µA	V_{CC1} –0.1	3.3		
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, See Figure 22	$I_{O\ L}$ = 8 mA		0.2	0.4	V
				I_{OL} = 20 µA		0	0.1	
V_{OH}	High-level output voltage	V_{CC1} at 5 V and V_{CC2} at 5 V	V_{ID} = 200 mV, See Figure 22	I_{OH} = –8 mA	V_{CC1} –0.8	4.6		V
				$I_{O\ H}$ = –20 µA	V_{CC1} –0.1	5		
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, See Figure 22	$I_{O\ L}$ = 8 mA		0.2	0.4	V
				I_{OL} = –20 µA		0	0.1	
I_A, I_B	Bus pin input current		V_I = –7 V or 12 V, Other input = 0 V	V_{CC} = 4.75 V or 5.25 V	–160		200	µA
$I_{A(OFF)}$ $I_{B(OFF)}$				V_{CC2} = 0 V				
I_I	Receiver enable input current		$\overline{RE}$ = 0 V		–50		50	µA
I_{OZ}	High-impedance state output current		$\overline{RE}$ = V_{CC1}		–1		1	µA
R_{ID}	Differential input resistance		A, B		48			kΩ
C_{ID}	Differential input capacitance		Test input signal is a 1.5-MHz sine wave with 1 V_{pp} amplitude , C_D is measured across A and B			7	10	pF
CMR	Common-mode rejection		See Figure 26			4		V

7.9 Power Dissipation Characteristics

PARAMETER			VALUE	UNIT
P_D	Power Dissipation	V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, CL = 15 pF, Input a 20 MHz 50% duty-cycle square wave	220	mW

7.10 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay time	V_{CC1} at 5 V V_{CC2} at 5 V	See Figure 17			35	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{p\ HL} – t_{pLH}\rvert$)				2	5	ns
t_{pLH}, t_{pHL}	Propagation delay time	V_{CC1} at 3.3 V V_{CC2} at 5 V				40	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{p\ HL} – t_{p\ LH}\rvert$)				2	5	ns
t_r	Differential output signal rise time			2	3	7.5	ns
t_f	Differential output signal fall time			2	3	7.5	ns
t_{pDE}	DE to ISODE prop delay		See Figure 21			30	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew		See Figure 18			1	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output		C_L = 50 pF, $\overline{RE}$ at 0 V, See Figure 19 and Figure 20			80	ns
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-to-high-impedance output					80	ns
$\lvert t_{p(AZL)} – t_{p(BZH)}\rvert$ $\lvert t_{p(AZH)} – t_{p(BZL)}\rvert$	Enable skew time				0.55	1.5	ns
$t_{(CFB)}$	Time from application of short-circuit to current foldback		See Figure 16		0.5		µs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown		T_A = 25°C, See Figure 16	100			µs

7.11 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pLH}, t_{pHL}	Propagation delay time	V_{CC1} at 5 V, V_{CC2} at 5 V	See Figure 23			50	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{p\ HL} - t_{pLH} \rvert$)				2	5	ns
t_{pLH}, t_{pHL}	Propagation delay time	V_{CC1} at 3.3 V, V_{CC2} at 5 V				55	ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{p\ HL} - t_{p\ LH} \rvert$)				2	5	ns
t_r	Output signal rise time				2	4	ns
t_f	Output signal fall time				2	4	ns
t_{pZH}	Propagation delay time, high-impedance-to-high-level output		DE at V_{CC1}, See Figure 24		13	25	ns
t_{pHZ}	Propagation delay time, high-level-to-high-impedance output				13	25	ns
t_{pZL}	Propagation delay time, high-impedance-to-low-level output		DE at V_{CC}, See Figure 25		13	25	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output				13	25	ns

7.12 Typical Characteristics

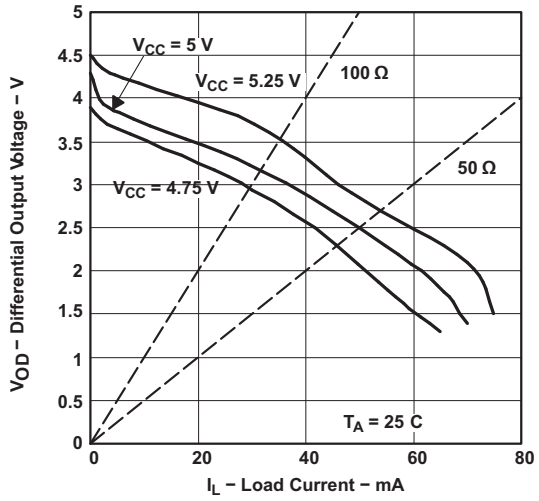


Figure 1. Differential Output Voltage vs Load Current

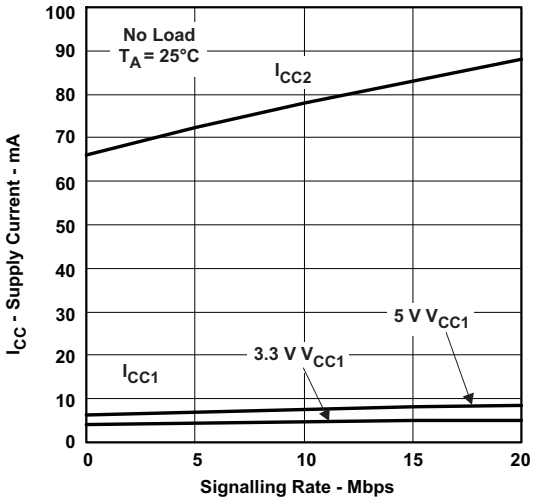


Figure 2. RMS Supply Current vs Signaling Rate

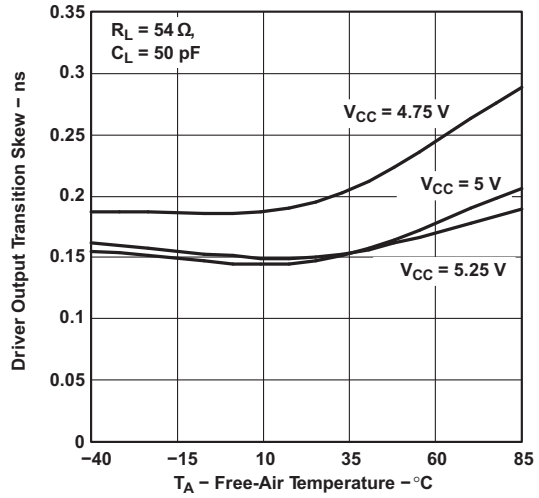


Figure 3. Driver Output Transition Skew vs Free-Air Temperature

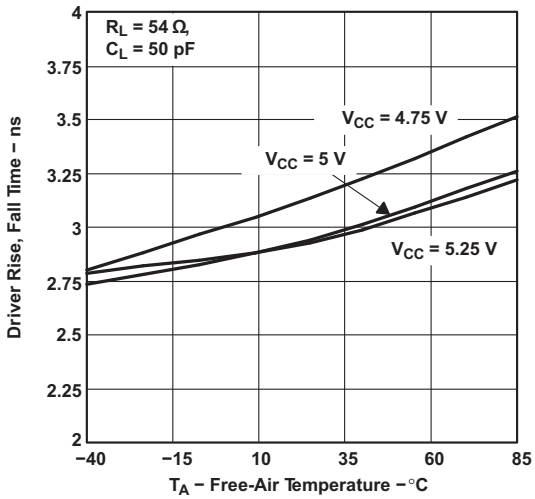


Figure 4. Driver Rise and Fall Time vs Free-Air Temperature

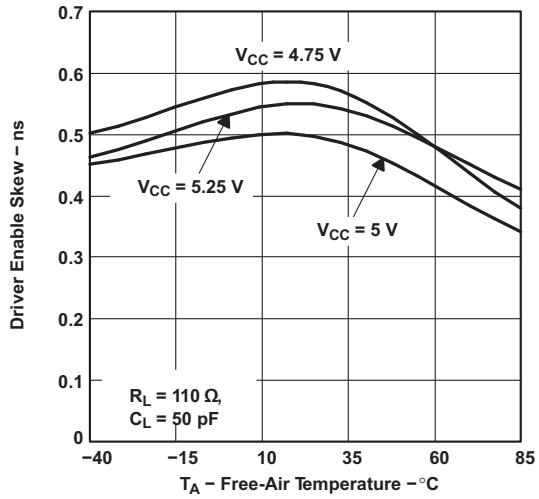


Figure 5. Driver Enable Skew vs Free-Air Temperature

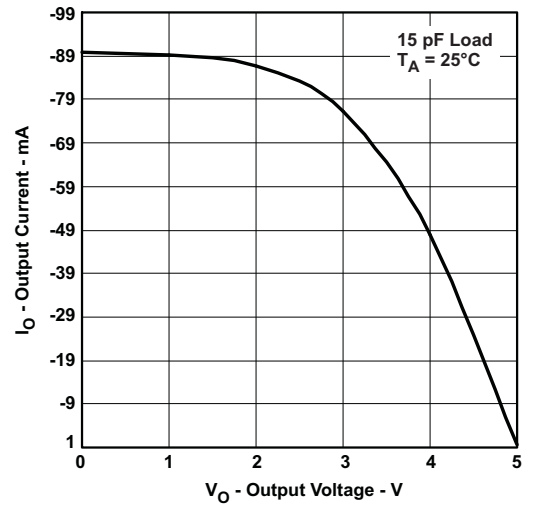


Figure 6. High-Level Output Voltage vs High-Level Output Current

Typical Characteristics (continued)

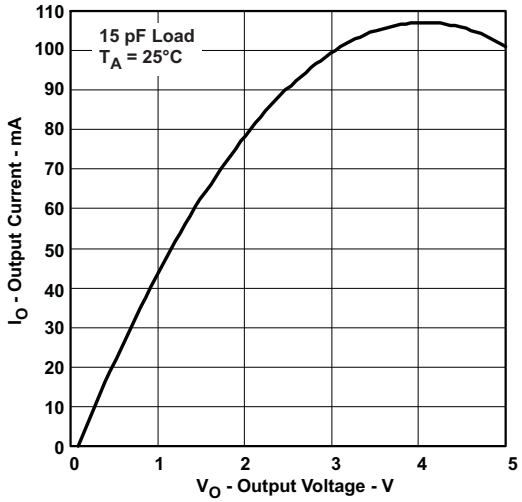


Figure 7. Low-Level Output Voltage vs Low-Level Output Current

8 Parameter Measurement Information

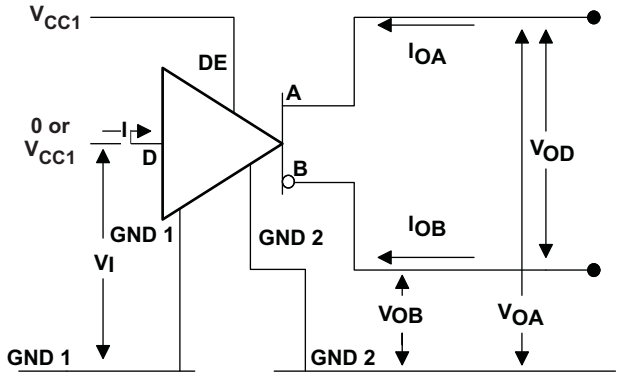


Figure 8. Open Circuit Voltage Test Circuit

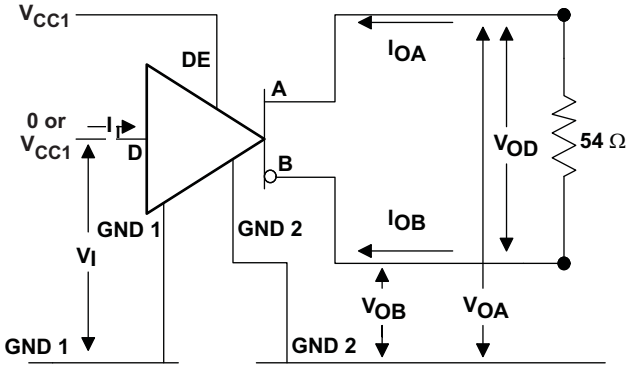


Figure 9. V_{OD} Test Circuit

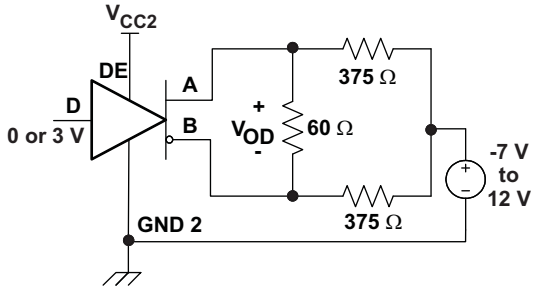


Figure 10. Driver V_{OD} With Common-Mode Loading Test Circuit

Parameter Measurement Information (continued)

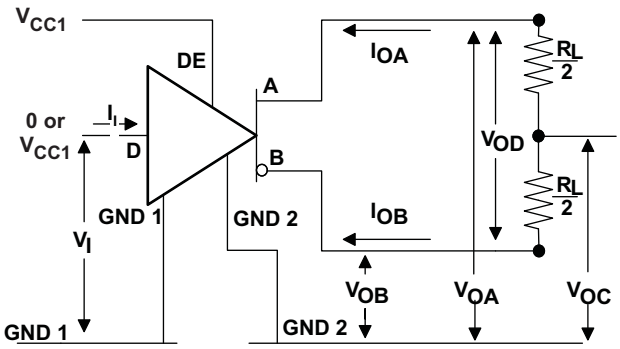


Figure 11. Driver V_{OD} and V_{OC} Without Common-Mode Loading Test Circuit

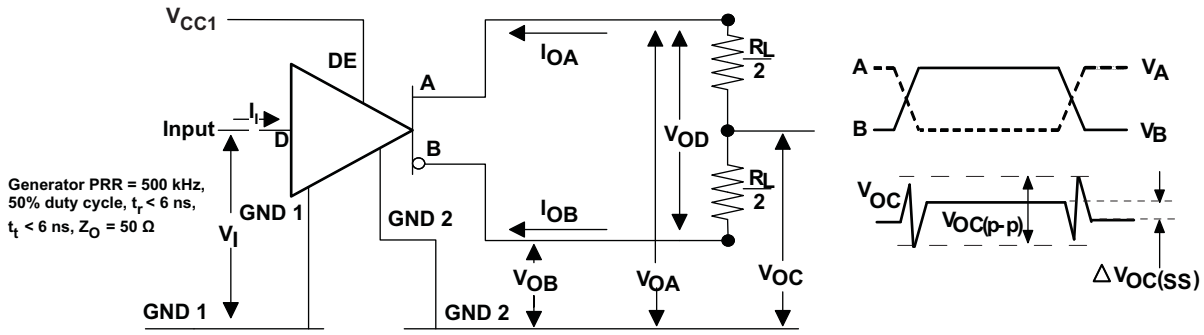


Figure 12. Steady-State Output Voltage Test Circuit and Voltage Waveforms

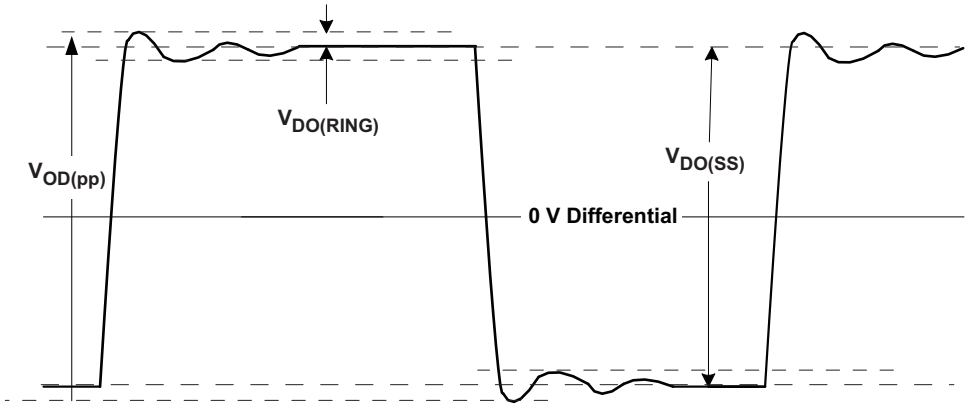


Figure 13. $V_{OD(RING)}$ Waveform and Definitions

Parameter Measurement Information (continued)

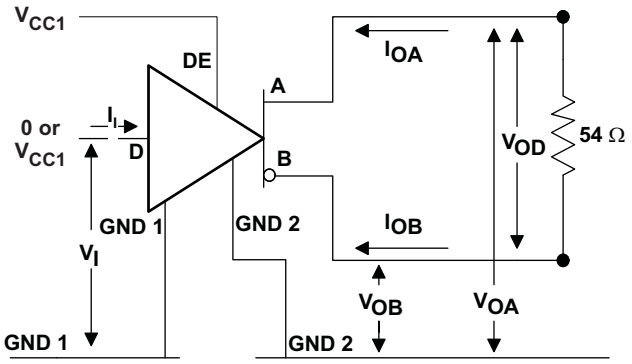


Figure 14. Input Voltage Hysteresis Test Circuit

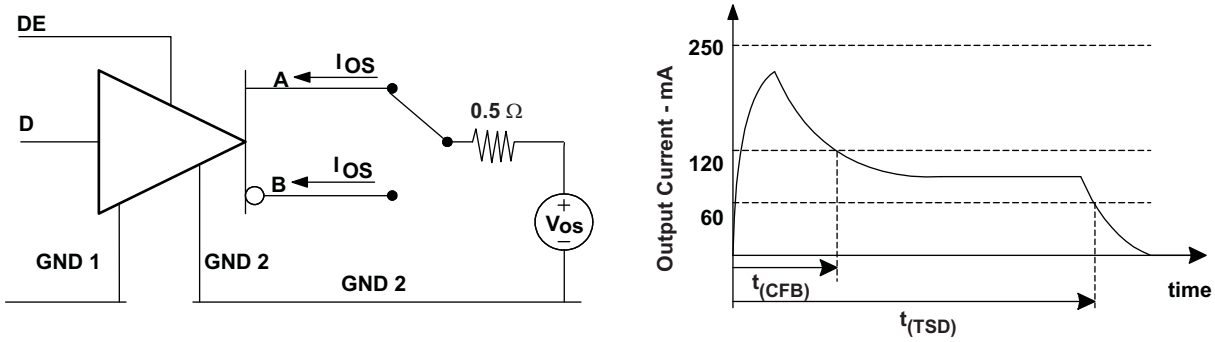


Figure 15. Driver Short-Circuit Test Circuit and Waveforms (Short-Circuit Applied at Time t=0)

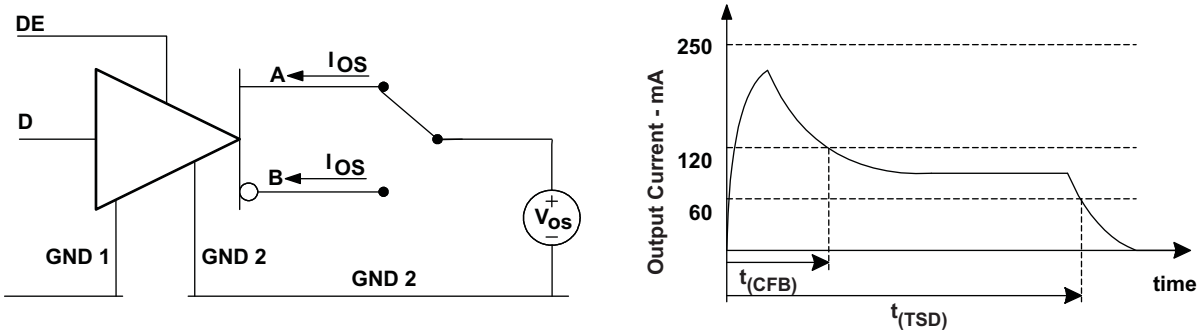


Figure 16. $I_{OS(SS)}$ Steady State Short-Circuit Output Current Test Circuit

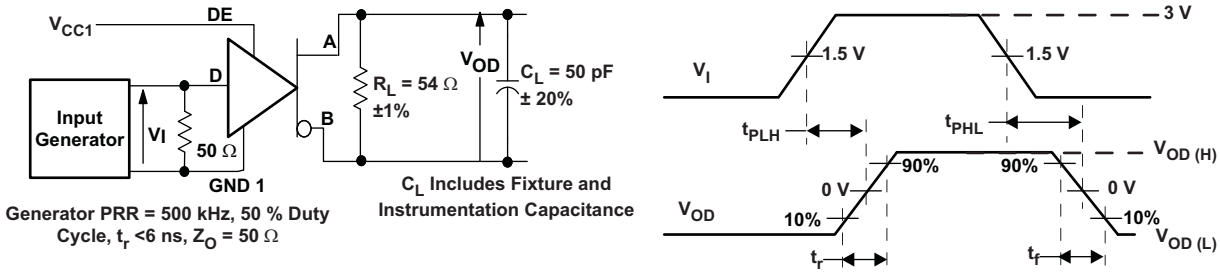


Figure 17. Driver Switching Test Circuit and Waveforms

Parameter Measurement Information (continued)

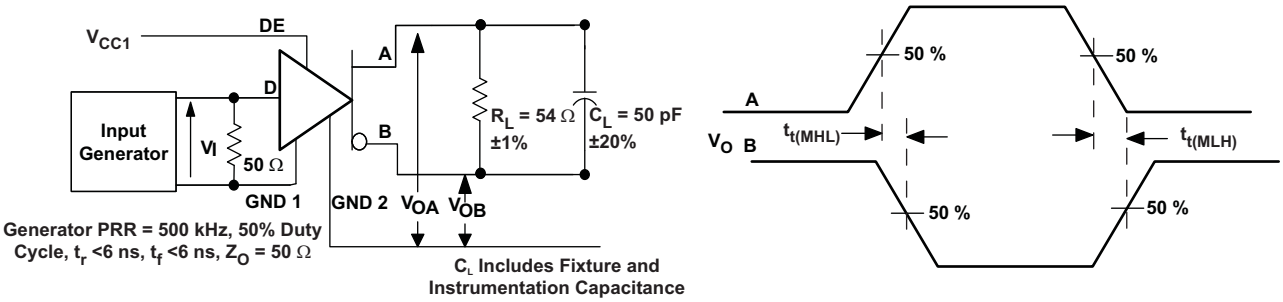


Figure 18. Driver Output Transition Skew Test Circuit and Waveforms

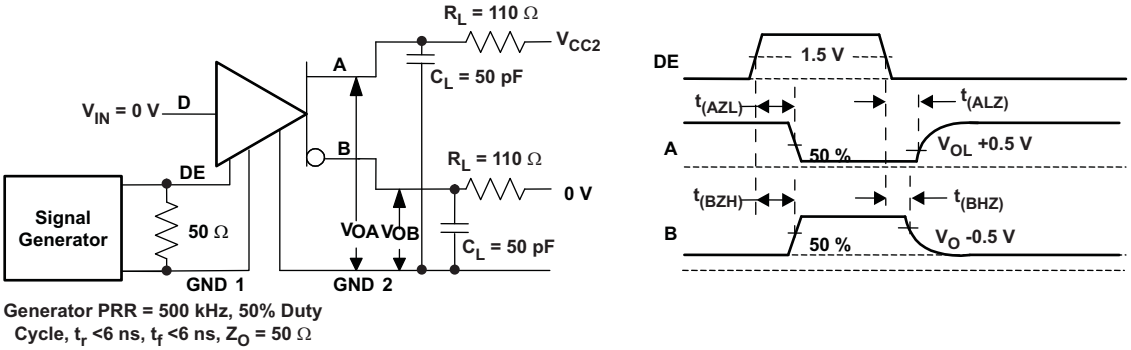


Figure 19. Driver Enable and Disable Test, D at Logic Low Test Circuit and Waveforms

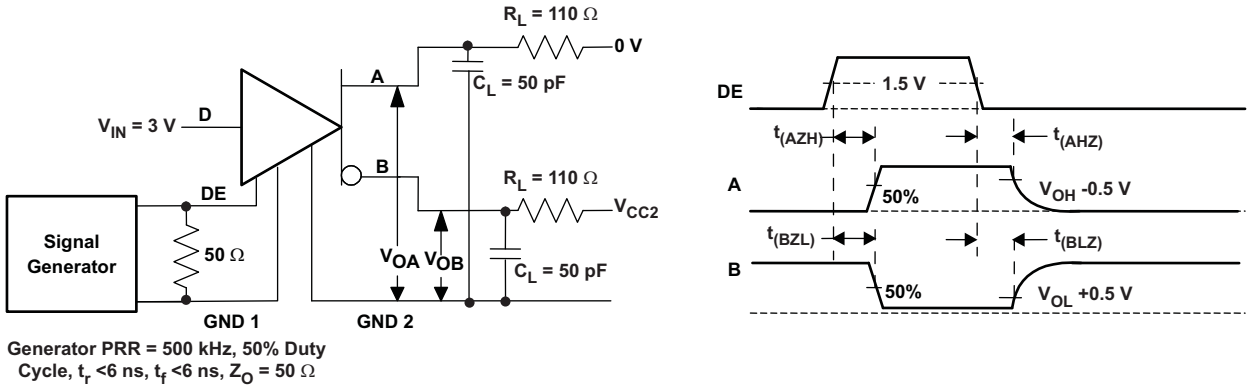


Figure 20. Driver Enable and Disable Test, D at Logic High Test Circuit and Waveforms

Parameter Measurement Information (continued)

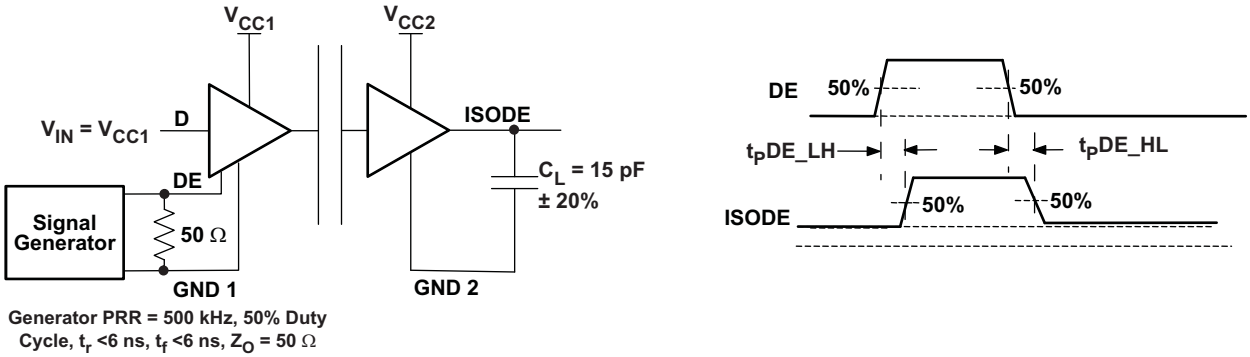


Figure 21. DE to ISODE Prop Delay Test Circuit and Waveforms

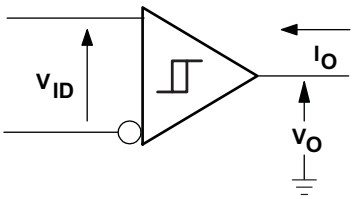


Figure 22. Receiver DC Parameter Definitions

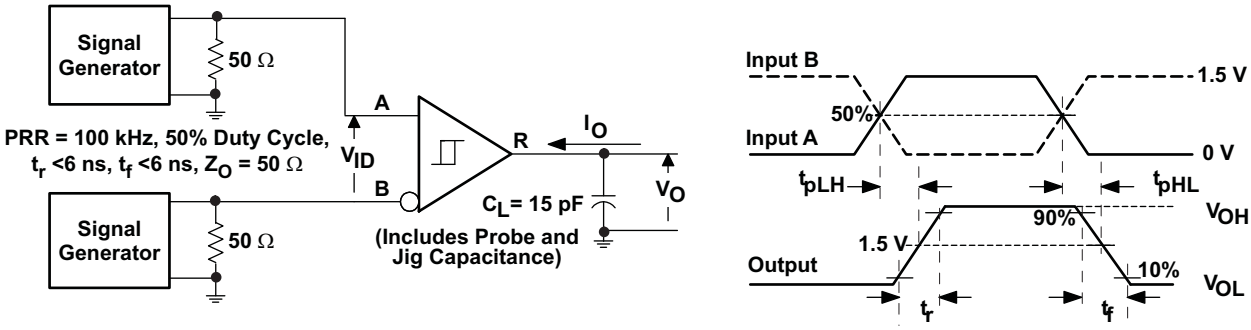


Figure 23. Receiver Switching Test Circuit and Waveforms

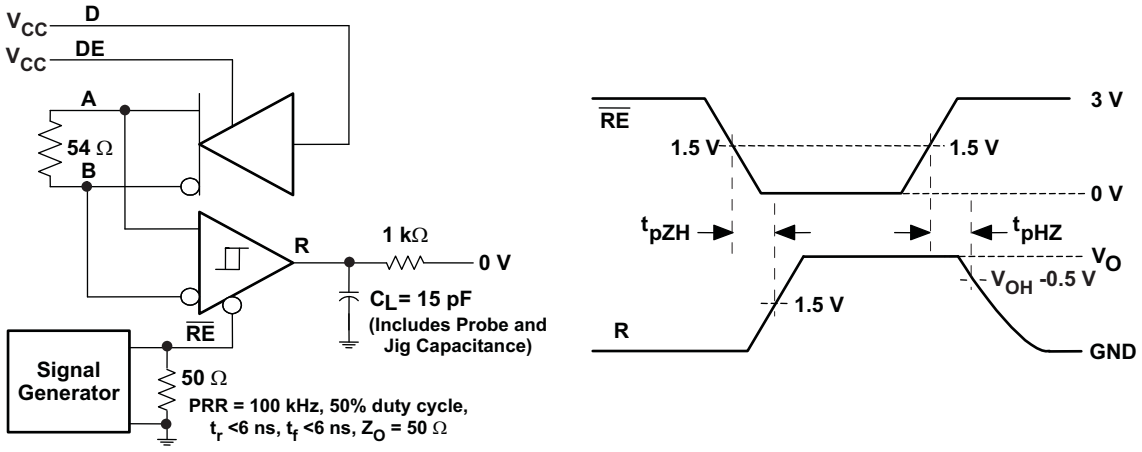


Figure 24. Receiver Enable Test Circuit and Waveforms, Data Output High

Parameter Measurement Information (continued)

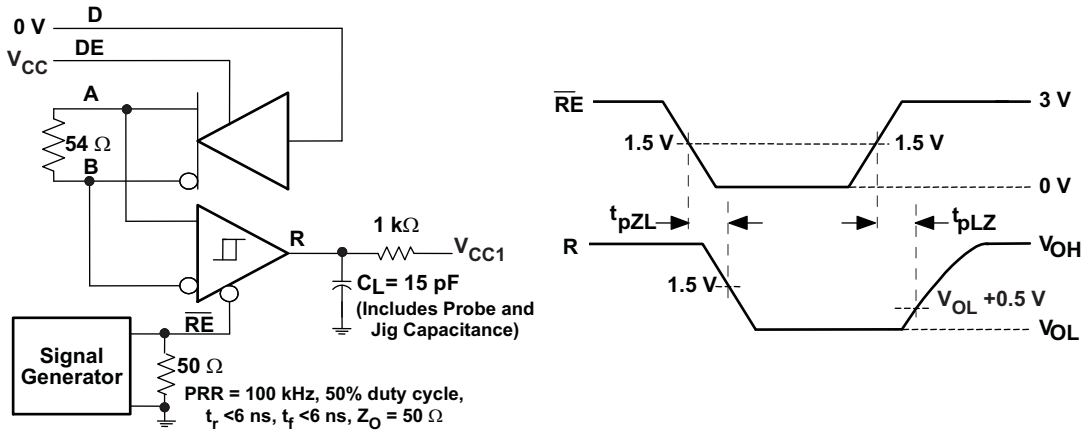


Figure 25. Receiver Enable Test Circuit and Waveforms, Data Output Low

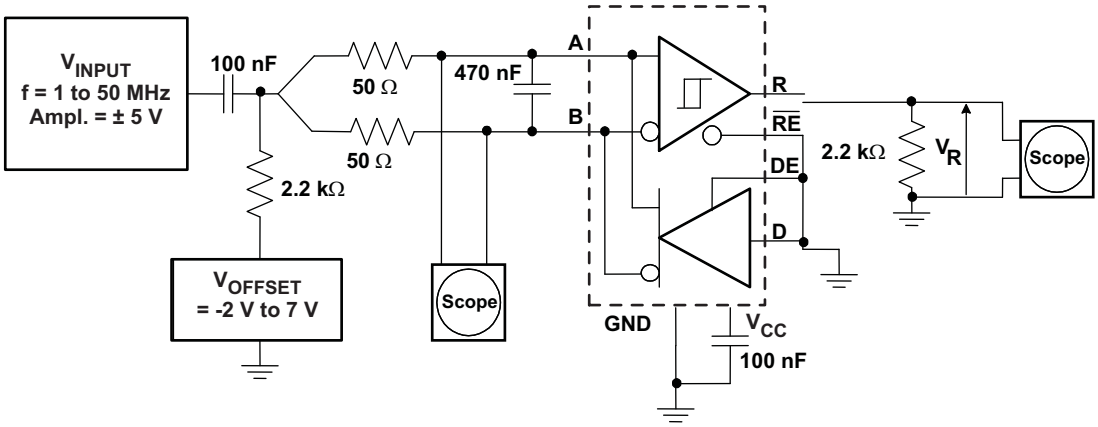


Figure 26. Common-Mode Rejection Test Circuit

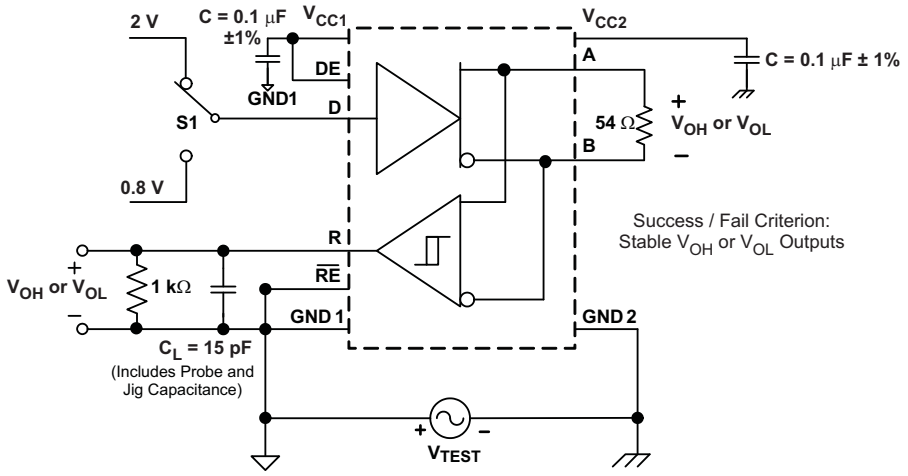


Figure 27. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

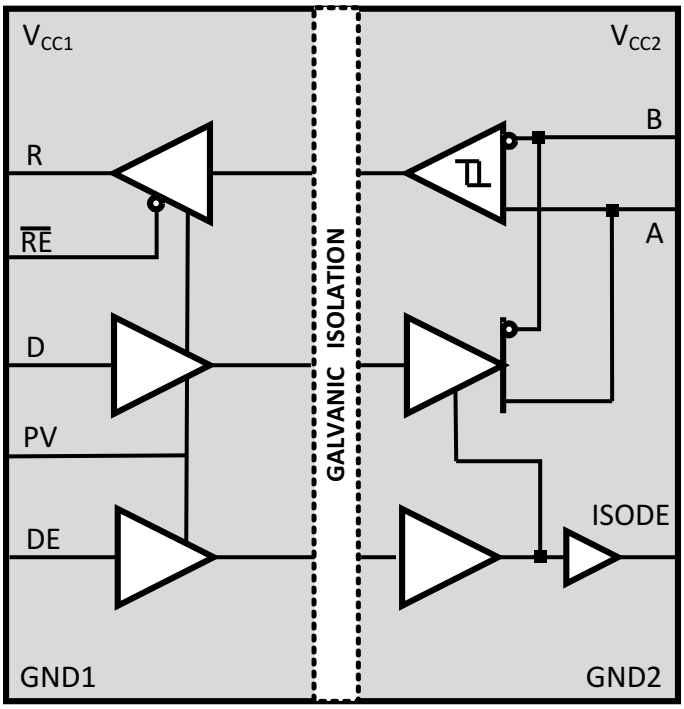
9.1 Overview

The ISO1176 is an isolated half-duplex differential line transceiver that meets the requirements of EN 50170 and TIA/EIA 485/422 applications. The device is rated to provide galvanic isolation of up to 2500 V_{RMS} for 60 s per UL 1577. The device has active-high driver enable and active-low receiver enable functions to control the data flow. The device has maximum data transmission speed of 40 Mbps.

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_{(A)} – V_{(B)}$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative. When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}, thus, when left open while the driver is enabled, output A turns high and B turns low.

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$ the output is indeterminate. When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Insulation and Safety-Related Package Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (Clearance)	Shortest terminal-to-terminal distance through air	8.34			mm
L(I02)	Minimum external tracking (Creepage)(1)	Shortest terminal-to-terminal distance across the package surface	8.1			mm
CTI	Tracking resistance (Comparative Tracking Index)	DIN IEC 60112 / VDE 0303 Part 1	≥400			V
	Minimum internal gap (Internal Clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, TA = 25°C, all pins on each side of the barrier tied together creating a 2-terminal device		$>10^{12}$		Ω
C_{IO}	Barrier capacitance Input to output	V_I = 0.4 sin (4E6πt)		2		pF
C_I	Input capacitance to ground	V_I = 0.4 sin (4E6πt)		2		pF

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit-board (PCB) do not reduce this distance.
Creepage and clearance on a PCB become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a PCB are used to help increase these specifications.

9.3.2 DIN V VDE V 0884-10 Insulation Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IOTM}	Transient overvoltage	t = 60 s	4000	V_{PK}
V_{IORM}	Maximum working insulation voltage		560	V_{PK}
V_{PR}	Input to output test voltage	Method b1, V_{PR} = V_{IORM} × 1.875, 100% Production test with t = 1 s, Partial discharge <5 pC	1050	V_{PK}
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

9.3.3 IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	II
Installation classification	Rated mains voltage < 150 V_{RMS}	I-IV
	Rated mains voltage < 300 V_{RMS}	I-III

9.3.4 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current-limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DW-16	$R_{\theta JA}$ = 168°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			157	mA
T_S	Maximum case temperature	DW-16				150	°C

The safety-limiting constraint is the absolute maximum junction temperature specified in *Absolute Maximum Ratings*. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in *Thermal Information* is that of a device installed in the JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages and is conservative.

The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance..

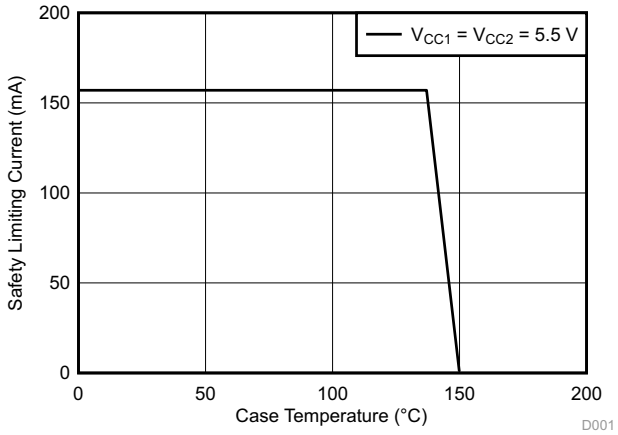


Figure 28. DW-16 $R_{\theta JC}$ Thermal Derating Curve per VDE

9.3.5 Regulatory Information

VDE	CSA	UL
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12	Approved under CSA Component Acceptance Notice 5A and IEC 60950-1	Recognized under UL 1577 Component Recognition Program(1)
Basic insulation, 4000 V_{PK} Maximum transient overvoltage, 560 V_{PK} Maximum working voltage	4000 V_{PK} Isolation rating, 560 V_{PK} Basic working voltage per CSA 60950-1-07 and IEC 60950-1 (2nd Ed)	Single Protection, 2500 V_{RMS}
Certificate number: 40016131	Master contract number: 220991	File number: E181974

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

9.4 Device Functional Modes

Table 1. Driver Function Table(1)

V_{CC1}	V_{CC2}	POWER VALID (PV) (ISO1176)	INPUT (D)	ENABLE INPUT (DE)	ENABLE OUTPUT (ISODE)	OUTPUTS	
						A	B
PU	PU	H or open	H	H	H	H	L
PU	PU	H or open	L	H	H	L	H
PU	PU	H or open	X	L	L	Z	Z
PU	PU	H or open	X	open	L	Z	Z
PU	PU	H or open	open	H	H	H	L
PD	PU	X	X	X	L	Z	Z
PU	PD	X	X	X	L	Z	Z
PD	PD	X	X	X	L	Z	Z
X	X	L	X	X	L	Z	Z

(1) PU = powered up, PD = powered down, H = high level, L= low level, X = don't care, Z = high impedance (off)

Table 2. Receiver Function Table(1)

V_{CC1}	V_{CC2}	POWER VALID (PV) (ISO1176)	DIFFERENTIAL INPUT $V_{ID} = (V_A - V_B)$	ENABLE ($\overline{RE}$)	OUTPUT (R)
PU	PU	H or open	$-0.01\ V \le V_{ID}$	L	H
PU	PU	H or open	$-0.2\ V < V_{ID} < -0.01\ V$	L	?
PU	PU	H or open	$V_{ID} \le -0.2\ V$	L	L
PU	PU	H or open	X	H	Z
PU	PU	H or open	X	open	Z
PU	PU	H or open	Open-circuit	L	H
PU	PU	H or open	Short-circuit	L	H
PU	PU	H or open	Idle (terminated) bus	L	H
PD	PU	X	X	X	Z
PU	PD	H or open	X	L	H
PD	PD	X	X	X	Z
X	X	L	X	X	Z

(1) PU = powered up, PD = powered down, H = high level, L= low level, X = don't care, Z = high impedance (off), ? = indeterminate

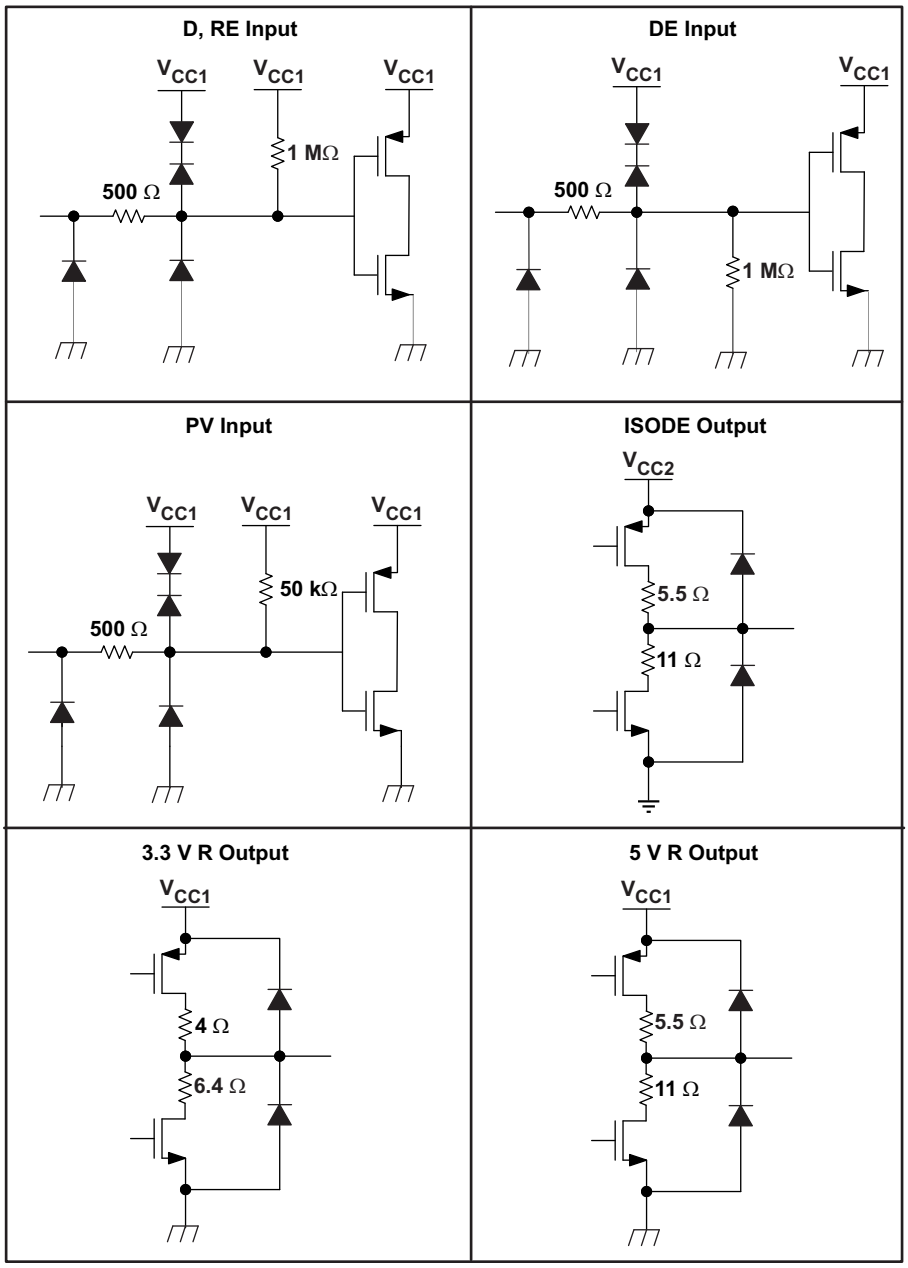


Figure 29. Equivalent I/O Schematics

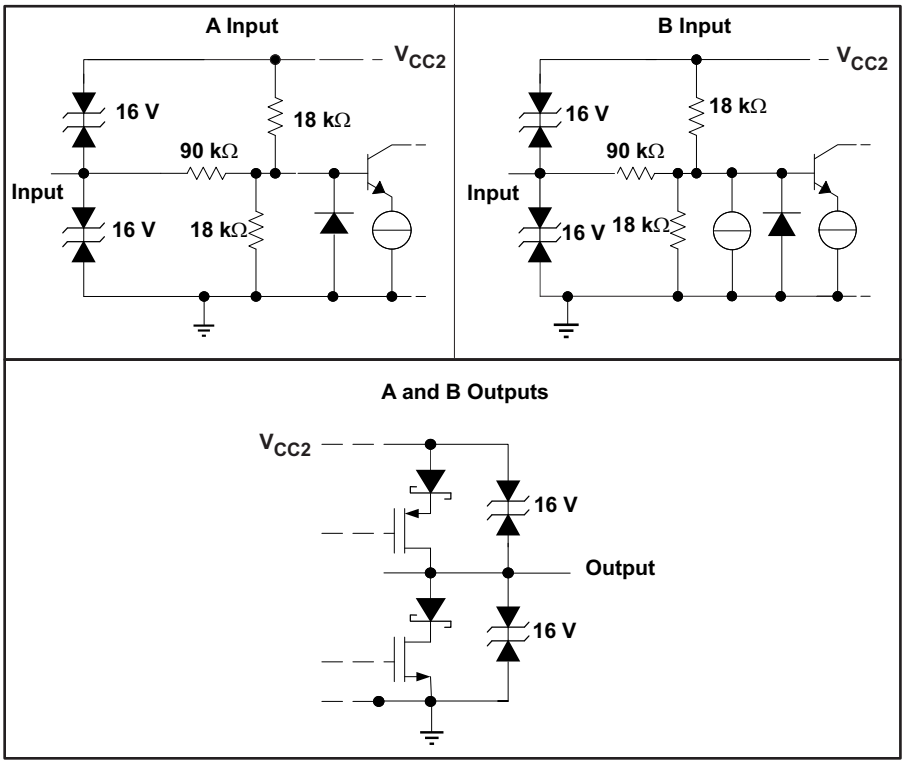


Figure 30. Equivalent I/O Schematics for A and B Inputs and Outputs

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ISO1176 device consists of a RS-485 transceiver, commonly used for asynchronous data transmissions. For half-duplex transmission, only one pair is shared for both transmission and reception of data. To eliminate line reflections, each cable end is terminated with a termination resistor, R(T), whose value matches the characteristic impedance, Z0, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

10.2 Typical Application

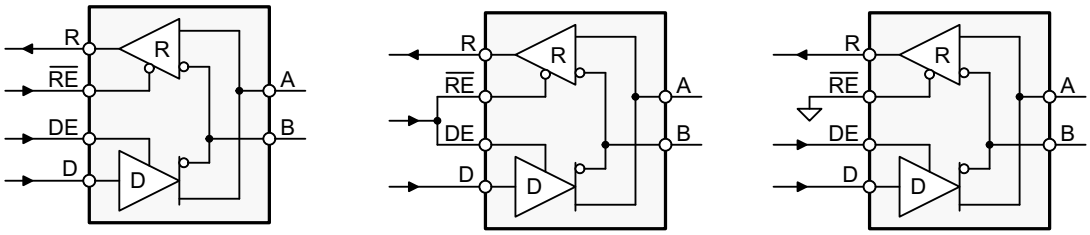


Figure 31. Half-Duplex Transceiver Configurations

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

Table 3. Design Parameters

PARAMETER	VALUE
Pullup and Pulldown Resistors	1 kΩ to 10 kΩ
Decoupling Capacitors	100 nF

10.2.2 Detailed Design Procedure

Isolating of a circuit insulates it from other circuits and earth, so that noise voltage develops across the insulation rather than circuit components. The most common noise threat to data-line circuits is voltage surges or electrical fast transients that occur after installation. The transient ratings of the ISO1176 standard are sufficient for all but the most severe installations. However, some equipment manufacturers use ESD generators to test equipment transient susceptibility. This practice can exceed insulation ratings. ESD generators simulate static discharges that may occur during device or equipment handling with low-energy but high-voltage transients.

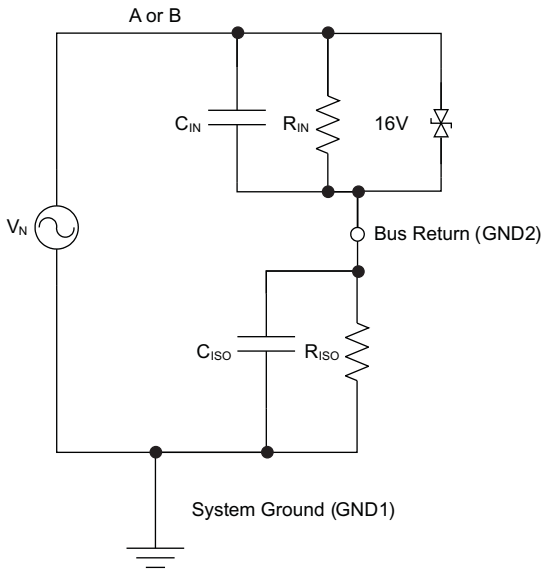


Figure 32. Device Model for Static Discharge Testing

Figure 32 models the ISO1176 bus IO connected to a noise generator. C_{IN} and R_{IN} is the device, and any other stray or added capacitance or resistance across the A or B pin to GND2. C_{ISO} and R_{ISO} is the capacitance and resistance between GND1 and GND2 of the ISO1176, plus those of any other insulation (transformer, and so forth). Stray inductance is assumed to be negligible.

10.2.2.1 Transient Voltages

From this model, the voltage at the isolated bus return is

$$v_{GND2} = v_N \frac{Z_{ISO}}{Z_{ISO} + Z_{IN}} \tag{1}$$

and is always less than 16 V from V_N. If the ISO1176 is tested as a stand-alone device,

- R_{IN}= 6 x 10^4 Ω,
- C_{IN}= 16 x 10^{-12} F,
- R_{ISO}= 10^9 Ω and
- C_{ISO}= 10^{-12} F.

Notice from Figure 32 that the resistor ratio determines the voltage ratio at low frequencies, and that the inverse capacitance ratio determines the voltage ration at high frequencies. In the stand-alone case and for low frequencies,

$$\frac{v_{GND2}}{v_N} = \frac{R_{ISO}}{R_{ISO} + R_{IN}} = \frac{10^9}{10^9 + 6x10^4} \tag{2}$$

or essentially all of the noise appears across the barrier.

At high frequencies,

$$\frac{v_{GND2}}{v_N} = \frac{1/C_{ISO}}{1/C_{ISO} + 1/C_{IN}} = \frac{1}{1 + C_{ISO}/C_{IN}} = \frac{1}{1 + 1/16} = 0.94 \tag{3}$$

and 94% of V_N appears across the barrier. As long as R_{ISO} is greater than R_{IN} and C_{ISO} is less than C_{IN}, most of the transient noise appears across the isolation barrier, as it should.

Using ESD generators to test equipment transient susceptibility, or considering product claims of ESD ratings greater than the barrier transient ratings of an isolated interface is not recommended. ESD is best managed through recessing or covering connector pins in a conductive connector shell, and by proper installer training.

10.2.2.2 ISO1176 "Sticky Bit" Issue (Under Certain Conditions)

Summary: In applications with sufficient differential noise on the bus, the output of the ISO1176 receiver may "stick" at an incorrect state for up to 30 µs.

Description: The ISO1176 isolated Profibus (RS-485) transceiver is rated for signaling up to 40 Mbps on twisted-pair bus lines. The receiver thresholds comply with RS-485 and Profibus specifications; an input differential voltage $V_{ID} = V_A – V_B > 200$ mV causes a logic High on the R output, and $V_{ID} < –200$ mV causes a logic Low on the R output. To assure a known receiver output when the bus is shorted or idle, the upper threshold is set below zero, such that $V_{ID} = 0$ mV causes a logic High on the R output. The data sheet specifies a typical upper threshold (V_{IT+}) of –80 mV and a typical lower threshold (V_{IT-}) of –120 mV.

At a signaling rate of 40 Mbps, each valid data bit has a duration of 25 ns. At typical Profibus signaling rates of 12 Mbps or lower, each valid data bit has a duration of 83 ns or more. The ISO1176 correctly sets the R output for each of these valid data bits.

In applications with a high degree of differential noise on the bus lines, it is possible to get short periods when an invalid bus voltage triggers a change in state of the internal receiver circuits. An issue with the digital isolation channel in the ISO1176 may cause the invalid receiver state to "stick" rather than immediately transition back to the correct state. The receiver output will always transition to the correct state, but may stick in the incorrect state for up to 30 µs. This can cause a temporary loss of data.

Figure 33 shows two cases which could result in temporary loss of data.

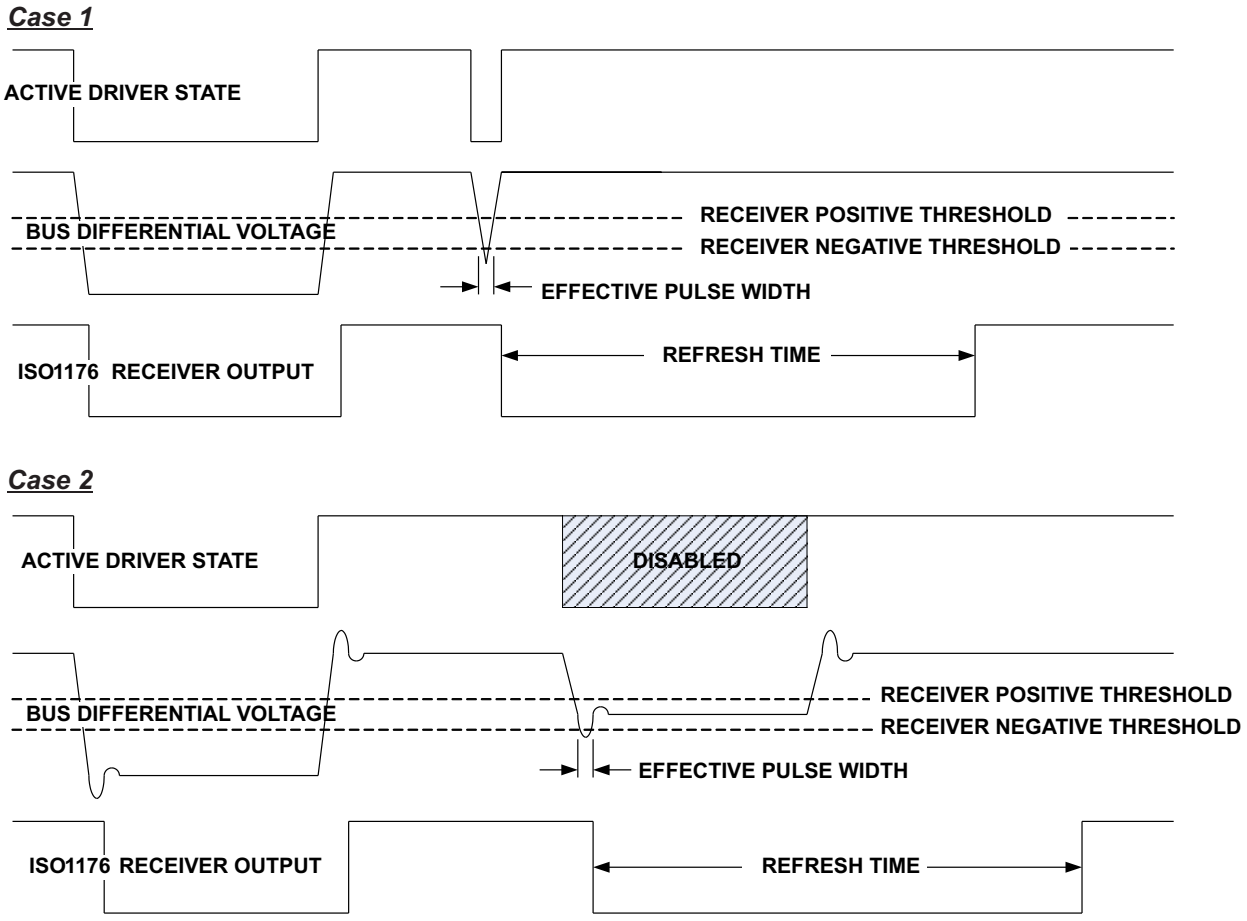


Figure 33. "Sticky Bit" Issue Waveforms

10.2.3 Application Curve

At maximum working voltage, ISO1176 isolation barrier has more than 28 years of life.

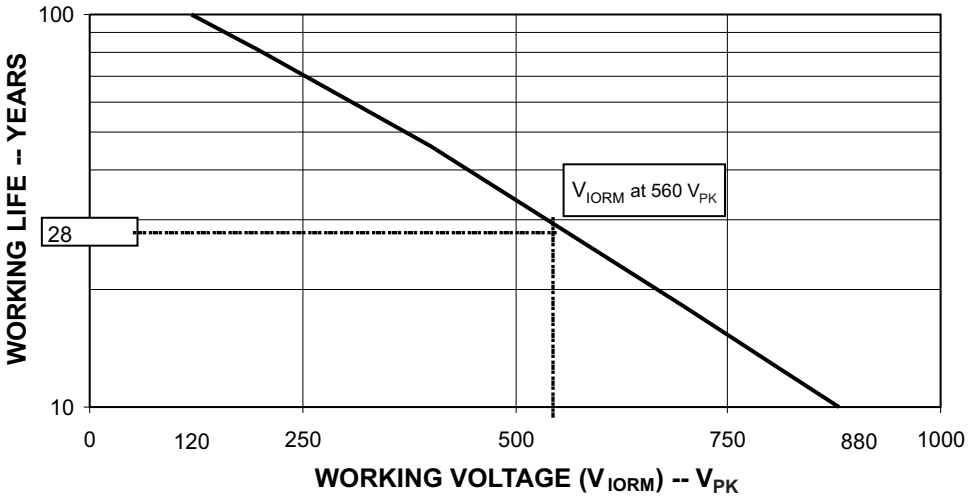


Figure 34. Time-Dependent Dielectric Breakdown Test Results

11 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, TI recommends a 0.1-µF bypass capacitor at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as TI's SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 data sheet (SLLSEA0).

12 Layout

12.1 Layout Guidelines

ON-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices. Because ESD and EFT transients have a wide frequency bandwidth from approximately 3-MHz to 3-GHz, high-frequency layout techniques must be applied during PCB design. A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 35).

- Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane, and low-frequency signal layer.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.
- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use V_{CC} and ground planes to provide low-inductance. High-frequency currents might follow the path of least inductance and not necessarily the path of least resistance.
- Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
- Apply 0.1-µF bypass capacitors as close as possible to the V_{CC}-pins of transceiver, UART, and controller ICs on the board.
- Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in theses lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.
- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.

If an additional supply voltage plane or signal layer is needed, add a second power and ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

NOTE

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

12.2 Layout Example

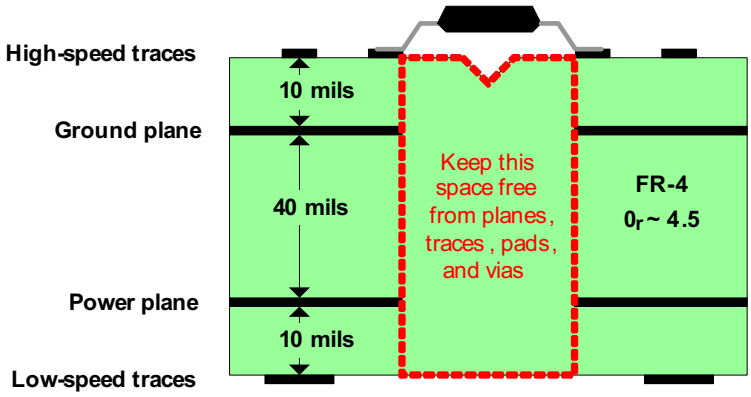


Figure 35. Recommended Layer Stack

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- SLLA284, *Digital Isolator Design Guide*
- SLLSEA0, *Transformer Driver for Isolated Power Supplies*
- SLLA353, *Isolation Glossary*

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO1176DW	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176	Samples
ISO1176DWG4	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176	Samples
ISO1176DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ISO1176	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

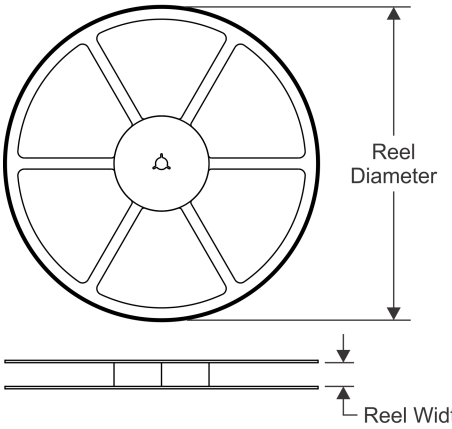
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

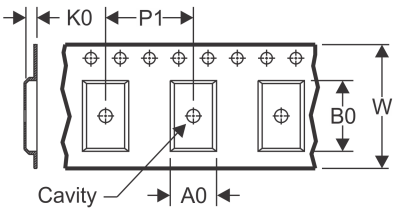
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

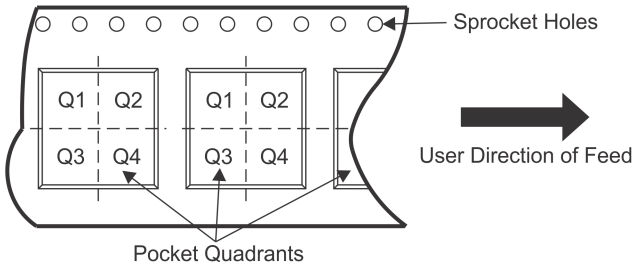


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

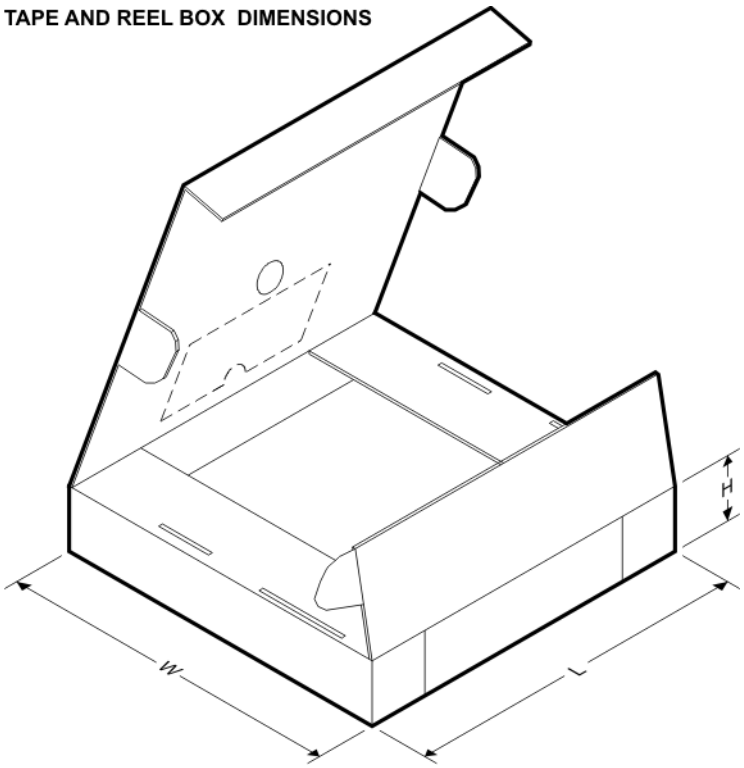
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO1176DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO1176DWR	SOIC	DW	16	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

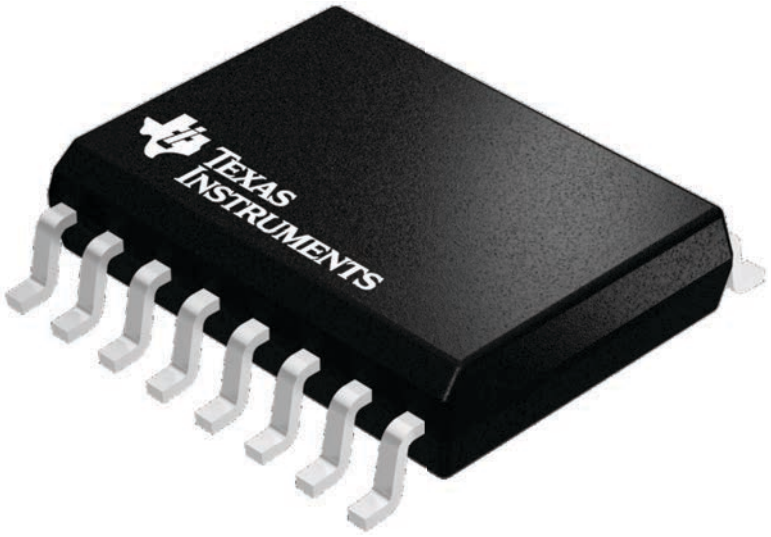
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

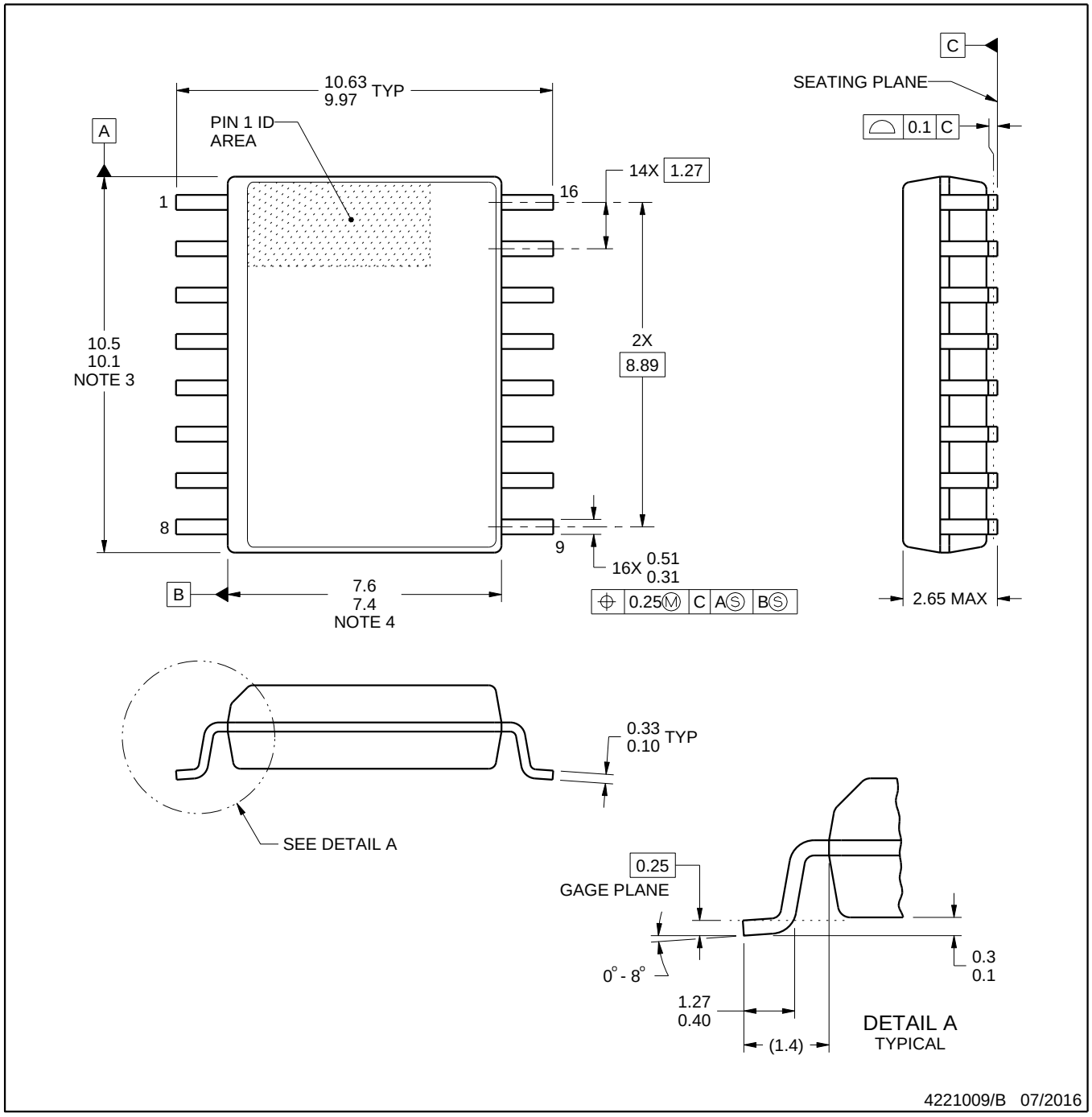
SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



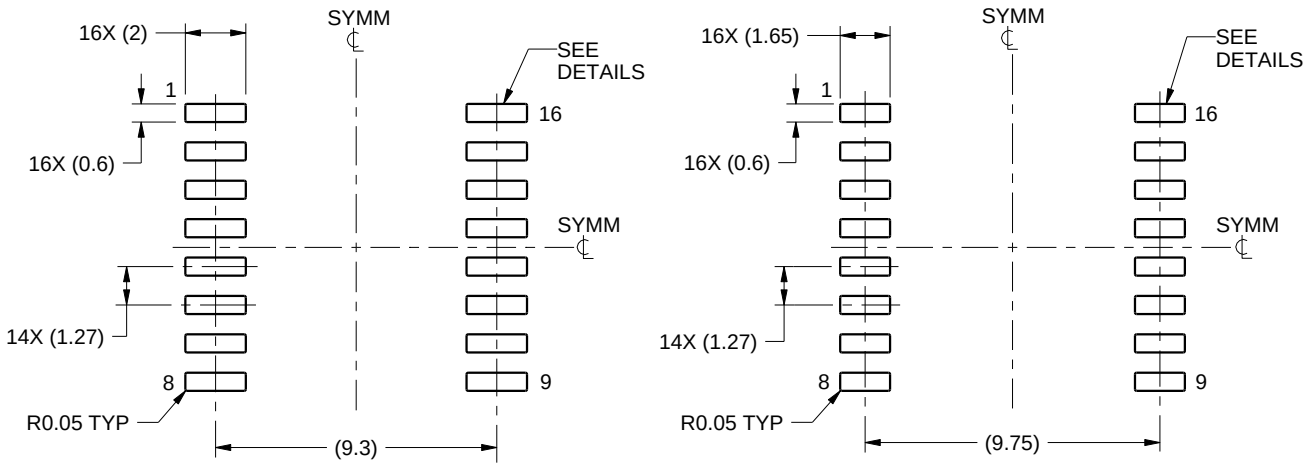
4224780/A

SOIC



NOTES:

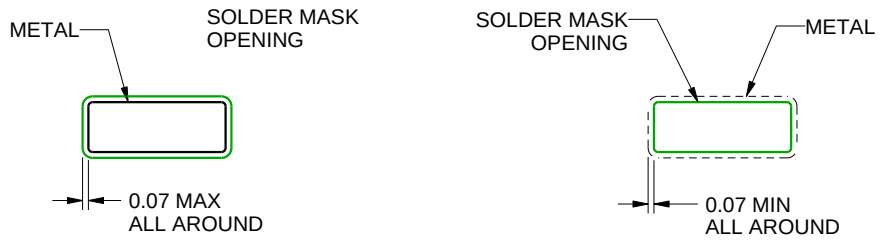
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

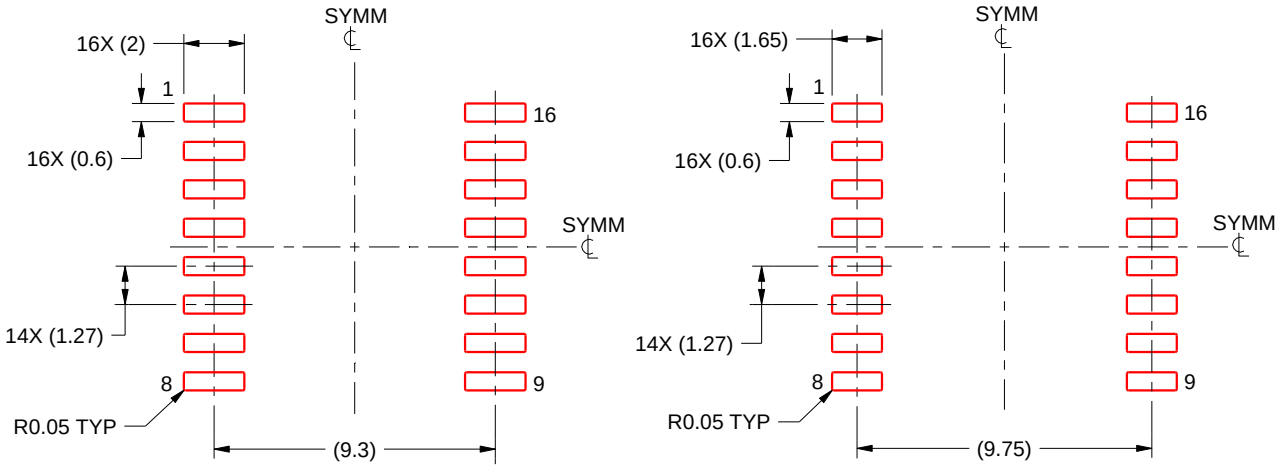
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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