

N-Channel MOSFET

Lead Free Package and Finish

Applications:

- Adaptor
- Charger
- SMPS

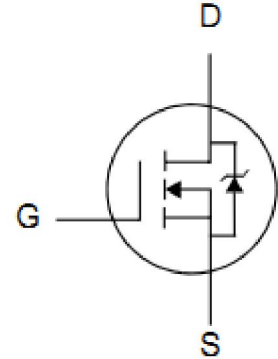
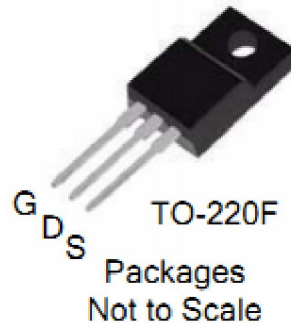
V_{DSS}	$R_{DS(ON)}(Typ.)$	I_D
650V	1.2Ω	7A

Features:

- RoHS Compliant
- Low ON Resistance
- Low Gate Charge
- Peak Current vs Pulse Width Curve
- Inductive Switching Curves

Ordering Information

PART NUMBER	PACKAGE	BRAND
ITA07N65R	TO-220F	IPS



Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	ITA07N65R	Units
V_{DSS}	Drain-to-Source Voltage	650	V
I_D	Continuous Drain Current	7	A
I_{DM}	Pulsed Drain Current, $V_{GS}@10\text{V}$ (NOTE *2)	28	A
P_D	Power Dissipation	35	W
	Derating Factor above 25°C	0.28	W/ $^\circ\text{C}$
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy (L=10mH)	350	mJ
T_L	Maximum Temperature for Soldering	300	$^\circ\text{C}$
T_J and T_{STG}	Operating Junction and Storage Temperature Range (NOTE *1)	150, -55 to 150	

Thermal Resistance

Symbol	Parameter	Typ.	Units	Test Conditions
$R_{\theta JC}$	Junction-to-Case	3.57	$^\circ\text{C}/\text{W}$	Water cooled heatsink, P_D adjusted for a peak junction temperature of $+150^\circ\text{C}$.
$R_{\theta JA}$	Junction-to-Ambient	62.5		1 cubic foot chamber, free air.



ITA07N65R

OFF Characteristics $T_C=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	650	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=650V, V_{GS}=0V$ $T_J=25^\circ\text{C}$
		--	--	100		$V_{DS}=520V, V_{GS}=0V$ $T_J=125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	--	--	+100	nA	$V_{GS}=+30V$
	Gate-to-Source Reverse Leakage	--	--	-100		$V_{GS}=-30V$

ON Characteristics $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance (NOTE *3)	--	1.2	1.4	Ω	$V_{GS}=10V, I_D=3.5A$
$V_{GS(TH)}$	Gate Threshold Voltage	2	--	4	V	$V_{DS}=V_{GS}, I_D=250\mu A$
g_{fs}	Forward Transconductance (NOTE *3)	--	6.5	--	S	$V_{DS}=15V, I_D=3.5A$

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
C_{iss}	Input Capacitance	--	1130	--	pF	$V_{GS}=0V, V_{DS}=25V$ $f=1.0MHz$
C_{oss}	Output Capacitance	--	93	--		
C_{rss}	Reverse Transfer Capacitance	--	5.5	--		
Q_g	Total Gate Charge	--	24	--	nC	$I_D=7A, V_{DD}=520V$ $V_{GS}=10V$
Q_{gs}	Gate-to-Source Charge	--	5.1	--		
Q_{gd}	Gate-to-Drain ("Miller") Charge	--	9.5	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	19		ns	$V_{DD}=325V, I_D=7A,$ $V_G=10V, R_G=10\Omega$
t_{rise}	Rise Time	--	21			
$t_{d(OFF)}$	Turn-Off Delay Time	--	42			
t_{fall}	Fall Time	--	19			



ITA07N65R

Source-Drain Diode Characteristics

T_c=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	--	--	7	A	T _C =25°C
I _{SM}	Maximum Pulsed Current (Body Diode)	--	--	28	A	
V _{SD}	Diode Forward Voltage	--	--	1.5	V	I _{SD} =7A, V _{GS} =0V
t _{rr}	Reverse Recovery Time	--	382	--	ns	I _F = I _S di/dt=100A/us
Q _{rr}	Reverse Recovery Charge	--	1980	--	nC	

Notes:

- *1. T_J = +25°C to +150°C.
- *2. Repetitive rating; pulse width limited by maximum junction temperature.
- *3. Pulse width < 380µs; duty cycle < 2%.

Characteristics Curve:

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

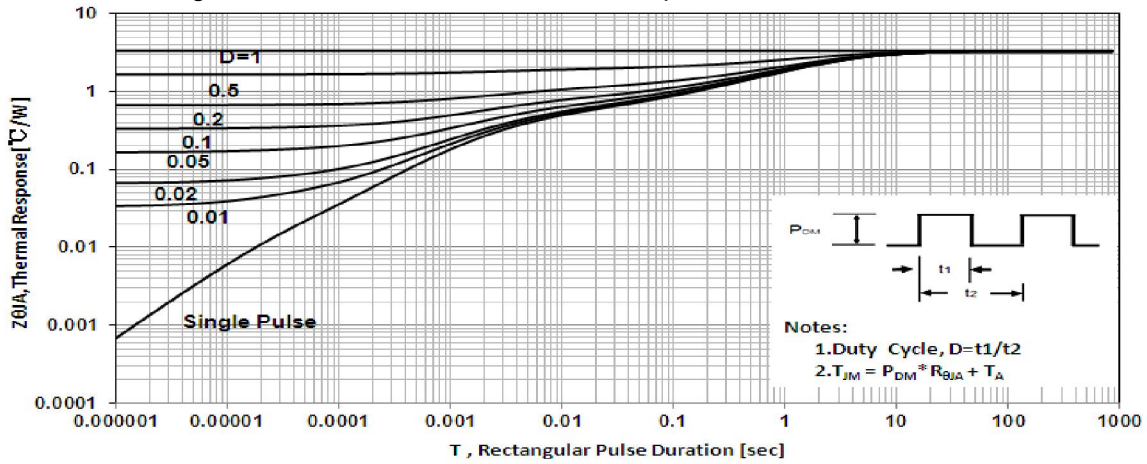


Figure 2. Typical Output Characteristics

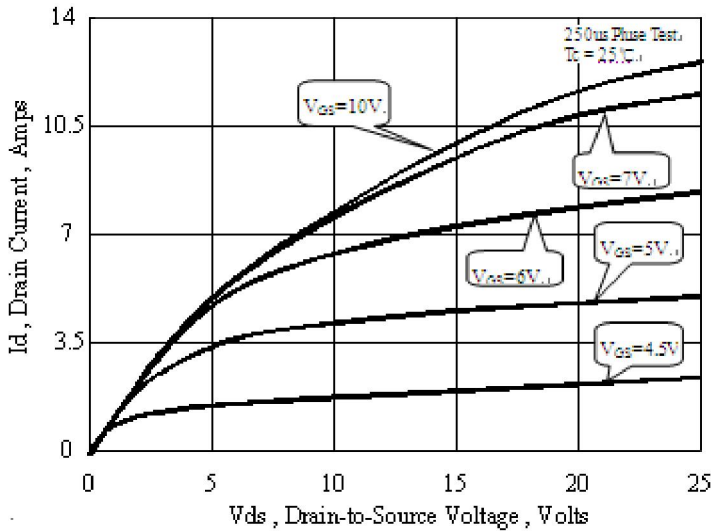


Figure 3. Typical Transfer Characteristics

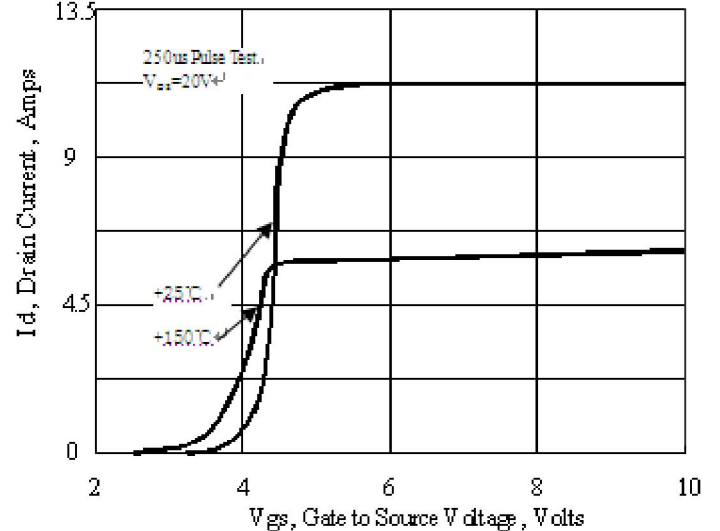


Figure 4. Typical Body Diode Transfer Characteristics

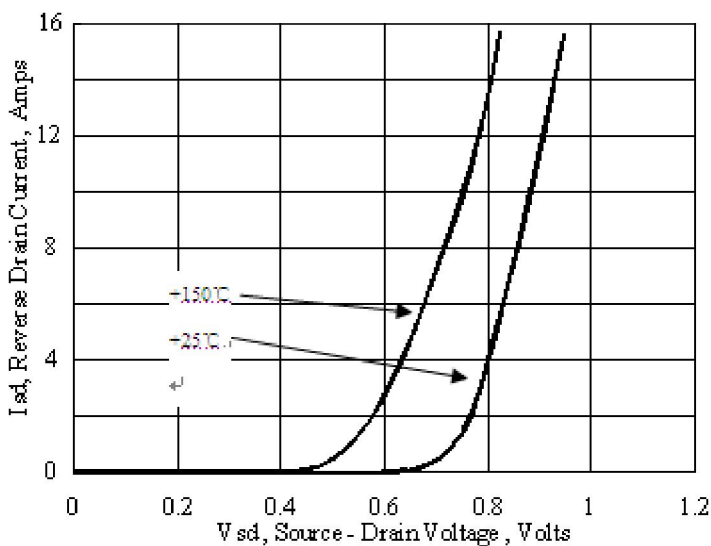


Figure 5. Typical Drain-to-source on Resistance VS Drain Current

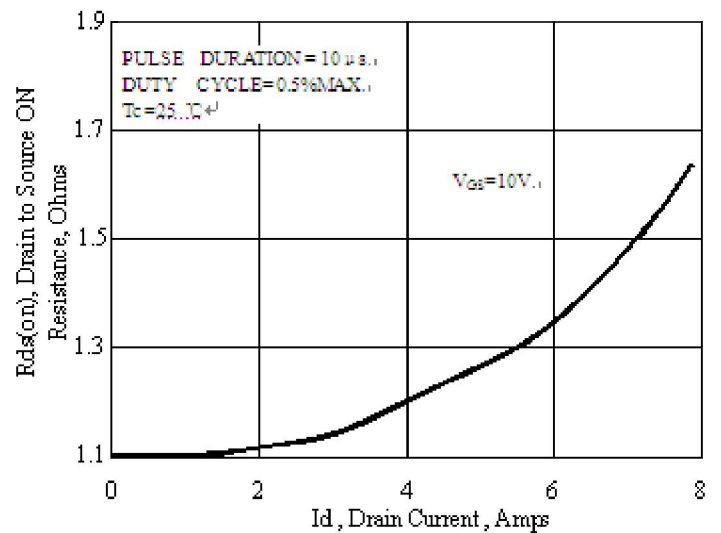


Figure 6. Capacitance VS Drain-to-Source Voltage

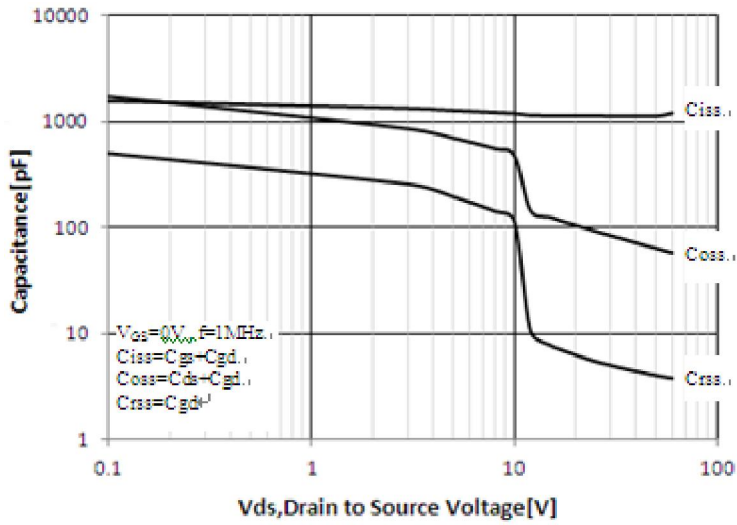


Figure 7. Gate Charge VS Gate-to-Source Voltage

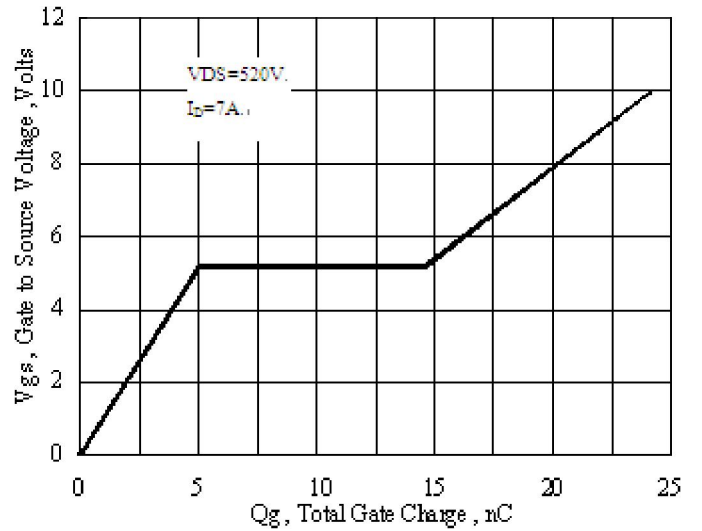


Figure 8. Breakdown Voltage VS Temperature

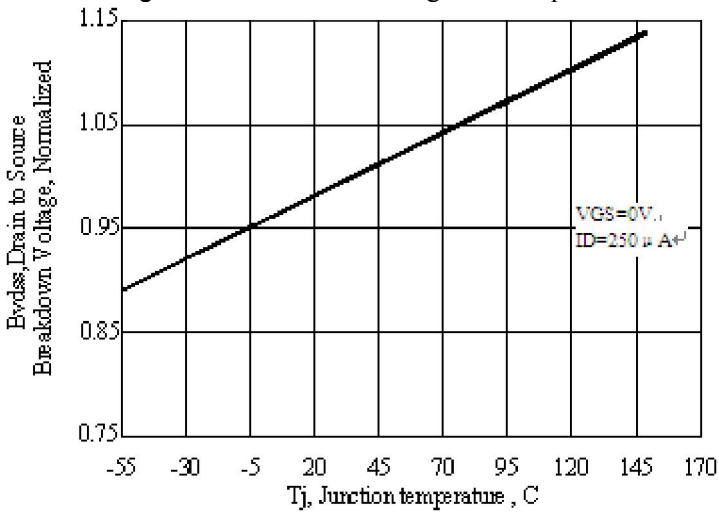


Figure 9. on-Resistance VS Temperature

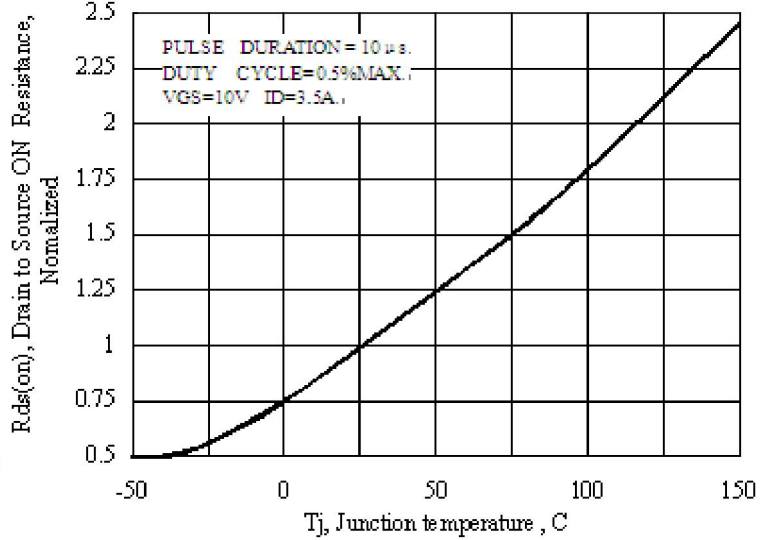
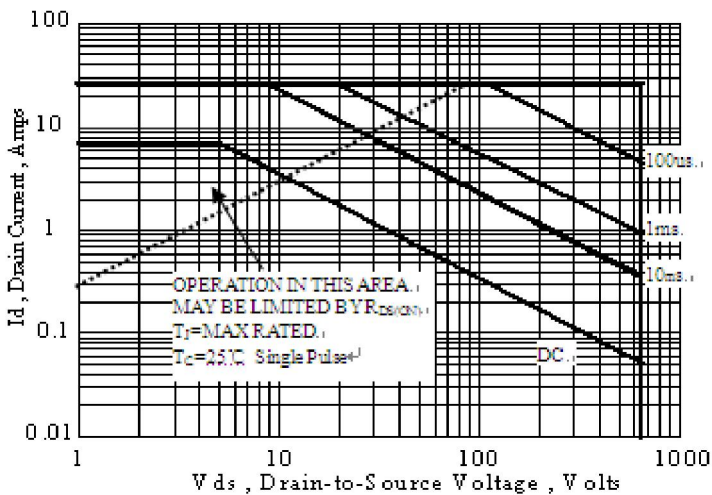


Figure 10. Safe Operating Area



Test Circuits and Waveforms

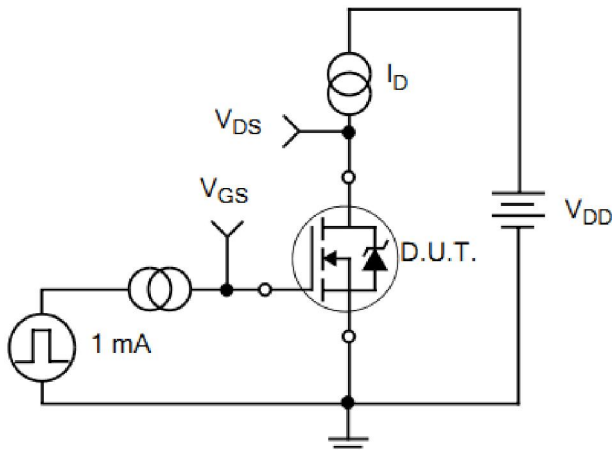


Figure 11. Gate Charge Test Circuit

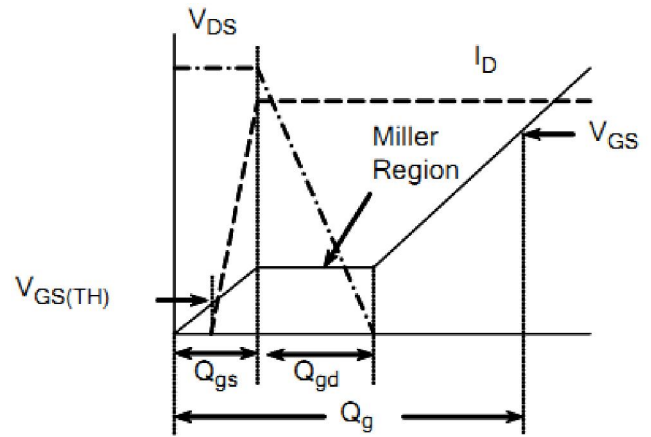


Figure 12. Gate Charge Waveforms

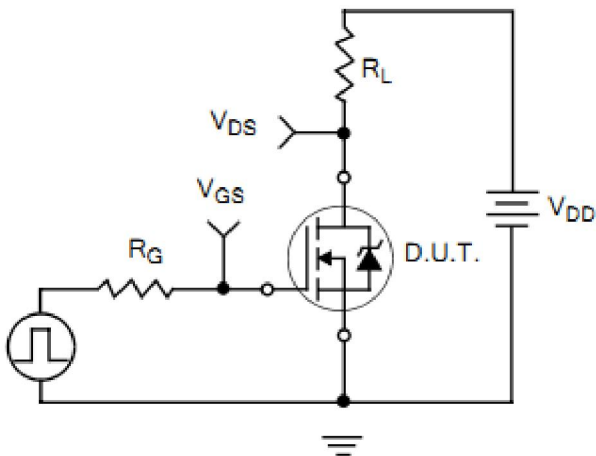


Figure 13. Resistive Switching Test Circuit

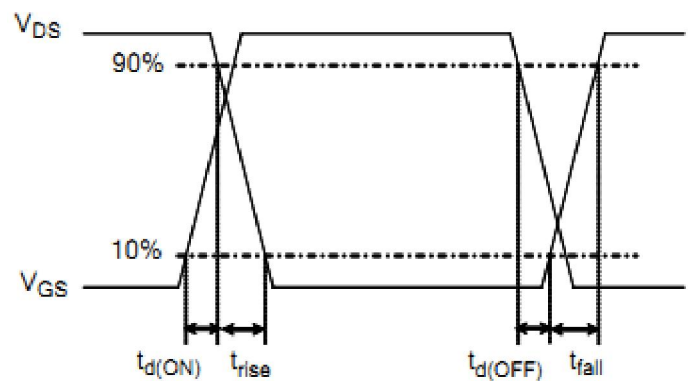


Figure 14. Resistive Switching Waveforms

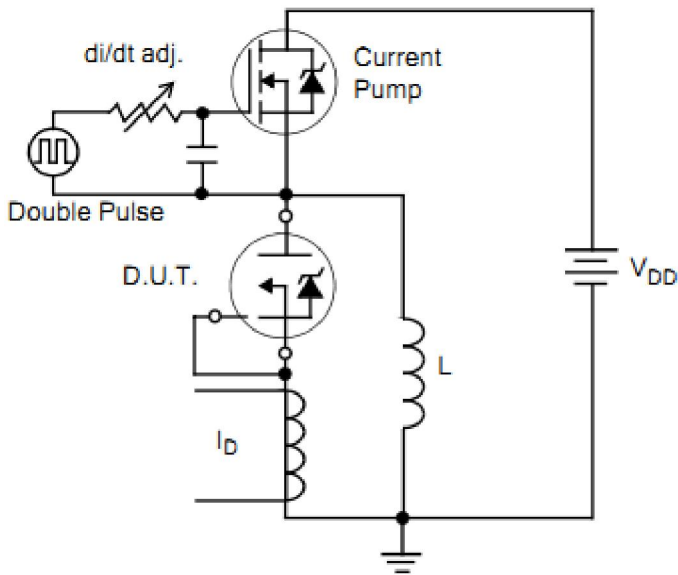


Figure 15. Diode Reverse Recovery Test Circuit

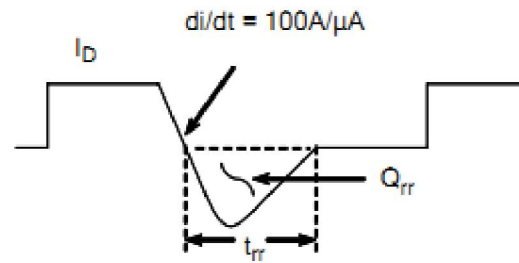


Figure 16. Diode Reverse Recovery Waveform

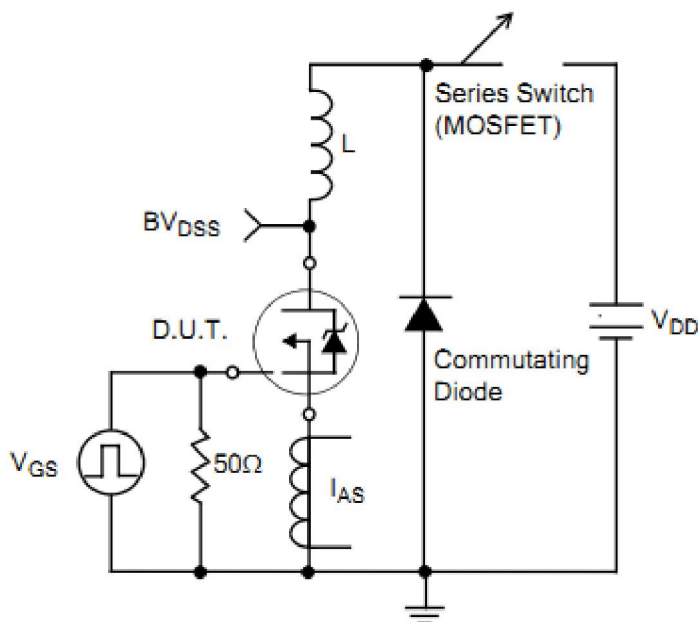


Figure 17. Unclamped Inductive Switching Test Circuit

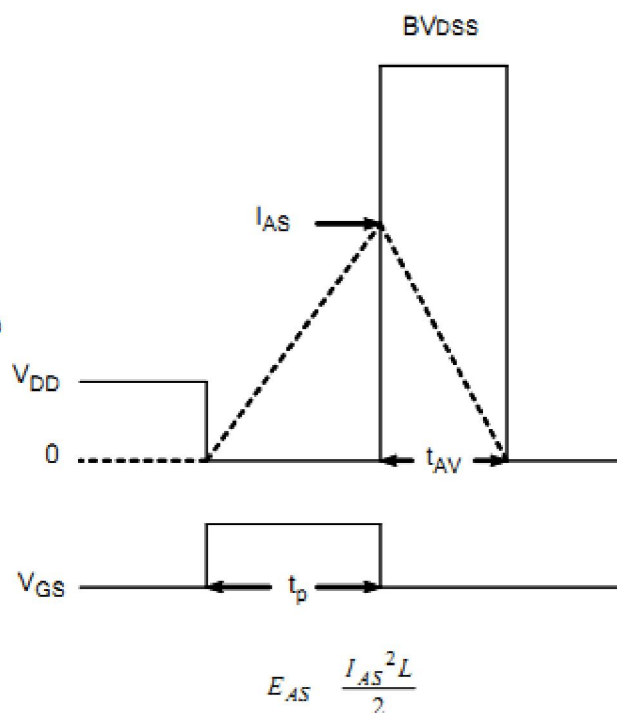


Figure 18. Unclamped Inductive Switching Waveform



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