



**ABSOLUTE MAXIMUM RATINGS \***

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN,OUT</sub>	-0.5 to 7.0	V
Voltage on Vcc Supply Relative to Vss	V <sub>CC</sub>	-0.5 to 7.0	V
Power Dissipation	P <sub>D</sub>	1.0	W
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C
Operating Temperature	T <sub>A</sub>	0 to 70	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** (T<sub>A</sub>=0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V <sub>CC</sub>	4.5	5.0	5.5	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.5	V
Input Low Voltage	V <sub>IL</sub>	-0.3 *	-	0.8	V

\* V<sub>IL</sub>(Min.)= -3.0V for ≤50 ns Pulse

**DC AND OPERATING CHARACTERISTICS**

(T<sub>A</sub>=0 to 70°C, V<sub>CC</sub>=5V ± 10%, unless otherwise specified)

Item	Symbol	Test Condition	Min.	Typ*	Max.	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ V <sub>I/O</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
DC Operating Power Supply Current	I <sub>CC</sub>	$\overline{CS}=V_{IL}$ , V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , I <sub>I/O</sub> =0mA	-	-	25	mA	
Average Operating Current	I <sub>CC1</sub>	Cycle Time=1μs, 100%Duty $\overline{CS} \leq 0.2V$ , V <sub>IH</sub> ≥V <sub>CC</sub> -0.2V V <sub>IL</sub> ≤0.2V, I <sub>I/O</sub> =0mA	-	-	20	mA	
	I <sub>CC2</sub>	Min Cycle, 100% Duty, $\overline{CS}=V_{IL}$ V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , I <sub>I/O</sub> =0mA	-	-	70	mA	
Standby Power Supply Current	I <sub>SB</sub>	$\overline{CS}=V_{IH}$	-	-	3	mA	
	I <sub>SB1</sub>	$\overline{CS} \geq V_{CC}-0.2V$ V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V	L	-	-	100	μA
			L-L	-	-	20	μA
Output Low Voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1 mA	-	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>OH</sub> =-1.0 mA	2.4	-	-	V	

Typ\* : V<sub>CC</sub>=5V, T<sub>A</sub>=25°C



**CAPACITANCE** \* (f=1MHz, TA=25 °C)

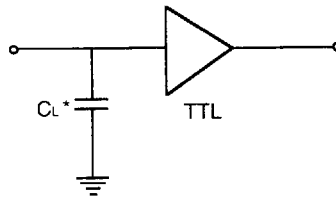
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	8	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>IO</sub> =0V	-	10	pF

\* Note: Capacitance is sampled and not 100% tested.

**TEST CONDITIONS**

(TA= 0 to 70 °C, Vcc=5V ±10%, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> =100pF+1TTL



\* Including Scope and Jig Capacitance

**READ CYCLE**

Parameter	Symbol	KM684000L-5 KM684000L-5L		KM684000L-7 KM684000L-7L		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	trc	55	-	70	-	ns
Address Access Time	tAA	-	55	-	70	ns
Chip Select to Output	tCO	-	55	-	70	ns
Output Enable to Valid Output	tOE	-	25	-	35	ns
Chip Select to Low-Z Output	tLZ	10	-	10	-	ns
Output Enable to Low-Z Output	tOLZ	5	-	5	-	ns
Chip Disable to High-Z Output	tHZ	0	20	0	25	ns
Output Disable to High-Z Output	tOHZ	0	20	0	25	ns
Output Hold from Address Change	tOH	10	-	10	-	ns

**WRITE CYCLE**

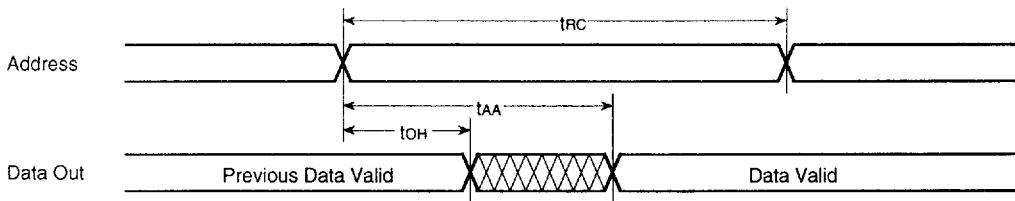
Parameter	Symbol	KM684000L-5 KM684000L-5L		KM684000L-7 KM684000L-7L		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t <sub>wc</sub>	55	-	70	-	ns
Chip Select to End of Write	t <sub>cw</sub>	45	-	60	-	ns
Address Set-up Time	t <sub>as</sub>	0	-	0	-	ns
Address Valid to End of Write	t <sub>aw</sub>	45	-	60	-	ns
Write Pulse Width	t <sub>wp</sub>	40	-	50	-	ns
Write Recovery Time	t <sub>wr</sub>	0	-	0	-	ns
Write to Output High-Z	t <sub>whz</sub>	0	25	0	30	ns
Data to Write Time Overlap	t <sub>dw</sub>	25	-	30	-	ns
Data Hold from Write Time	t <sub>dh</sub>	0	-	0	-	ns
End Write to Output Low-Z	t <sub>ow</sub>	5	-	5	-	ns

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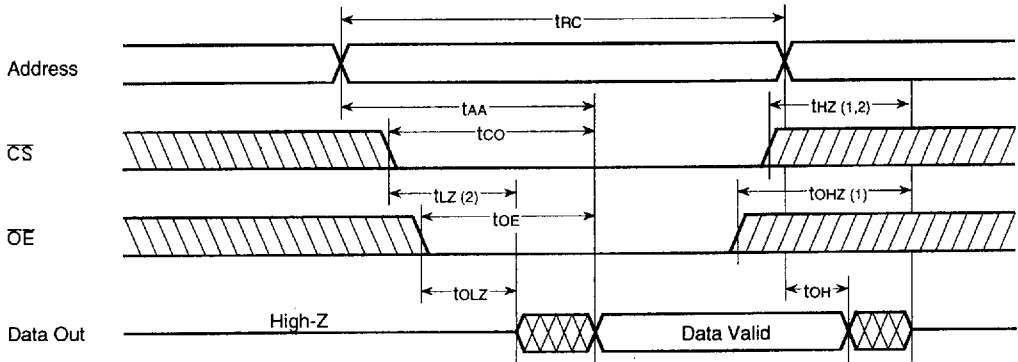
**TIMING DIAGRAMS**

**TIMING WAVEFORM OF READ CYCLE(1)** (Address Controlled)

( $\overline{CS} = \overline{OE} = V_{IL}$ ,  $\overline{WE} = V_{IH}$ )



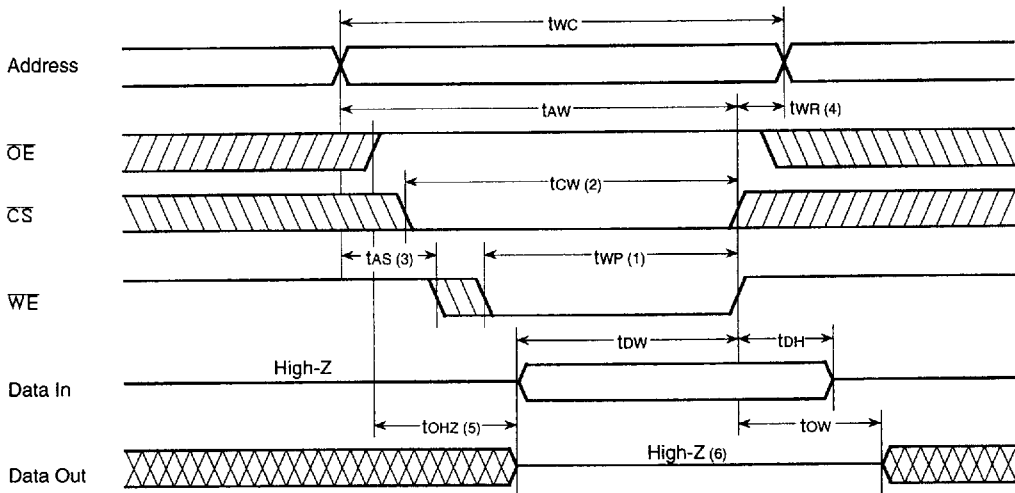
**TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )**



**NOTES (READ CYCLE)**

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are referenced to the  $V_{OH}$  or  $V_{OL}$ .
2. At any given temperature and voltage condition  $t_{HZ}(\max)$  is less than  $t_{LZ}(\min)$  both for a given device and from device to device.
3.  $\overline{WE}$  is high for read cycle.
4. Address valid prior to or coincident with  $\overline{CS}$  transition Low.

**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}$  Clock)**





**DATA RETENTION CHARACTERISTICS** (Ta= 0 to 70 °C)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Vcc for Data Retention	Vdr	$\overline{CS} \geq V_{cc} - 0.2V$	2.0	-	5.5	V
Data Retention Current	Idr	Vcc=3.0V $\overline{CS} \geq V_{cc} - 0.2V$	L	-	50*	$\mu A$
			L-L	-	10**	$\mu A$
Data Retention Set-up Time	tSDR	See Data Retention	0	-	-	ns
Recovery Time	tRDR	Waveforms (below)	5	-	-	ms

\* 20  $\mu A$  (max.) at 0 °C to 40 °C

\*\* 3  $\mu A$  (max.) at 0 °C to 40 °C

**DATA RETENTION WAVEFORM 1** ( $\overline{CS}$  Controlled)

