



5-Pin Microprocessor Supervisory Circuits

General Description

The MAX823/MAX824/MAX825* microprocessor (μ P) supervisory circuits combine reset output, watchdog, and manual-reset input functions in a 5-pin SOT23-5 package. They significantly improve system reliability and accuracy compared to separate ICs or discrete components. The MAX823/MAX824/MAX825 are specifically designed to ignore fast transients on VCC.

Five preprogrammed reset threshold voltages are available, designated by the following package suffixes: L = 4.63V, M = 4.38V, T = 3.08V, S = 2.93V, and R = 2.63V. All three devices have an active-low reset output, which is guaranteed to be in the correct state for VCC down to 1V. The MAX824/MAX825 also have an active-high reset output. The following *Selector Guide* explains the functions offered in this series of parts.

Applications

Battery-Powered Computers and Controllers
 Embedded Controllers
 Intelligent Instruments
 Automotive Systems
 Critical μ P Monitoring
 Portable/Battery-Powered Equipment

Selector Guide

FUNCTION	MAX823	MAX824	MAX825
Active-Low Reset	✓	✓	✓
Active-High Reset	—	✓	✓
Watchdog Input	✓	✓	—
Manual-Reset Input	✓	—	✓

Typical Operating Circuit appears at end of data sheet.

Marking Information appears at end of data sheet.

Features

- ◆ Precision Monitoring of +3V, +3.3V, and +5V Power Supplies
- ◆ Operating Current: 10 μ A (MAX823L/M)
3 μ A (MAX825T/S/R)
- ◆ Fully Specified Over Temperature
- ◆ 140ms Min Power-On Reset
- ◆ Guaranteed $\overline{\text{RESET}}$ Valid to VCC = 1V
- ◆ Power-Supply Transient Immunity
- ◆ Watchdog Timer with 1.6sec Timeout (MAX823/MAX824)
- ◆ Manual-Reset Input (MAX823/MAX825)
- ◆ No External Components

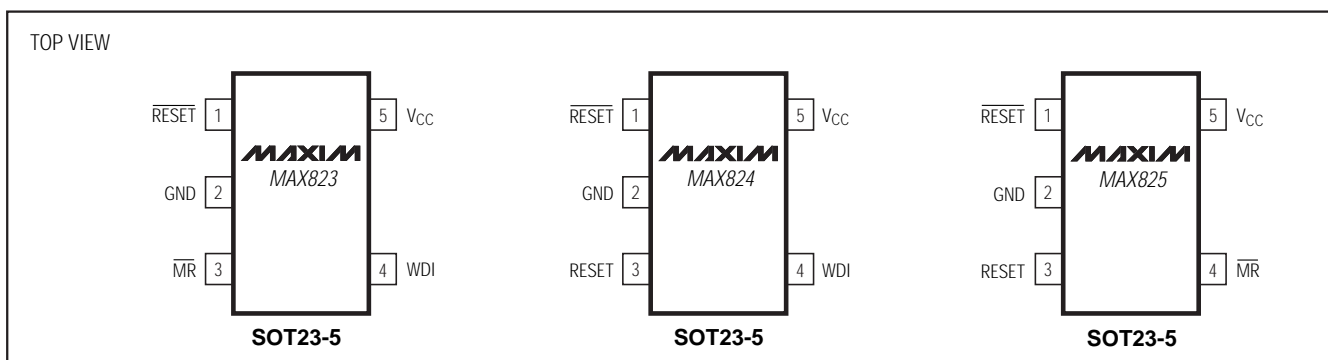
Ordering Information

PART [†]	TEMP. RANGE	PIN-PACKAGE
MAX823_EUK	-40°C to +85°C	5 SOT23-5
MAX824_EUK	-40°C to +85°C	5 SOT23-5
MAX825_EUK	-40°C to +85°C	5 SOT23-5

[†]Insert the desired suffix letter (from the table below) into the blank to complete the part number.

SUFFIX	RESET THRESHOLD (V)
L	4.63
M	4.38
T	3.08
S	2.93
R	2.63

Pin Configurations



*Patents Pending



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ABSOLUTE MAXIMUM RATINGS

V_{CC}-0.3V to +6.0V
 All Other Pins-0.3V to (V_{CC} + 0.3V)
 Input Current, All Pins Except RESET and $\overline{\text{RESET}}$ 20mA
 Output Current, RESET, $\overline{\text{RESET}}$ 20mA
 Rate of Rise, V_{CC}100V/ μ s
 Continuous Power Dissipation (T_A = +70°C)
 SOT23-5 (derate 7.1mW/°C above +70°C)571mW

Operating Temperature Range
 MAX82_EUK-40°C to +85°C
 Storage Temperature Range-65°C to +160°C
 Lead Temperature (soldering, 10sec)+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +4.75V to +5.5V for MAX82_L, V_{CC} = +4.5V to +5.5V for MAX82_M, V_{CC} = +3.15V to +3.6V for MAX82_T, V_{CC} = +3V to +3.6V for MAX82_S, V_{CC} = +2.7V to +3.6V for MAX82_R, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Operating Voltage Range	V _{CC}	T _A = 0°C to +70°C	1.0		5.5	V	
		T _A = -40°C to +85°C	1.2				
Supply Current	I _{SUPPLY}	WDI and $\overline{\text{MR}}$ unconnected	MAX823L/M, MAX824L/M	10	24	μ A	
			MAX823T/S/R, MAX824T/S/R	5	12		
		$\overline{\text{MR}}$ unconnected	MAX825L/M	4.5	12		
			MAX825T/S/R	3	8		
Reset Threshold	V _{RST}	MAX82_L	T _A = +25°C	4.56	4.63	4.70	V
			T _A = -40°C to +85°C	4.50		4.75	
		MAX82_M	T _A = +25°C	4.31	4.38	4.45	
			T _A = -40°C to +85°C	4.25		4.50	
		MAX82_T	T _A = +25°C	3.04	3.08	3.11	
			T _A = -40°C to +85°C	3.00		3.15	
		MAX82_S	T _A = +25°C	2.89	2.93	2.96	
			T _A = -40°C to +85°C	2.85		3.00	
MAX82_R	T _A = +25°C	2.59	2.63	2.66			
	T _A = -40°C to +85°C	2.55		2.70			
Reset Threshold Hysteresis		MAX82_L/M		10		mV	
		MAX82_T/S/R		5			
Reset Threshold Temperature Coefficient				40		ppm/°C	
Reset Timeout Period	t _{RP}	MAX82_L/M	140	200	280	ms	
		MAX82_T/S/R	140	200	280		

5-Pin Microprocessor Supervisory Circuits

MAX823/MAX824/MAX825

ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = +4.75V$ to $+5.5V$ for MAX82_L, $V_{CC} = +4.5V$ to $+5.5V$ for MAX82_M, $V_{CC} = +3.15V$ to $+3.6V$ for MAX82_T, $V_{CC} = +3V$ to $+3.6V$ for MAX82_S, $V_{CC} = +2.7V$ to $+3.6V$ for MAX82_R, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
\overline{RESET} Output Voltage	V_{OH}	MAX82_L/M, $V_{CC} = V_{RST\ max}$, $I_{SOURCE} = 120\mu A$	$V_{CC} - 1.5$			V
		MAX82_T/S/R, $V_{CC} = V_{RST\ max}$, $I_{SOURCE} = 30\mu A$	$0.8V_{CC}$			
	V_{OL}	MAX82_L/M, $V_{CC} = V_{RST\ min}$, $I_{SINK} = 3.2mA$	0.4			
		MAX82_T/S/R, $V_{CC} = V_{RST\ min}$, $I_{SINK} = 1.2mA$	0.3			
		$T_A = 0^{\circ}C$ to $+70^{\circ}C$, $V_{CC} = 1V$, V_{CC} falling, $I_{SINK} = 50\mu A$	0.3			
		$T_A = -40^{\circ}C$ to $+85^{\circ}C$, $V_{CC} = 1.2V$, V_{CC} falling, $V_{BATT} = 0V$, $I_{SINK} = 100\mu A$	0.3			
\overline{RESET} Output Short-Circuit Current (Note 2)	I_{SOURCE}	MAX82_L/M, $\overline{RESET} = 0V$, $V_{CC} = 5.5V$	800			μA
		MAX82_T/S/R, $\overline{RESET} = 0V$, $V_{CC} = 3.6V$	400			
RESET Output Voltage	V_{OH}	$V_{CC} > 1.8V$, $I_{SOURCE} = 150\mu A$	$0.8V_{CC}$			V
	V_{OL}	MAX824L/M, MAX825L/M, $V_{CC} = V_{RST\ max}$, $I_{SINK} = 3.2mA$	0.4			
		MAX824T/S/R, MAX825T/S/R, $V_{CC} = V_{RST\ max}$, $I_{SINK} = 1.2mA$	0.3			
V_{CC} to \overline{RESET} Delay		$V_{RST} - V_{CC} = 100mV$	20			μs
WATCHDOG INPUT (MAX823/MAX824)						
Watchdog Timeout Period	t_{WD}		1.12	1.60	2.40	sec
WDI Pulse Width	t_{WDI}	$V_{IL} = 0.4V$, $V_{IH} = 0.8V_{CC}$	50			ns
WDI Input Threshold (Note 3)	V_{IL}	$V_{CC} = 5V$	0.3 V_{CC}			V
	V_{IH}		0.7 V_{CC}			
WDI Input Current (Note 4)		WDI = V_{CC} , time average	120			μA
		WDI = $0V$, time average	-20			
MANUAL-RESET INPUT (MAX823/MAX825)						
\overline{MR} Input Threshold	V_{IL}		0.3 V_{CC}			V
	V_{IH}		0.7 V_{CC}			
\overline{MR} Pulse Width			1.0			μs
\overline{MR} Noise Immunity (pulse width with no reset)			100			ns
\overline{MR} to Reset Delay			500			ns
\overline{MR} Pull-Up Resistance (internal)			35	52	75	$k\Omega$

Note 1: Over-temperature limits are guaranteed by design and not production tested.

Note 2: The \overline{RESET} short-circuit current is the maximum pull-up current when \overline{RESET} is driven low by a μP bidirectional reset pin.

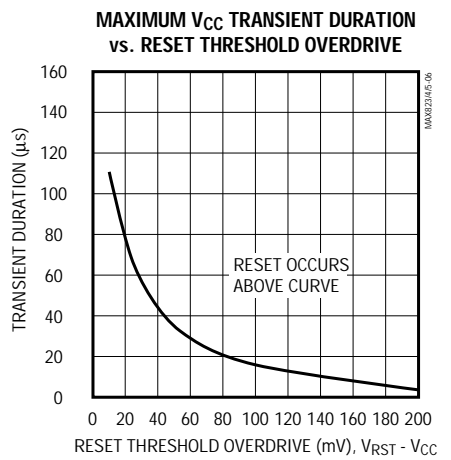
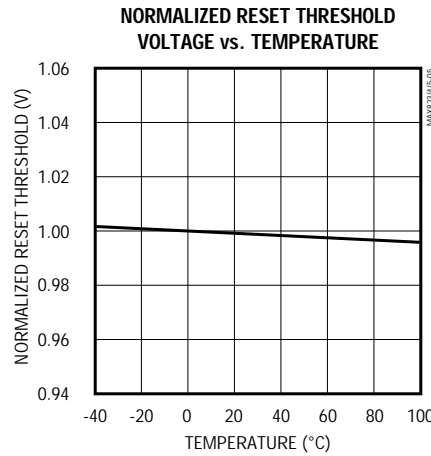
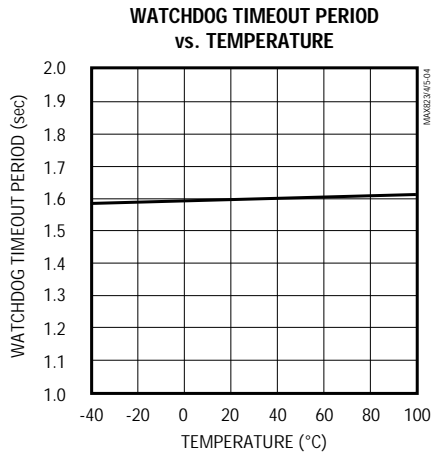
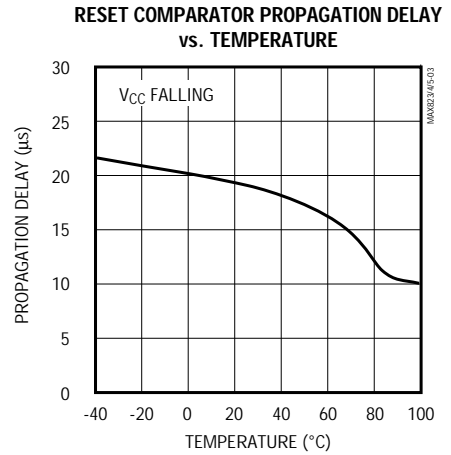
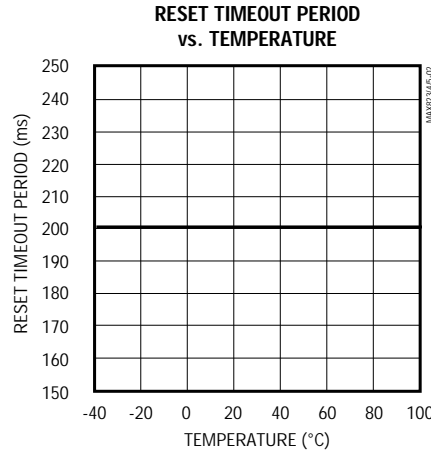
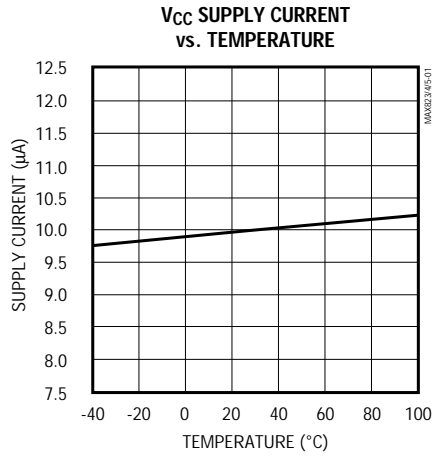
Note 3: WDI is internally serviced within the watchdog period if WDI is left unconnected.

Note 4: The WDI input current is specified as the average input current when the WDI input is driven high or low. The WDI input is designed to drive a three-stated-output device with a $10\mu A$ maximum leakage current and a maximum capacitive load of $200pF$. This output device must be able to source and sink at least $200\mu A$ when active.

5-Pin Microprocessor Supervisory Circuits

Typical Operating Characteristics

(MAX823L, $V_{CC} = +5V$, $T_A = +25^{\circ}C$, unless otherwise noted.)



5-Pin Microprocessor Supervisory Circuits

Pin Description

MAX823/MAX824/MAX825

PIN			NAME	FUNCTION
MAX823	MAX824	MAX825		
1	1	1	$\overline{\text{RESET}}$	Active-Low Reset Output. Pulses low for 200ms when triggered, and remains low whenever V_{CC} is below the reset threshold or when $\overline{\text{MR}}$ is a logic low. It remains low for 200ms after one of the following occurs: V_{CC} rises above the reset threshold, the watchdog triggers a reset, or $\overline{\text{MR}}$ goes low to high.
2	2	2	GND	Ground. 0V reference for all signals.
3	—	4	$\overline{\text{MR}}$	Manual-Reset Input. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted as long as $\overline{\text{MR}}$ is held low and for 200ms after $\overline{\text{MR}}$ returns high. The active-low input has an internal 52k Ω pull-up resistor. It can be driven from a CMOS-logic line or shorted to ground with a switch. Leave open or connect to V_{CC} if unused.
—	3	3	RESET	Active-High Reset Output. Inverse of $\overline{\text{RESET}}$.
4	4	—	WDI	Watchdog Input. If WDI remains either high or low for longer than the watchdog timeout period, the internal watchdog timer runs out and a reset is triggered. The internal watchdog timer clears whenever reset is asserted, or whenever WDI sees a rising or falling edge. If WDI is left unconnected or is connected to a three-stated buffer output, the watchdog feature is disabled.
5	5	5	V_{CC}	Supply Voltage

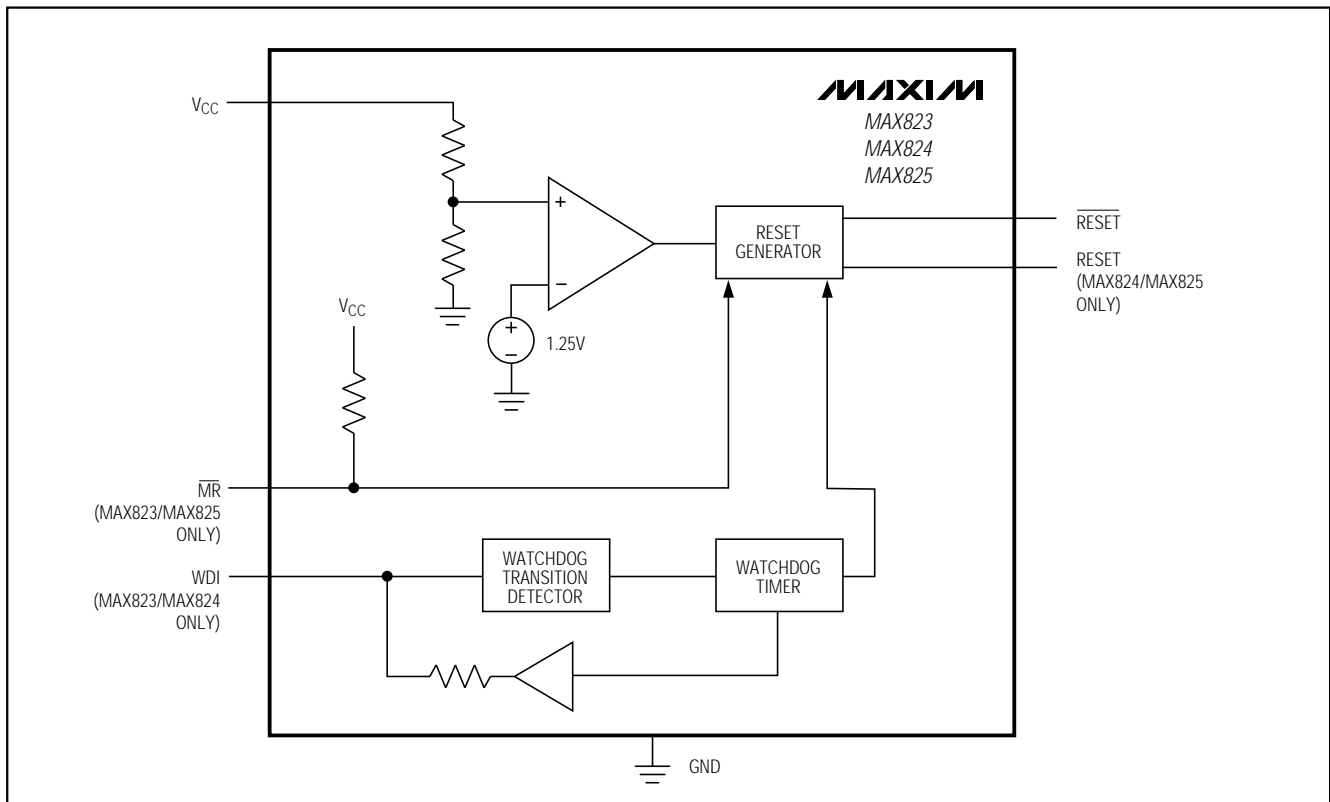


Figure 1. Functional Diagram

5-Pin Microprocessor Supervisory Circuits

Detailed Description

$\overline{\text{RESET}}$ Output

A microprocessor's (μP 's) reset input starts the μP in a known state. The MAX823/MAX824/MAX825 μP supervisory circuits assert a reset to prevent code-execution errors during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ is guaranteed to be a logic low for V_{CC} down to 1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{\text{RESET}}$ low for the specified reset timeout period (t_{RP}); after this interval, $\overline{\text{RESET}}$ returns high (Figure 2).

If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{\text{RESET}}$ goes low. Each time $\overline{\text{RESET}}$ is asserted it stays low for the reset timeout period. Any time V_{CC} goes below the reset threshold the internal timer restarts. $\overline{\text{RESET}}$ both sources and sinks current. $\overline{\text{RESET}}$ on the MAX824/MAX825 is the inverse of $\overline{\text{RESET}}$.

Manual-Reset Input (MAX823/MAX825)

Many μP -based products require manual-reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. On the MAX823/MAX825, a logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted while $\overline{\text{MR}}$ is low, and for t_{RP} (200ms nominal) after it returns high. $\overline{\text{MR}}$ has an internal 52k Ω pull-up resistor, so it can be left open if not used. This input can be driven with CMOS-logic levels or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{\text{MR}}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1 μF capacitor from $\overline{\text{MR}}$ to GND to provide additional noise immunity.

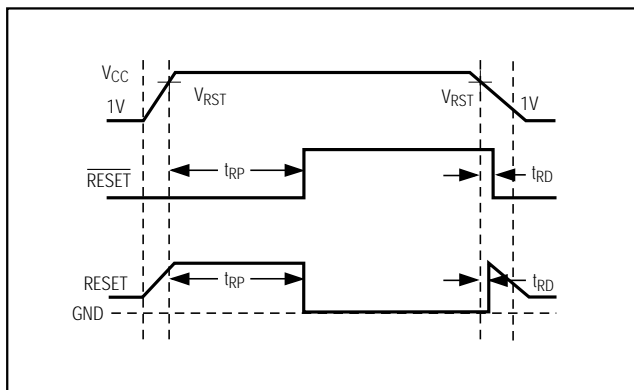


Figure 2. Reset Timing Diagram

Watchdog Input (MAX823/MAX824)

In the MAX823/MAX824, the watchdog circuit monitors the μP 's activity. If the μP does not toggle the watchdog input (WDI) within t_{WD} (1.6sec), reset asserts. The internal 1.6sec timer is cleared by either a reset pulse or by toggling WDI, which detects pulses as short as 50ns. While reset is asserted, the timer remains cleared and does not count. As soon as reset is released, the timer starts counting (Figure 3).

Disable the watchdog function by leaving WDI unconnected or by three-stating the driver connected to WDI. The watchdog input is internally driven low during the first 7/8 of the watchdog timeout period and high for the last 1/8 of the watchdog timeout period. When WDI is left unconnected, this internal driver clears the 1.6sec timer every 1.4sec. When WDI is three-stated or unconnected, the maximum allowable leakage current is 10 μA and the maximum allowable load capacitance is 200pF.

Applications Information

Watchdog Input Current

The MAX823/MAX824 WDI inputs are internally driven through a buffer and series resistor from the watchdog counter (Figure 1). When WDI is left unconnected, the watchdog timer is serviced within the watchdog timeout period by a low-high-low pulse from the counter chain. For minimum watchdog input current (minimum overall power consumption), leave WDI low for the majority of the watchdog timeout period, pulsing it low-high-low once within the first 7/8 of the watchdog timeout period to reset the watchdog timer. If WDI is externally driven high for the majority of the timeout period, up to 160 μA can flow into WDI.

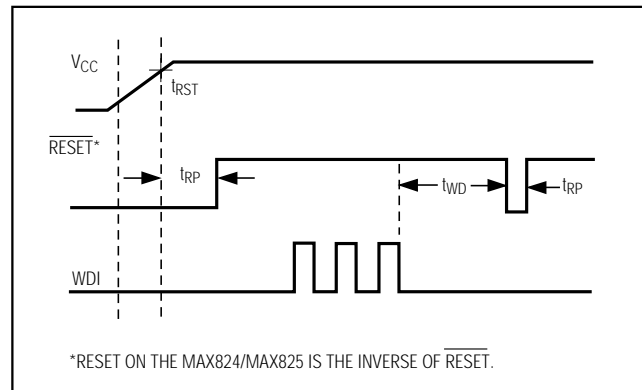


Figure 3. MAX823/MAX824 Watchdog Timing Relationship

5-Pin Microprocessor Supervisory Circuits

Interfacing to μ Ps with Bidirectional Reset Pins

The $\overline{\text{RESET}}$ output maximum pull-up current is 800 μ A for L/M versions (400 μ A for T/S/R versions). This allows μ Ps with bidirectional resets, such as the 68HC11, to force $\overline{\text{RESET}}$ low when the MAX823/MAX824/MAX825 are pulling $\overline{\text{RESET}}$ high (Figure 4).

Negative-Going V_{CC} Transients

These supervisors are relatively immune to short-duration, negative-going V_{CC} transients (glitches), which usually do not require the entire system to shut down. Resets are issued to the μ P during power-up, power-down, and brownout conditions.

The *Typical Operating Characteristics* show a graph of the MAX823L's Maximum V_{CC} Transient Duration vs. Reset Threshold Overdrive, for which reset pulses are **not** generated. The graph was produced using negative-going V_{CC} pulses, starting at 5V and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a negative-going V_{CC} transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{CC} transient that goes 100mV below the reset threshold and lasts for 15 μ s or less will not trigger a reset pulse.

An optional 0.1 μ F bypass capacitor mounted close to V_{CC} provides additional transient immunity.

Watchdog Software Considerations (MAX823/MAX824)

One way to help the watchdog timer monitor software execution more closely is to set and reset the watchdog input at different points in the program, rather than pulsing the watchdog input high-low-high or low-high-low. This technique avoids a stuck loop, in which the watchdog timer would continue to be reset inside the loop, keeping the watchdog from timing out.

Figure 5 shows an example of a flow diagram where the I/O driving the watchdog input is set high at the beginning of the program, set low at the beginning of every subroutine or loop, then set high again when the program returns to the beginning. If the program should hang in any subroutine, the problem would quickly be corrected, since the I/O is continually set low and the watchdog timer is allowed to time out, causing a reset or interrupt to be issued. As described in the *Watchdog Input Current* section, this scheme results in higher time average WDI input current than does leaving WDI low for the majority of the timeout period and periodically pulsing it low-high-low.

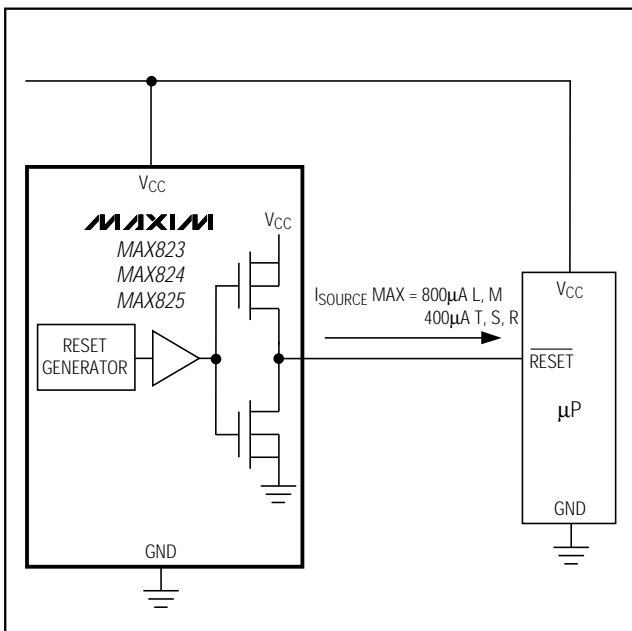


Figure 4. Interfacing to μ Ps with Bidirectional Resets

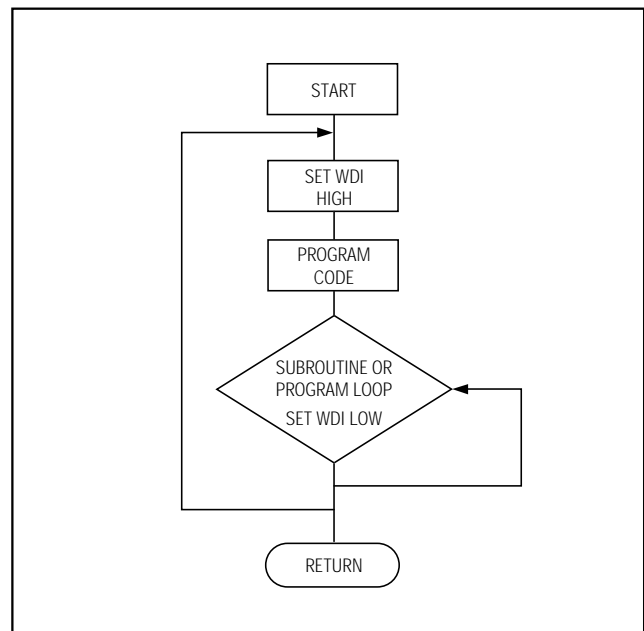
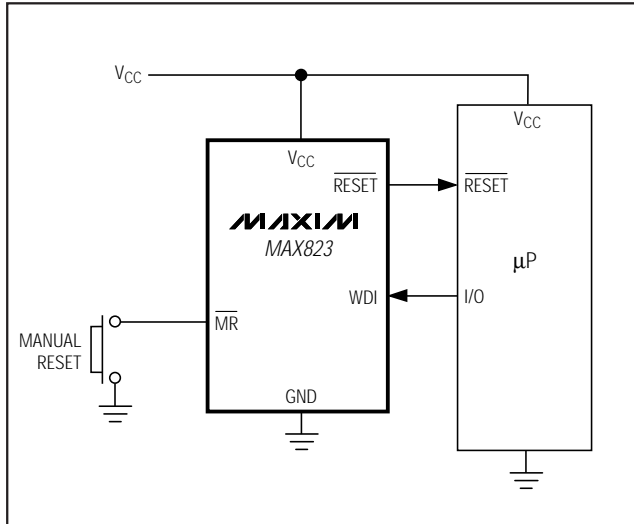


Figure 5. Watchdog Flow Diagram

5-Pin Microprocessor Supervisory Circuits

Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 607

Package Information

MARKING INFORMATION (TOP)

XXXX

- AAAI = MAX823L
- AAAJ = MAX823M
- AAAK = MAX823T
- AAAL = MAX823S
- AAAM = MAX823R
- AAAN = MAX824L
- AAAO = MAX824M
- AAAP = MAX824T
- AAAQ = MAX824S
- AAAR = MAX824R
- AAAS = MAX825L
- AAAT = MAX825M
- AAAU = MAX825T
- AAAV = MAX825S
- AAAW = MAX825R

SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.55
e		0.95 REF
e1		1.90 REF
α	0°	10°

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.

MAXIM

PREPROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, SOT23, 5L

APPROVAL	DOCUMENT CONTROL NO	REV
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