Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT2259 is an 8-pin 2-channel volume controller which utilizes CMOS technology and incorporates the I^2C interface control. The controller features an attenuation range of 0 to -79dB, low noise output, a high degree of stereo separation and requires only a small number of external components. PT2259 is an essential component for modern audio visual systems.

FEATURES

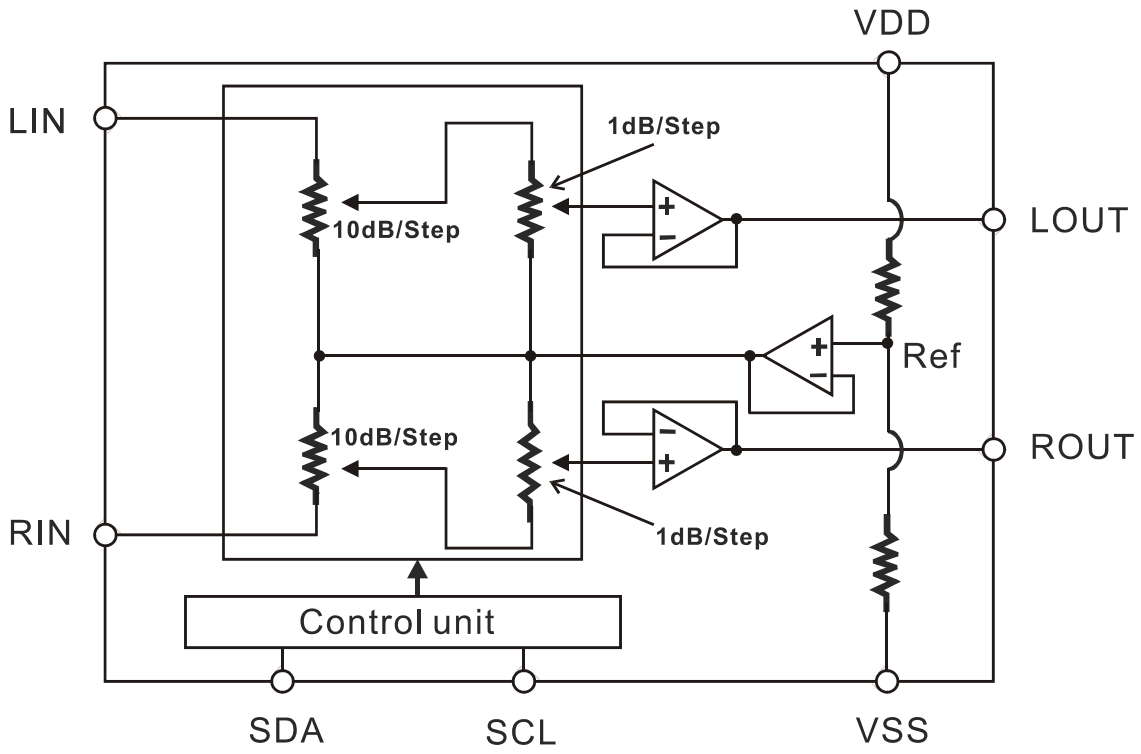
- Attenuation range: 0 to –79dB in 1dB steps
- Operating voltage: 4 to 9V
- Low power consumption
- Low signal noise: S/N > 100dB (A-weighting)
- Stereo separation > 100dB
- Requires few external components
- 2-channel volume individual adjust
- Available in 8 Pins DIP or SOP

APPLICATIONS

- Audio/visual surround sound systems
- Car audio systems
- Mini-compo systems
- Computer multi-media speakers
- Other audio applications

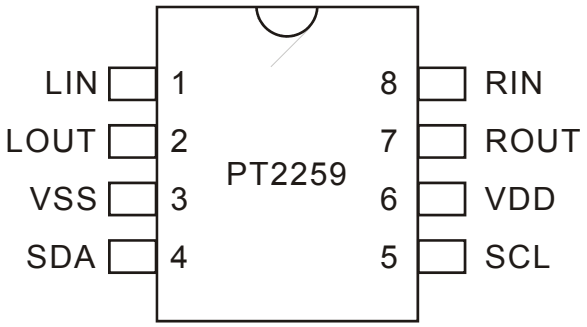
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

BLOCK DIAGRAM



Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
LIN	I	Left Channel Input (capacitor coupled to input port)	1
LOUT	O	Left Channel Output (capacitor coupled to output port)	2
VSS	-	Ground	3
SDA	I	I^2C Data Input	4
SCL	I	I^2C Clock Input	5
VDD	-	Power Supply	6
ROUT	O	Right Channel Output (capacitor coupled to input port)	7
RIN	I	Right Input Channel (capacitor coupled to output port)	8

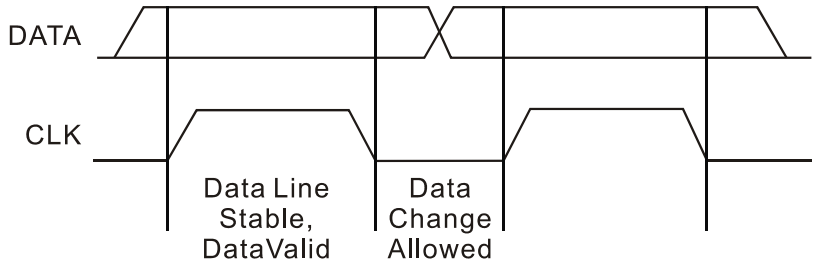
FUNCTIONAL DESCRIPTION

I²C BUS INTERFACE

In PT2259 the DATA and CLK make up the bus interface through which data is transmitted to and from the microprocessor.

DATA VALIDITY

Data on the DATA line is considered valid and stable only when the CLK signal is in the “high” state. In addition, the “high” and “low” states of the DATA line can change only when the CLK signal is in the “low” state. Please refer to the diagram below:



START AND STOP CONDITIONS

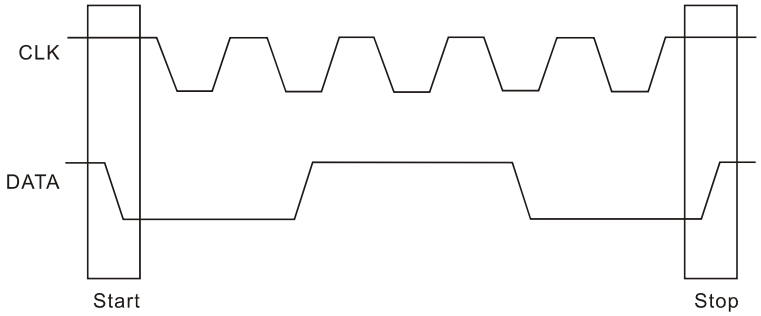
A start condition is activated when:

1. the CLK signal is set to “high”, and
2. the DATA signal shifts from “high” to “low”

A stop condition is activated when:

1. the CLK signal is set to “high”, and
2. the DATA signal shifts from “low” to “high”

Please refer to the timing diagram below:

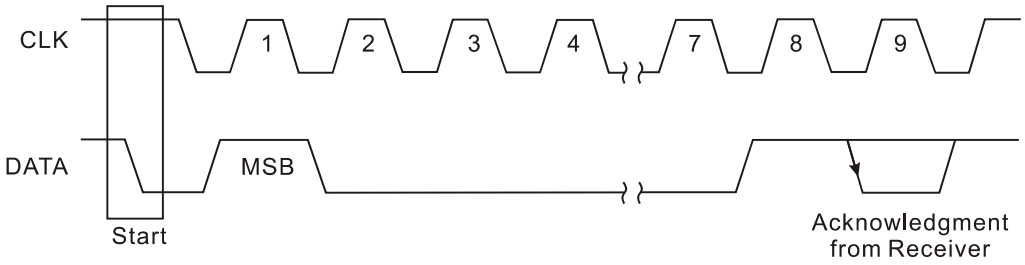


BYTE FORMAT

Every byte transmitted to the DATA line consists of 8 bits and each byte must be followed by an "acknowledge" bit. The MSB is transmitted first.

ACKNOWLEDGE SIGNAL

During the ninth clock pulse, the microprocessor puts a resistive "high" level on the DATA line. If the peripheral audio processor (PT2259) acknowledges, it will pull the DATA line from a "high" state to a "low" state during this acknowledge clock phase so that the DATA line is in a stable "low" state during this clock pulse. Please refer to the diagram below.



The audio processor that has been address (PT2259) must generate an "acknowledge" signal after receiving each byte or the DATA line will remain at the "high" level during the ninth clock pulse.

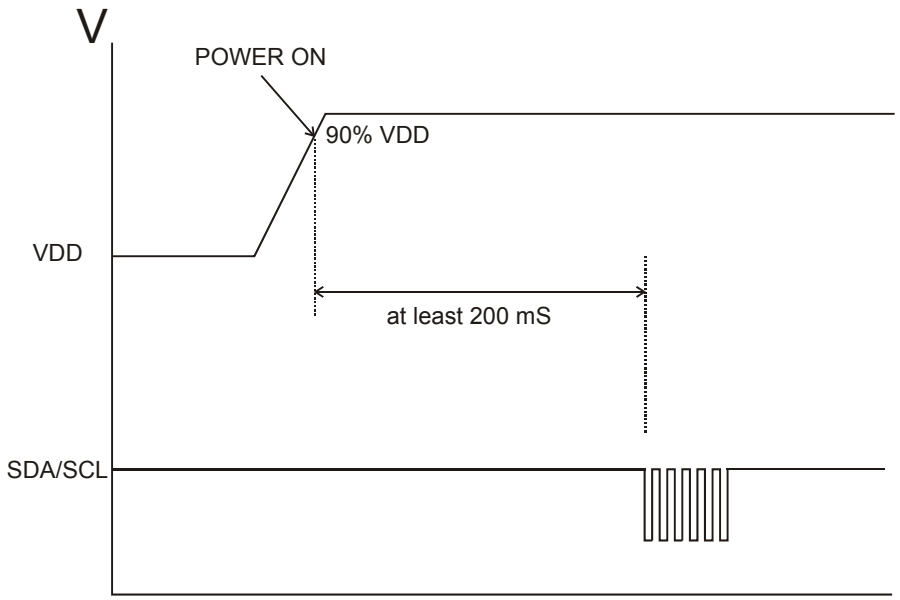
TRANSMISSION WITHOUT ACKNOWLEDGE

If you do not wish the audio processor (PT2259) to detect the "acknowledge" signal, a simpler microprocessor transmission method can be used: after PT2259 has received a byte wait for one clock pulse and do not acknowledge it. If this approach is used, however, there is a greater chance for faulty operations to occur and noise immunity will be decreased.

Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

I²C START TIME

When PT2259 is powered on, a short period must elapse before voltage becomes stable. After the power is turned on, PT2259 must wait at least 200ms before it is able to send an I²C control signal otherwise control efficacy and normal operation will be comprised. Please refer to the diagram below:



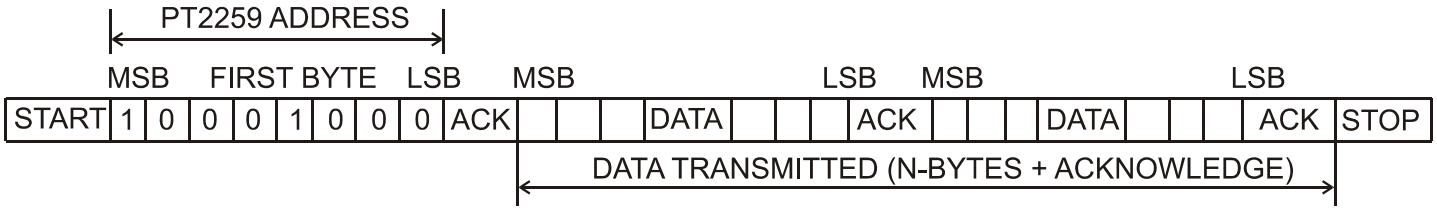
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

INTERFACE PROTOCOL

The interface protocol consists of the following:

1. a start condition
2. the PT2259 address byte followed by an “acknowledge” signal
3. a data sequence (n-bytes and an “acknowledge” signal)
4. a stop condition

Please refer to the following diagram:



Note: ACK=ACKNOWLEDGE
Max Clock Speed = 100K BITS/S

SOFTWARE SPECIFICATIONS

PT2259 address is shown below:

1 MSB	0	0	0	1	0	0	0 LSB

DATA BYTES DESCRIPTION

FUNCTION BITS

MSB							LSB	Function
1	1	0	1	A3	A2	A1	A0	2-channel, -1dB/step
1	1	1	0	0	B2	B1	B0	2-channel, -10db/step
1	0	1	0	A3	A2	A1	A0	Left channel, -1db/step
1	0	1	1	0	B2	B1	B0	Left channel, -10dB/step
0	0	1	0	A3	A2	A1	A0	Right channel, -1dB/step
0	0	1	1	0	B2	B1	B0	Right channel, -10dB/step
1	1	1	1	0	0	0	0	Clear register
0	1	1	1	0	1	C1	C0	Mute select

ATTENUATION UNIT BITS

A3	A2/B2	A1/B1	A0/B0	Attenuation (dB)
0	0	0	0	0/0
0	0	0	1	-1/-10
0	0	1	0	-2/-20
0	0	1	1	-3/-30
0	1	0	0	-4/-40
0	1	0	1	-5/-50
0	1	1	0	-6/-60
0	1	1	1	-7/-70
1	0	0	0	-8/
1	0	0	1	-9/

MUTE FUNCTION BITS

C1	C0	Function
0	0	Mute OFF
0	1	Right channel mute ON
1	0	Left channel mute ON
1	1	Left and right channel mute ON

PT2259 CONTROL SOFTWARE PROCEDURE

PT2259 has a built-in Power-On Reset function which clears the function register to zero after power-on. In order to ensure normal operation under any operating voltage, it is recommended an instruction to clear the register must be transmitted. Please refer to the following diagram:

Start	1	0	0	0	1	0	0	0	ACK	1	1	1	1	0	0	0	0	ACK	Stop

2259 Address Clear Registry

The PT2259 function register does not have any default settings. After clearing the register, an initial value must send in order to each register. If a register does has not been set, it is possible that no sound will be output.

When adjusting the volume of PT2259, it is necessary to send a multiple of 10dB followed by a 1dB code to the attenuator in sequence. If this sequence is not followed, or if only a 10dB or 1dB value is sent, the IC may not operate normally. Please refer to the diagram below:

Example : Request volume setting of –42dB:

Start	1	0	0	0	1	0	0	0	ACK	1	1	1	0	0	1	0	0	ACK	1	1	0	1	0	0	1	0	ACK	Stop

2259 Address -40dB -2dB

Start	1	0	0	0	1	0	0	0	ACK	1	1	0	1	0	0	1	0	ACK	1	1	1	0	0	1	0	0	ACK	Stop

2259Address -2dB -40dB

The two methods above are both acceptable.

WARNING! THE FOLLOWING TRANSMISSION METHODS ARE NOT PERMITTED.

Sending only a 10dB attenuation value:

Start	1	0	0	0	1	0	0	0	ACK	1	1	1	0	0	1	0	0	ACK	Stop

2259 Address -40dB

Sending only a 1dB attenuation value:

Start	1	0	0	0	1	0	0	0	ACK	1	1	0	1	0	0	1	0	ACK	Stop

2259 Address -2dB

Sending a 10dB code with a 1dB code simultaneously or in combination with other control codes:

Start	1	0	0	0	1	0	0	0	ACK	1	1	0	1	0	0	1	0	ACK	0	0	1	0	0	0	1	0	ACK	1	1	1	0	0	1	0	0	ACK	Stop

2259 Address -2dB Right Channel -2dB -40dB

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Supply Voltage	Vcc	12	V
Operating Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-65 ~ +150	°C
Input Voltage	Vi	-0.3 ~ Vcc + 0.3	V

ELECTRICAL CHARACTERISTICS

(Conditions: Vcc=9V, Vi=1Vrms, f=1kHz, Temp=27°C)

Parameter	Symbol	Testing Conditions		Min.	Typ.	Max.	Unit
Operating Voltage	Vcc			4	9	12	V
Operating Current	Icc	Vcc=9V, Vi=0V		-	2.5	3	mA
Volume Attenuation Range	ARANGE	Minimum attenuation		-	0	-	dB
		Maximum attenuation		-	-79	-	
Attenuation Step	ASTEP	-		-	1	-	dB
Attenuation Step Gain Error	GERR	-		-	0.5	-	dB
Interchannel Attenuation Gain Error	CERR	-		-	0.5	-	dB
Maximum Output Voltage	Vomax	Vcc=9V, freq=1kHz, Volume Att.=0dB, Rload=50KΩ, THD<1%		2.0	2.3	2.5	Vrms
Total Harmonic Distortion	THD	f=1kHz, Vol.Att.=0dB, A-weight Rload = 50 KΩ	Vout=2Vrms	-	0.07	0.09	
			Vout= 200mVrms	-	0.003	0.005	%
Noise Output	NO	Vin=GND, Mute=OFF, Volume Att = 0dB, A-weighted		-	2	3	μVrms
Signal-to-Noise Ratio	SNR	Vin=1Vrms, Att.=0dB	No-weighted	95	100	103	
			A-weighted	110	120	125	dB
Channel Separation	CS	Vin=2.5Vrms, freq.=1kHz, Volume Att.=0dB		100	120	125	dB
Mute	MUTE	Vin=2.5Vrms, freq.=1kHz, Vol. Att.=0dB, A-weighted		90	95	97	dB
Frequency Response	FR	Vin=1Vrms, Volume Att.=-10dB		-	1	1.3	MHz
Input Impedance	Rin	f = 1kHz		-	33	-	KΩ
Output Impedance	Rout	f=1kHz, Vout=100mVrms		-	6	-	Ω

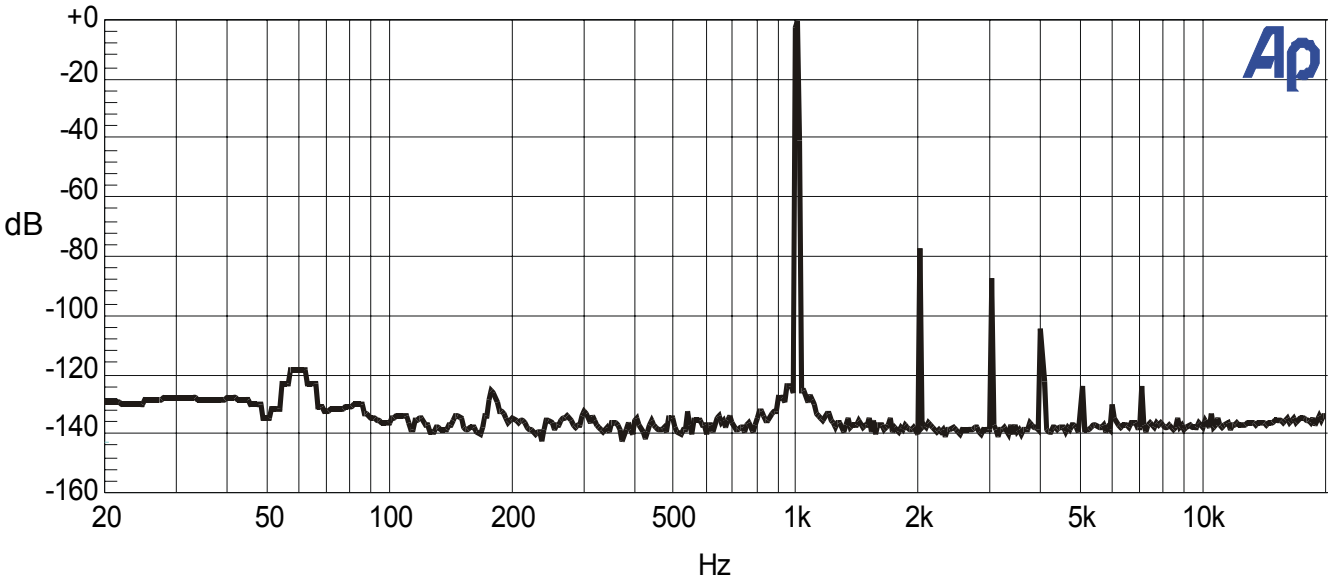
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

I²C BUS SECTION ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VIH	Bus High Input Level	-	3.5	-	-	V
VIL	Bus Low Input Level	-	-	-	0.8	V

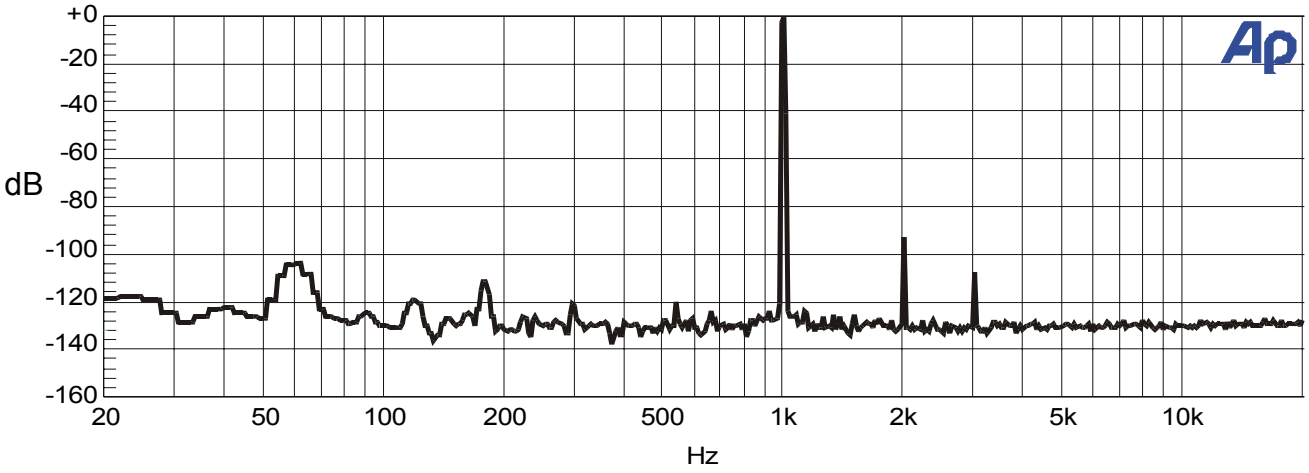
PT2259 THD - FAST FOURIER TRANSFORM (FFT) ANALYSIS 1

(Conditions: Rload = 10K, Volume Att = 0dB, Vcc = 9V, Output Level = 1Vrms)



PT2259 THD - FAST FOURIER TRANSFORM (FFT) ANALYSIS 2

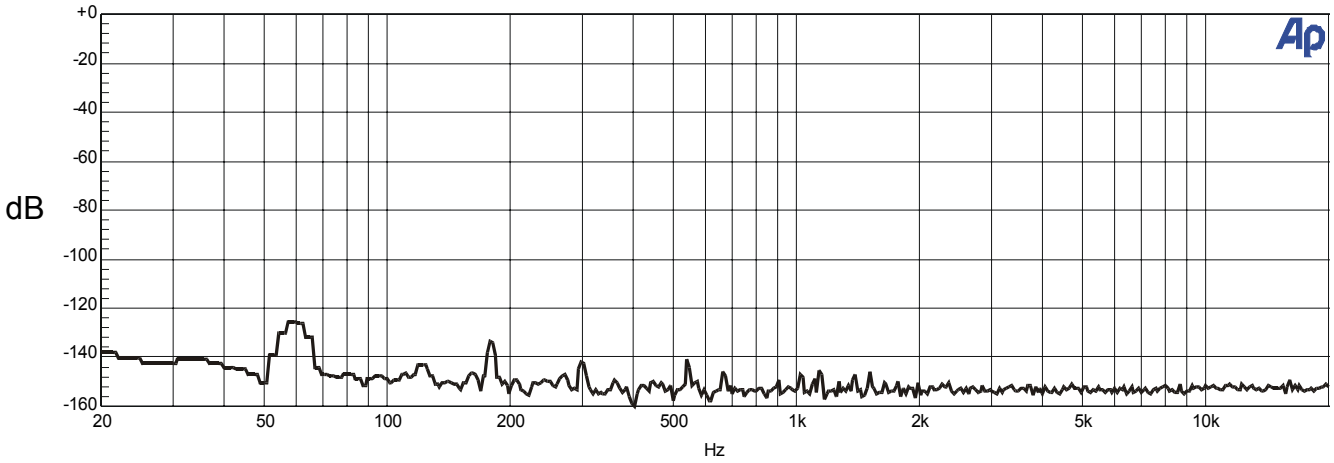
(Conditions: Rload = 10K, Volume Att = 0dB, Vcc = 9V, Output Level = 200m Vrms)



Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

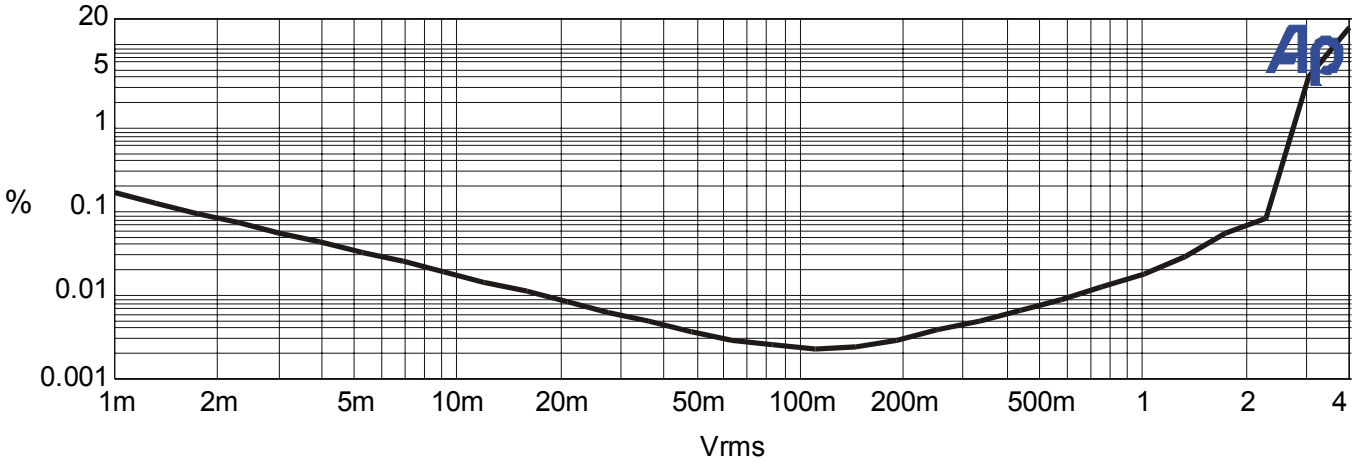
PT2259 NOISE FLOOR - FAST FOURIER TRANSFORM (FFT) ANALYSIS 3

(Conditions: Rload = 10K, Volume Att = 0dB, Vcc = 9V, Vin=GND)



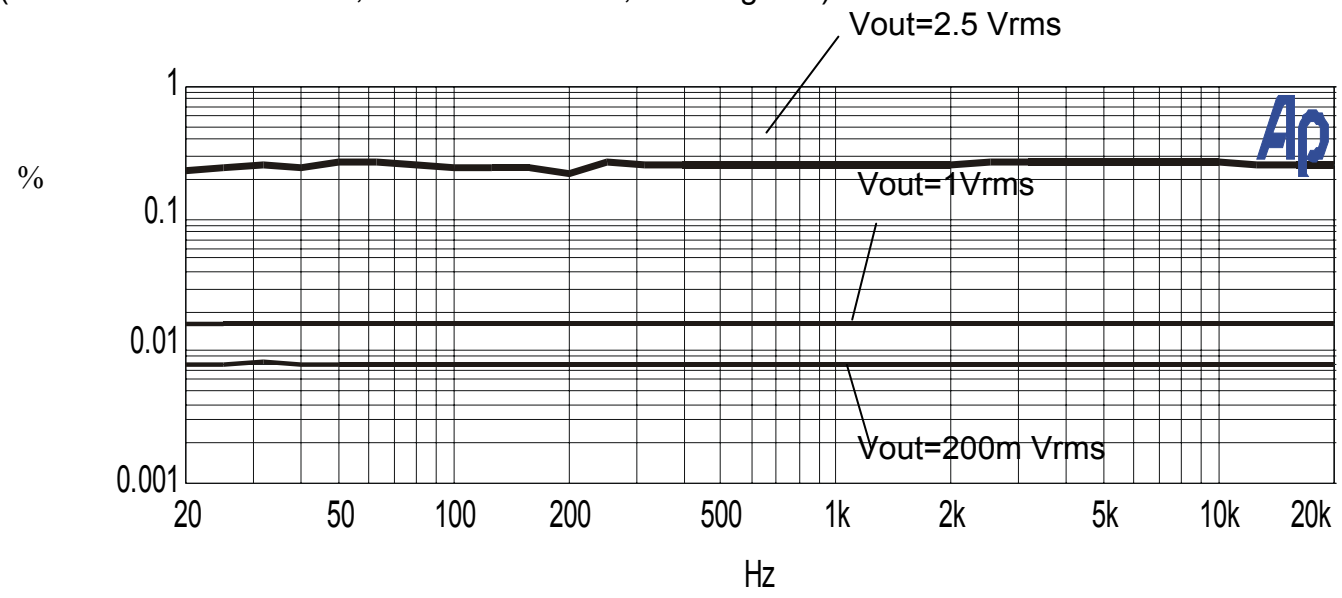
PT2259 THD VS. OUTPUT LEVEL

(Conditions: Rload = 10K, Volume Att = 0dB, Vcc = 9V, f = 1kHz， A-weighted)



PT2259 THD VS. FREQUENCY RESPONSE AT VARIOUS OUTPUT LEVELS

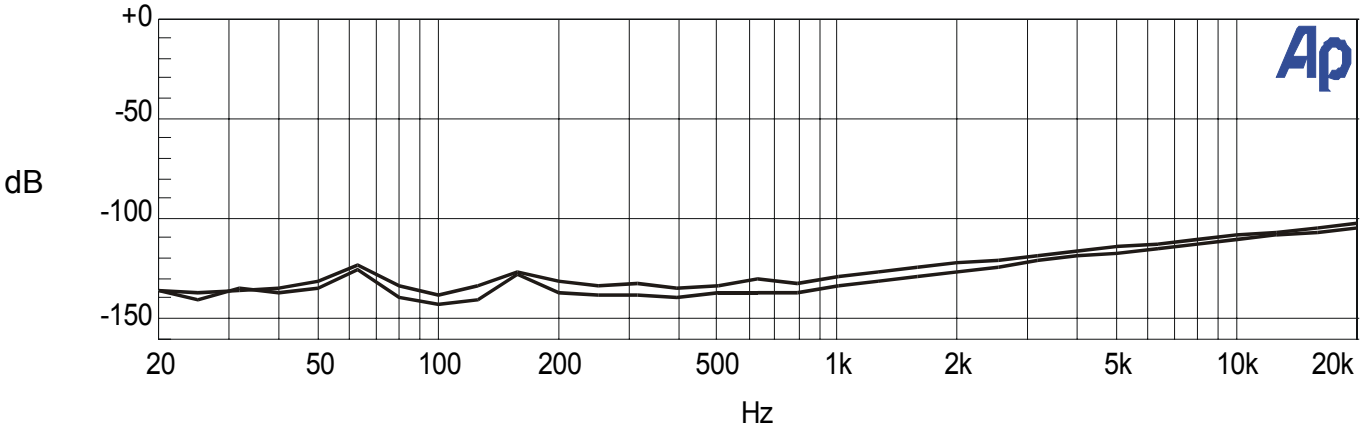
(Conditions: Rload = 10K, Volume Att = 0dB, No-weighted)



Note: from top to bottom: Vout = 2.5Vrms, 1Vrms = 200mVrms

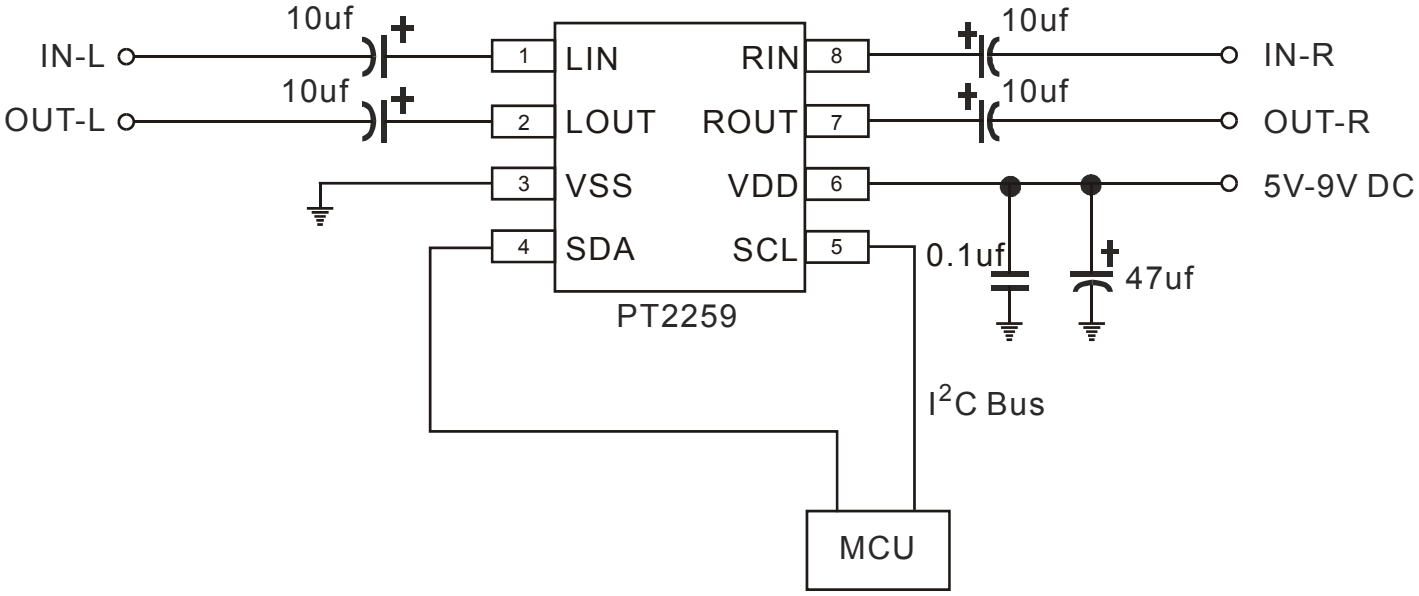
PT2259 INTERCHANNEL CROSSTALK

(Conditions: Rload = 10K, Volume Att = 0dB)



Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

APPLICATION CIRCUIT



Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

ORDERING INFORMATION

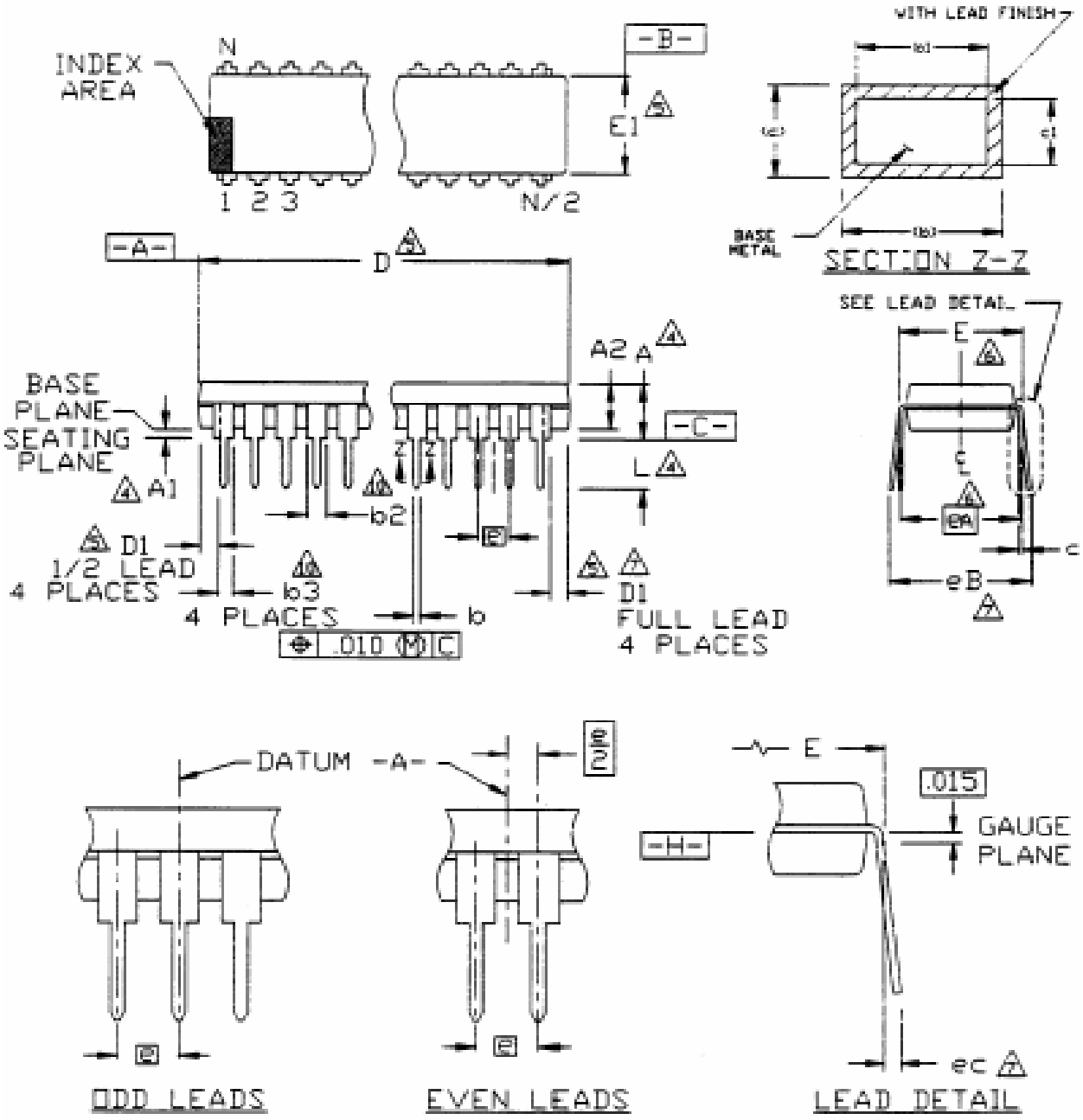
Valid Part Number	Package Type	Top Code
PT2259	8-Pins, DIP, 300mil	PT2259
PT2259-S	8-Pins, SOP, 150mil	PT2259-S
PT2259 (L)	8-Pins, DIP, 300mil	PT2259
PT2259-S (L)	8-Pins, SOP, 150mil	PT2259-S

Notes:
1. (L), (C) or (S) = Lead Free
2. The Lead Free mark is put in front of the date code.

Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

PACKAGING INFORMATION

8-PIN, DIP, 300 MIL



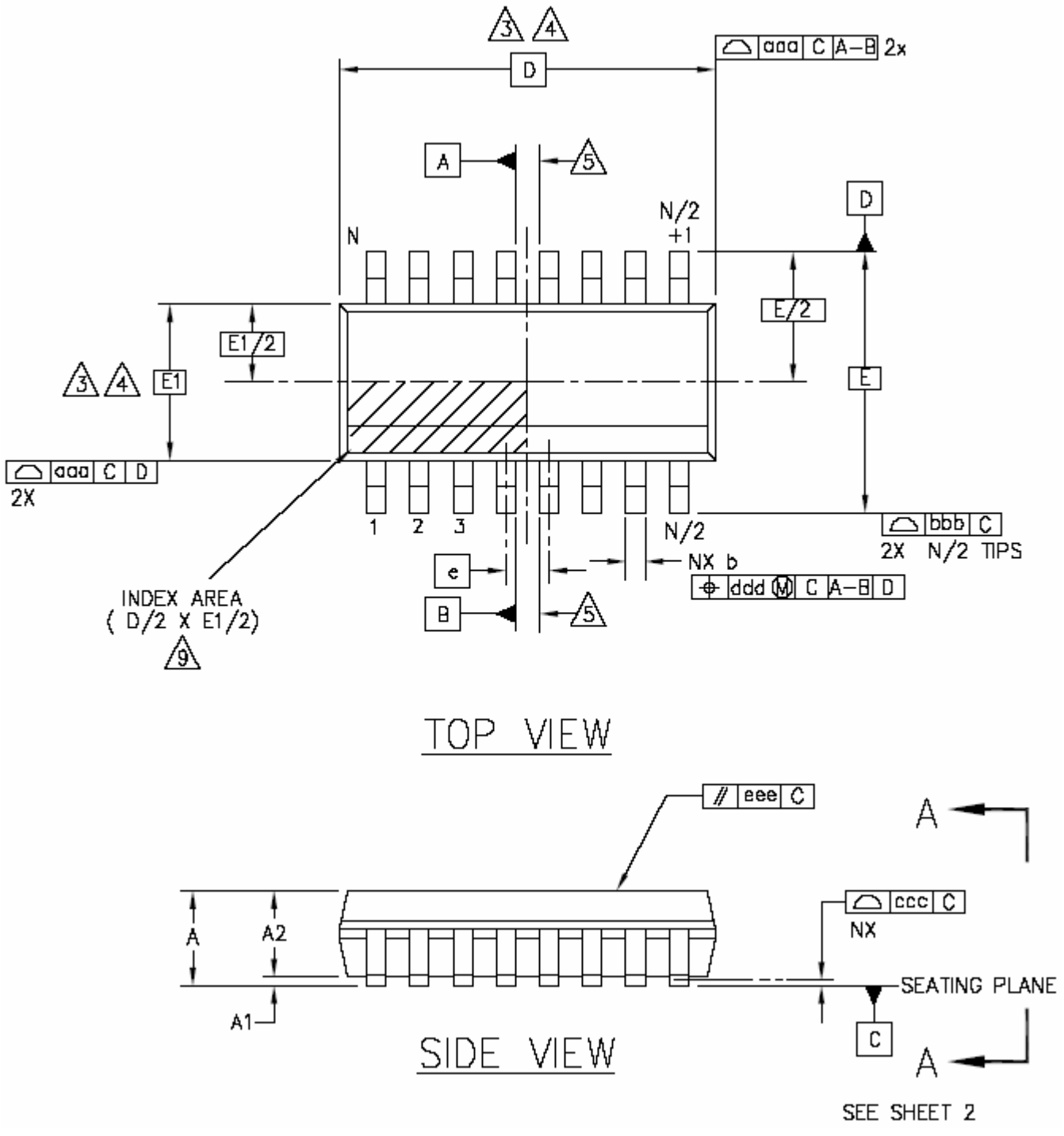
Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.355	0.365	0.400
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 bsc.		
eA	0.300 bsc.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

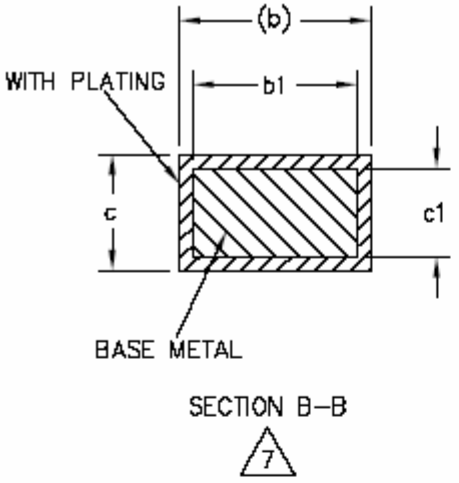
Notes:
1. Controlling Dimensions: INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. E and eA measured with the leads constrained to be perpendicular to data –c- .
5. eB and eC are measured at the lead tips with the leads unconstrained.
6. Pointed or rounded lead tips are preferred to ease insertion.
7. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm)
8. Distance between the leads including dambar protrusions to be 0.005 inch minimum.
9. Refer to JEDEC MS-001, Variation BA.

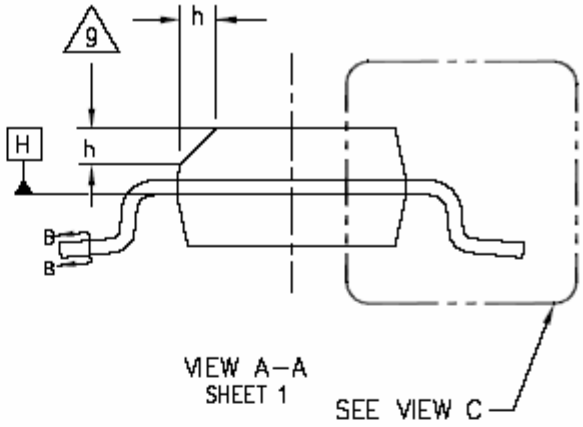
JEDEC is the trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.

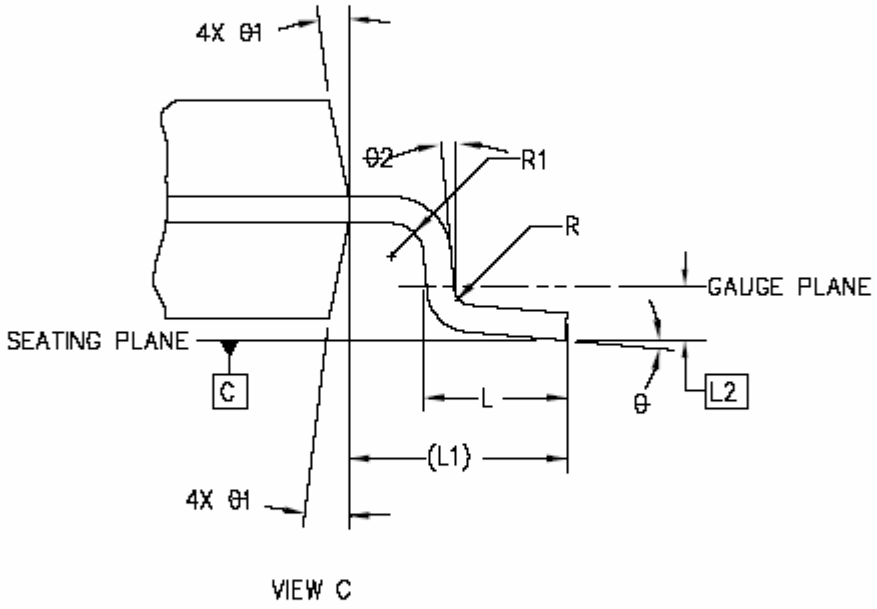
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

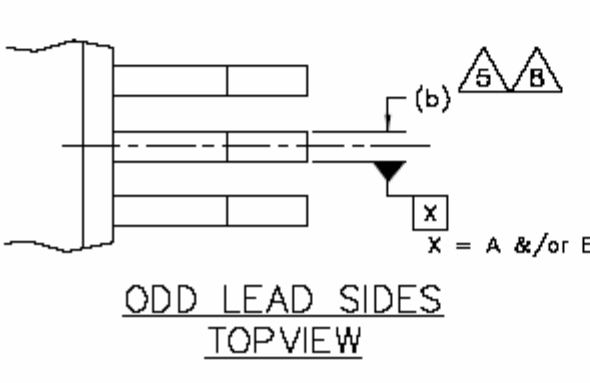
8-PIN, SOP, 150 MIL

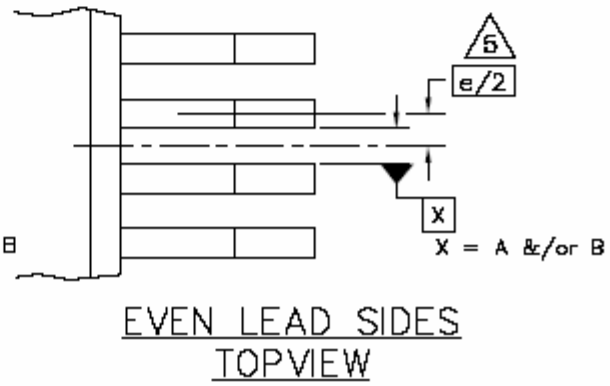



(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7


9
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C


4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C


(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW


5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	4.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Note:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AA.

JEDEC is the registered trademark of JEDEC SOLID STATE TECHNOLOGY ASSOCIATION.