RASCO T.M.

the new generation of data clock oscillators

ALL-METAL, WELDED PACKAGE — offers full hermetic seal to provide excellent resistance to extremes of heat/humidity. With pin 7 case ground, the all-metal package also offers improved shielding to minimize RF radiation, helping to meet FCC EMI specifications. The oscillator can be soldered in standard wave-line operations without damage; insulated stand-offs permit proper de-fluxing. Can also be plugged into a DIP socket. Takes up only .820" x .520" on a circuit board, and its seated height of .270" lets you use standard logic boards with no loss of spacing.

TTL COMPATIBLE — uses standard +5V dc input, drives standard and high speed TTL logic, fan out of 10.

CMOS COMPATIBLE — RASCO-C series oscillators are compatible with high speed CMOS logic, capable of driving such devices as the 74HC series with highly capacitive loads. The low current drain of the RASCO-C oscillators make them well suited for low power CMOS applications. Note: current drain is frequency-dependent; see chart at right.

±0.01% FREQUENCY STABILITY (RASCO-1)—over the range of 0°C to 70°C, suitable for most applications in data communication logic timing. RASCO-0 has ±0.005% stability over the same operating range. This specification is inclusive of calibration tolerance, stability vs. input voltage change, stability vs. load change, aging, and stability vs. shock and vibration.

TIGHT SYMMETRY — For system timing applications requiring controlled duty cycle, the RASCO-S series oscillators offer a worst-case symmetry specification of 45/55%.

RELAXED SPECS, RELAXED PRICES — for applications where frequency stability is not a primary requisite, RASCO-2 (±0.05%), RASCO-3 (±0.1%), and RASCO-4 (±1%) are ideal. They are cost-effective with discrete components and crystals. To the user of multi-vibrator, RC and LC circuits, they offer orders of magnitude better stability and reliability at minimum cost. Economies of scale plus relaxed design and manufacturing tolerances result in cost savings which are passed on to you.

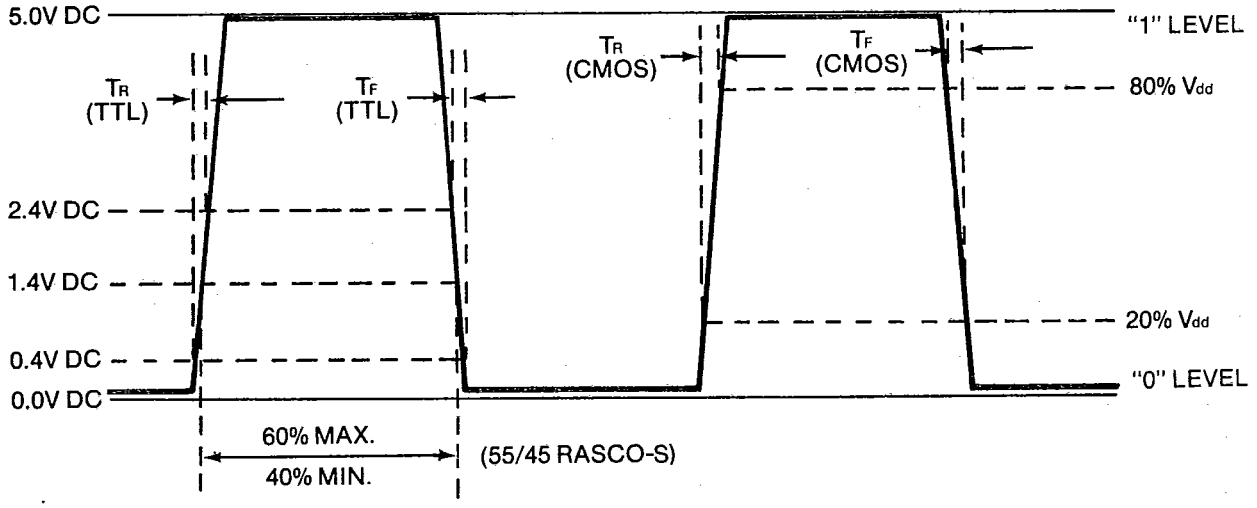
PRECISE RISE AND FALL TIMES — the rise and fall times of the RASCO series oscillators are rigidly controlled so as to be compatible with the stringent requirements of microprocessors. The charts at right show the typical relationships between rise and fall times and load capacitance for 20% to 80% V_{dd} and for .5 to 2.4V dc.

RUGGED, RELIABLE — Advanced circuit design offers drastically reduced component count and minimizes interconnects, improving reliability. Maximum reliability at minimum cost results from Motorola's extensive experience in quartz crystal technology and in thick film hybrid IC processing. Gold plating of crystals and clean-room processing testify that no short-cuts are taken that might diminish reliability.

YOUR TIMING NEEDS IN ONE PACKAGE — The single package oscillator saves you the board space required by discrete components, and eliminates production man-hours wasted analyzing oscillator circuits and matching crystal parameters to circuit components. The packaged oscillator provides first-time, every-time reliability, with no starting resistance problems, spurious modes, or activity dips. And with a packaged oscillator, you eliminate source-hunting and source-qualifying for its components, cut down on direct labor for parts insertion, cut down on overhead costs for Receiving, Incoming Inspection, Purchasing and Accounts Payable.

COMPLETE PROCESS CONTROL — uniform high quality in high volume production is made possible only by complete control of all aspects of the manufacturing process, from growing, sawing, lapping and finishing the quartz, through hybrid thick circuit processing and clean room assembly, with stringent quality control measures enforced at every step.

100% COMPUTER-AUTOMATED TESTING of *all* critical functional parameters, under maximum load conditions: rise and fall times, "0" and "1" levels, symmetry, frequency tolerance, and current drain.



CRYSTAL CLOCK OSCILLATOR WAVE SHAPE

MODEL IDENTIFICATION

RASCO 2 C S E

1. Stability
2. CMOS/TTL
3. Symmetry
4. Enable/Disable

1. Stability — the number in this position signifies the frequency stability specification of the particular model per the following chart:

MODEL	STABILITY
RASCO 0	±0.005%
RASCO 1	±0.01%
RASCO 2	±0.05%
RASCO 3	±0.1%
RASCO 4	±1.0%

2. CMOS/TTL — models with TTL compatibility have no designator here, while CMOS compatible models are designated by the letter "C." Thus, a RASCO 3C is a CMOS-compatible model with ±0.1% stability, and a RASCO 1 is TTL compatible with stability of ±0.01%.

3. Symmetry — tight symmetry (45/55%) models are indicated by an "S" suffix. Models with no "S" suffix have the standard 40/60% (worst case) symmetry specification.

4. Enable/Disable — the enable/disable feature is indicated by an "E" suffix.

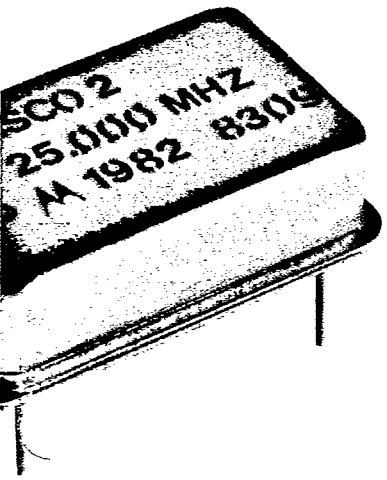
It is possible for a model to require all 3 letter designators; for example, a ±0.01% CMOS-compatible model with tight symmetry and enable/disable would become model RASCO 1CSE.

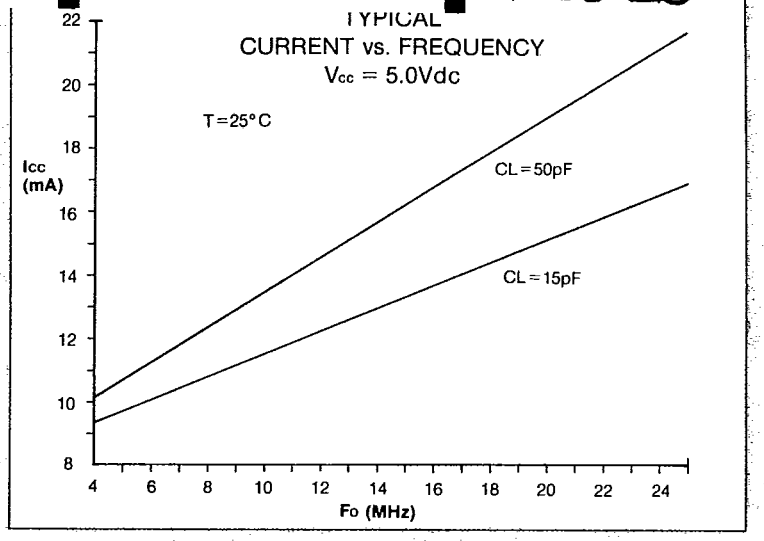
ENABLE/DISABLE APPLICATION

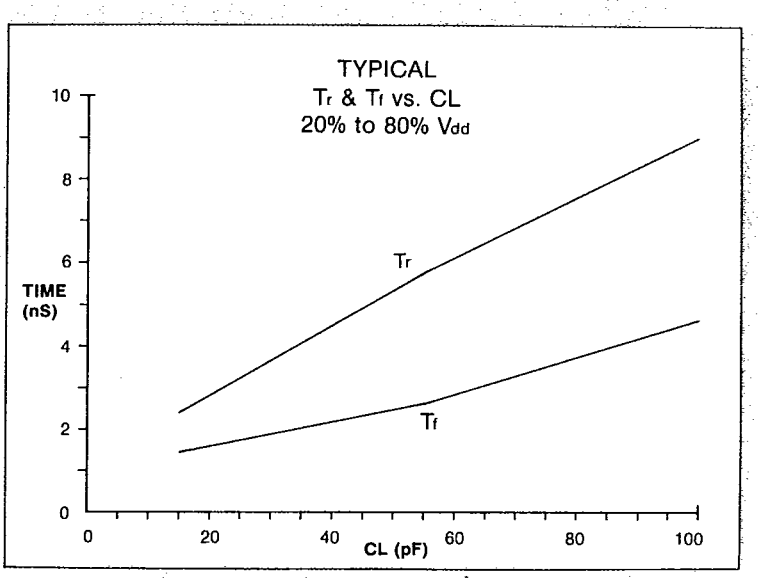
The enable input is CMOS compatible only. At Vdd of 4.5V dc, temperature range 0°C to 70°C, 4 MHz to 25 MHz:

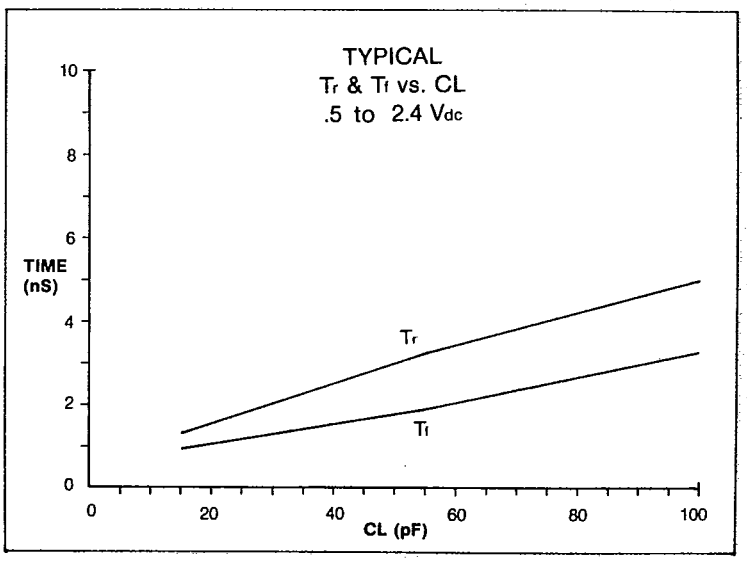
V_{IH} ("1" level input voltage) = 3.2V dc minimum
I_{IL} ("1" level input current) = 10 μA max @ V_{IH}
V_{IH} ("0" level input voltage) = 0.8V maximum
I_{IL} ("0" level input current) = 20 μA max @ V_{IL}

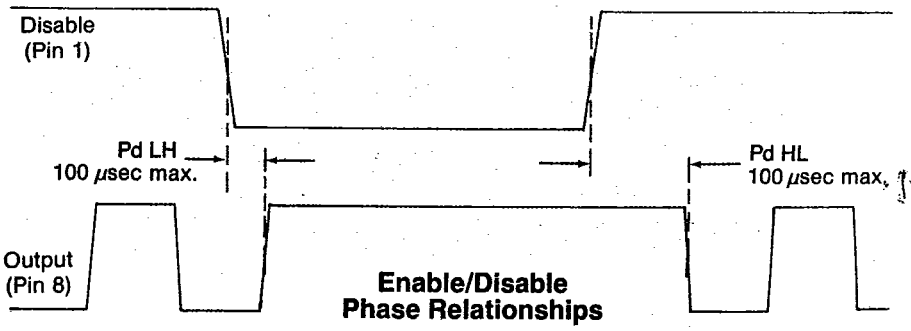
When enable input is low ("0") the output is disabled to logic "1" level and cannot be wire "OR"ed.











Enable/Disable Phase Relationships

Specifications

■ **FREQUENCY RANGE:**
1 MHz–25 MHz

■ **FREQUENCY STABILITY:**
RASCO-0, ±0.005%; RASCO-1, ±0.01%; RASCO-2, ±0.05%; RASCO-3, ±0.1%; RASCO-4, ±1.0% (Inclusive of calibration tolerance at 25°C, operating temperature range, input voltage change, load change, aging, shock, and vibration).

■ **TEMPERATURE RANGE:**
OPERATING: 0°C to 70°C
STORAGE: −55°C to 125°C

■ **INPUT VOLTAGE:**
+5V DC ±10%

■ **VOLTAGE STABILITY (±10%):**
<±3 PPM Typical

■ **INPUT CURRENT:** (See graph on inside page)
35 mA over temperature @ f = 25 MHz, C_L = 15 pF
For loads >15 pF, add .15 mA/pF @ 25 MHz
CURRENT, OUTPUT SHORTED: (1 sec. max.) −30 mA Min. −140 mA Max.

■ **OUTPUT (0°C to 70°C):**
SYMMETRY: 45/55% typ. @ 1.4V DC
40/60% (min/max)

RISE & FALL TIMES (Max) tr tf
20% V_{dd} to 80% V_{dd}: 8 ns 7ns C_L = 15 pF
.4V to 2.4V: 6 ns 6 ns C_L = 15 pF
(See graphs, inside page)

"0" LEVEL: (V_{OL}) +.4V max I_{OL} = 16 mA
16 mV/mA
TC = ±1.2 mV/C° @ I_{OL} = 16 mA

"1" LEVEL: (V_{OH}) V_{dd} −.2V min I_{OH} = −1 mA

HIGH OR LOW LEVEL OUTPUT CURRENT: ±25 mA Absolute Max. Value

V_{dd} OR GROUND CURRENT: ±50 mA Max.

OUTPUT VOLTAGE: −.5 to V_{dd} +.5

■ **START UP TIME**
(TYPICAL): ≤5 ms

■ **OUTPUT LOAD:**
10 TTL Gates
CMOS Compatible

■ **ENABLE/DISABLE:**
(Available 4–25 MHz)
Pd LH 100 μsec max.
Pd HL 100 μsec max.

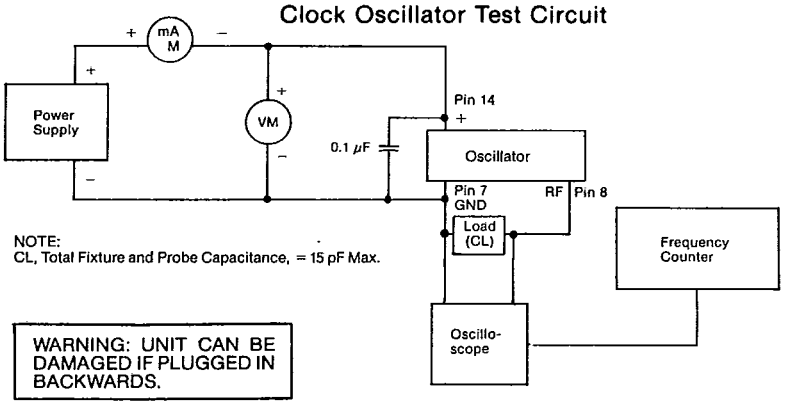
■ **LOAD STABILITY:**
<±2 PPM Typical R_L = 390Ω C_L = 50 pF

■ **ENVIRONMENTAL:**
TEMPERATURE CYCLE: MIL.-883B Method 1010.2 Level B
SHOCK: 1000 G's 0.35 millisec, 1/2 sine wave; 3 shocks each plane
VIBRATION: 10–55 Hz, .060" D.A., 55 Hz–2000 Hz 35 G's. Duration time—12 hours
HUMIDITY: 85% Relative humidity, @ +85° C, 500 hrs.

■ **MECHANICAL:**
GROSS LEAK TEST: Leak test in de-ionized H_2O.
HERMETICALLY SEALED PACKAGE: Mass spectrometer leak rate less than 2×10^{-8} atmos. cc/sec. of helium
SEAL STRENGTH: 20 lbs. max. force perpendicular to top and bottom
BEND TEST: Pins will withstand maximum bend of 90° reference to base for 2 bends.
MARKING INK: Epoxy, heat cured
SOLVENT RESISTANCE: Freon TMC
No marking or seal destruction
Dipped in solvent 1 minute @ +25°C ±5°C

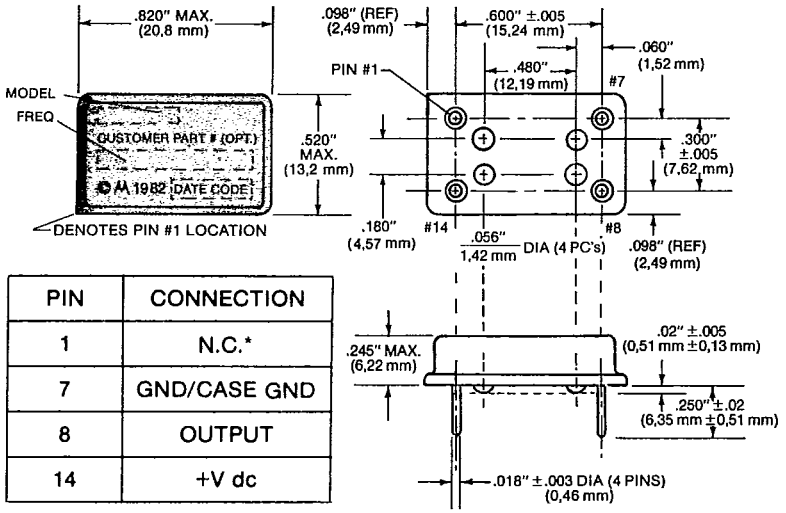
Note: (1) Unit can be cleaned by only one type solvent listed.
Note: (2) Ultrasonic degreaser not to be used.

Clock Oscillator Test Circuit



NOTE:
CL, Total Fixture and Probe Capacitance, = 15 pF Max.

WARNING: UNIT CAN BE DAMAGED IF PLUGGED IN BACKWARDS.



PIN	CONNECTION
1	N.C.*
7	GND/CASE GND
8	OUTPUT
14	+V dc

*Used for enable/disable function in "E" version only.

Solderability Specifications

■ **MATERIALS:**
SOLDER: 60% tin and 40% lead
FLUX: Mildly activated rosin base type such as Alpha 611.

■ **PROCEDURE:**
PREPARATION: No wiping, cleaning, scraping, or abrading shall be performed on the leads.
SOLDER BATH: The solder bath shall be maintained at 265 ±5°C.
SOLDERABILITY: Dip the terminals into room temperature flux, to a maximum of .020" from the unit base, for 5 to 10 seconds. Withdraw from the flux and dip the terminals to the same depth in the molten solder from 5 to 7 seconds. Flux residue may be removed with Freon rinse, or with soft swab moistened with isopropyl alcohol or Freon.

■ **REQUIREMENTS:**
EVALUATION: All leads must exhibit a minimum of 90% continuous solder coating over their entire length beyond .020" from the unit base. Pinholes or voids may not be concentrated in any one area and are not to exceed 10% of the total area under examination.

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