Proposed

RF3106

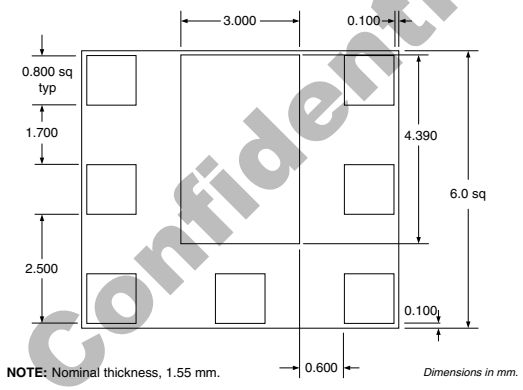
3V 1900MHZ LINEAR AMPLIFIER MODULE

Typical Applications

- 3V CDMA US-PCS Handsets
- Spread-Spectrum Systems

Product Description

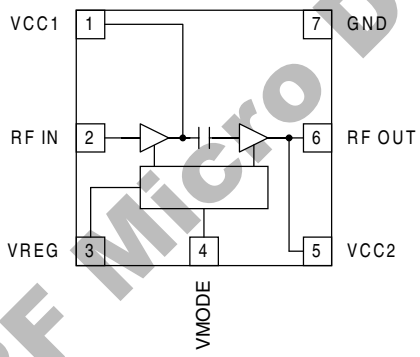
The RF3106 is a high-power, high-efficiency linear amplifier IC targeting 3V handheld systems. The device is manufactured on an advanced Gallium Arsenide Heterojunction Bipolar Transistor (HBT) process, and has been designed for use as the final RF amplifier in dual-mode 3V CDMA hand-held digital cellular equipment, spread-spectrum systems, and other applications in the 1850MHz to 1910MHz band. The RF3106 has a digital bias control voltage for low current in standby mode. The device is self-contained with 50Ω input and output that is matched to obtain optimum power, efficiency, and linearity characteristics. The module is an ultra-small 6mmx6mm land grid array with backside ground.



Optimum Technology Matching® Applied

- ☐ Si BJT
- ☑ GaAs HBT
- ☐ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS

Package Style: LGM (6mmx6mm)



Functional Block Diagram

Features

- Input/Output Internally Matched @ 50Ω
- Single 3V Supply
- 29dBm Linear Output Power
- 25dB Linear Gain
- 32% Linear Efficiency

Ordering Information

RF3106	3V 1900MHz Linear Amplifier Module
RF3106 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
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Tel (336) 664 1233
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http://www.rfmd.com

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (RF off)	+8.0	V_{DC}
Supply Voltage (P_{OUT}≤29dBm)	+4.5	V_{DC}
Control Voltage (V_{REG})	+4.2	V_{DC}
Mode Voltage (V_{MODE})	+3.5	V_{DC}
Input RF Power	+10	dBm
Operating Ambient Temperature	-30 to +85	°C
Storage Temperature	-30 to +150	°C

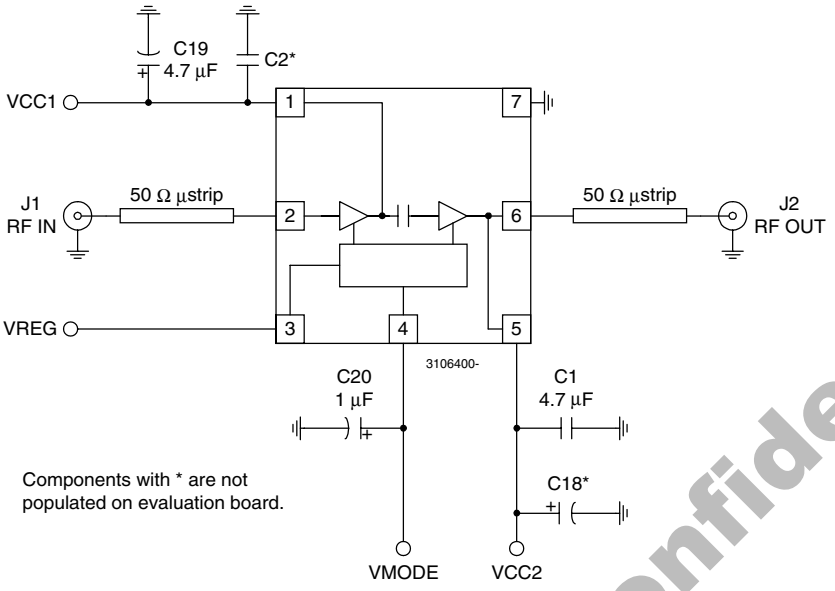
Caution! ESD sensitive device.

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Overall					T=25°C, V_{CC}=3.4V, V_{REG}=2.8V, V_{MODE}=2.8V, Freq=1850MHz to 1910MHz unless otherwise specified
Frequency Range	1850		1910	MHz	
Linear Gain	22	26		dB	
Second Harmonic			-35	dBc	
Third Harmonic			-40	dBc	
Maximum Linear Output Power (CDMA Modulation)	29			dBm	
Total Linear Efficiency	30	32		%	
Adjacent Channel Power Rejection			-44	dBc	ACPR @ 1250kHz
Input VSWR		<2:1			
Output VSWR			10:1		No damage.
			6:1		No oscillations.
Noise Power			-95	dBm/30kHz	At 80MHz offset.
Power Supply					
Power Supply Voltage	3.2	3.4	4.5	V	
Quiescent Current		100		mA	
V_{REG} Current			6	mA	Pin 3, V_{REG}=2.8V
Turn On/Off time			<100	ns	
Total Current (Power down)			10	µA	V_{REG}=low
V_{REG} "Low" Voltage		0	0.2	V	
V_{REG} "High" Voltage	2.7	2.8	2.9	V	

Pin	Function	Description	Interface Schematic
1	VCC1	Interstage tuning and collector supply.	
2	RF IN	RF input. An external DC blocking capacitor is required if this port is connected to a DC path to ground or a DC voltage.	
3	VREG	Regulated voltage supply for amplifier bias.	
4	VMODE	For nominal operation, V_{MODE} is set to HIGH. When set LOW: V_{MODE} will increase the bias current by approximately 50%; and, large signal gain is increased by approximately 1.5dB.	
5	VCC2	Output stage collector supply.	
6	RF OUT	RF output internally matched to 50Ω.	
7	GND	Ground connection. Connect to package base ground.	
Pkg Base	GND	Ground connection. The backside of the package should be soldered to a top side ground pad which is connected to the ground plane with multiple vias. The pad should have a short thermal path to the ground plane.	

Evaluation Board Schematic

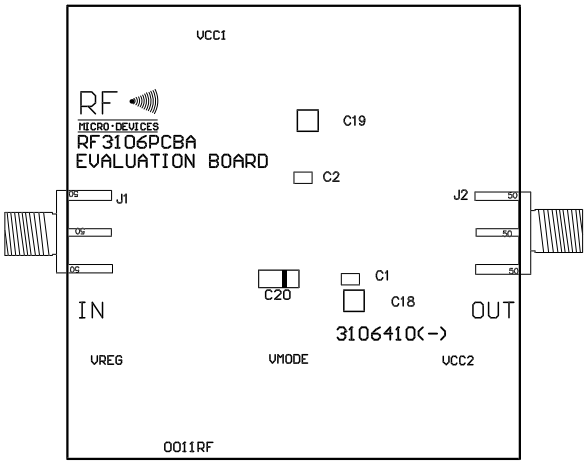
(Download Bill of Materials from www.rfmd.com.)



Evaluation Board Layout
Board Size 2.0” x 2.0”

Board Thickness 0.028”, Board Material FR-4, Multi-Layer

Assembly



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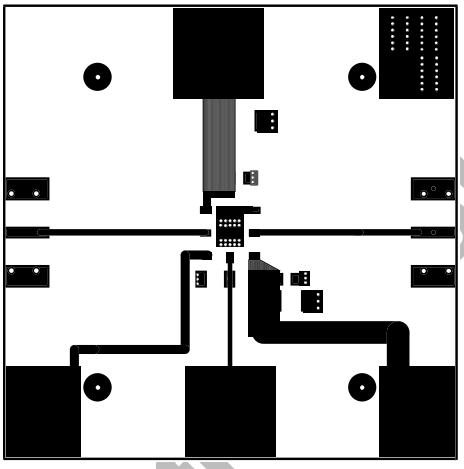
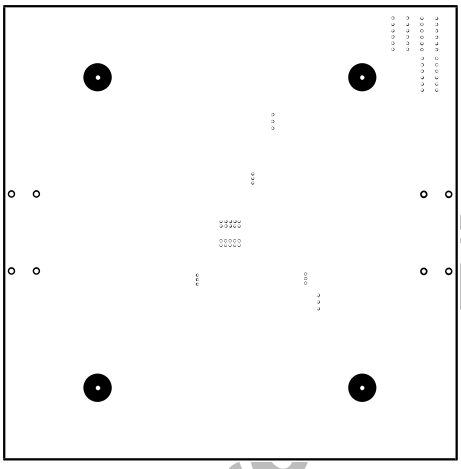


Inner 1



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