SCN2672
Programmable Video Timing Controller (PVTC)

Product Specification

Microprocessor Products

2

DESCRIPTION

The Signetics SCN2672 Programmable Video Timing Controller (PVTC) is a programmable device designed for use in CRT terminals and display systems that employ raster scan techniques. The PVTC generates the vertical and horizontal timing signals necessary for the display of interlaced or non-interlaced data on a CRT monitor. It provides consecutive addressing to a user-specified display buffer memory domain and controls the CPU-display buffer interface for various buffer configuration modes. A variety of operating modes, display formats, and timing profiles can be implemented by programming the control registers in the PVTC.

A minimum CRT terminal system configuration consists of a PVTC, an SCN2671 Keyboard and Communication Controller (PKCC), an SCN2670 Display Character and Graphics Generator (DCGG), an SCB2673/2677 Video and Attributes Controller (VAC), a single-chip microcomputer such as the 8048, a display buffer RAM, and a small amount of TTL for miscellaneous address decoding, interface, and control. Typically, the package count for a minimum system is between 15 and 20 devices; system complexity can be enhanced by upgrading the microprocessor and expanding via the system address and data buses.

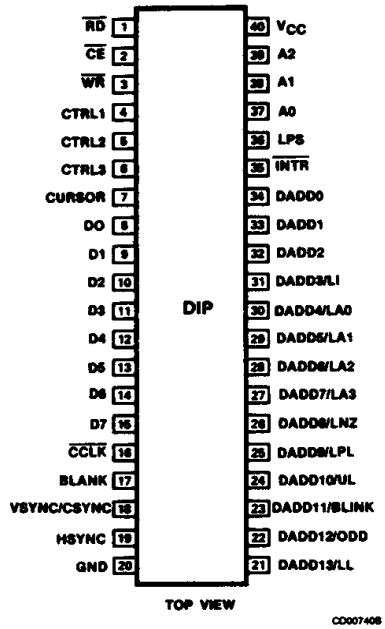
FEATURES

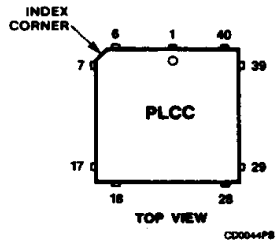
- **4MHz and 2.7MHz character rate versions**
- **Up to 256 characters per row**
- **1 to 16 raster lines per character row**
- **Up to 128 character rows per frame**
- **Programmable horizontal and vertical sync generators**
- **Interlaced or non-interlaced operation**
- **Up to 16k RAM addressing for multiple page operation**
- **Automatic wraparound of RAM**
- **Addressable incrementable and readable cursor**
- **Programmable cursor size, position, and blink**
- **Split screen and horizontal scroll capability**
- **Light pen register**
- **Selectable buffer interface modes**
- **Dynamic RAM refresh**
- **Completely TTL compatible**
- **Single +5V power supply**
- **Power-on reset circuit**

APPLICATIONS

- **CRT terminals**
- **Word processing systems**
- **Small business computers**
- **Home computers**

PIN CONFIGURATIONS





Pin	Function	Pin	Function
1	NC	23	NC
2	$\overline{RD}$	24	DADD13/LL
3	$\overline{CE}$	25	DADD12/ODD
4	$\overline{WR}$	26	DADD11/BLINK
5	CTRL1	27	DADD10/UL
6	CTRL2	28	DADD9/LPL
7	CTRL3	29	DADD8/LNZ
8	CURSOR	30	DADD7/LA3
9	D0	31	DADD6/LA2
10	D1	32	DADD5/LA1
11	D2	33	DADD4/LA0
12	NC	34	NC
13	D3	35	DADD3/LI
14	D4	36	DADD2
15	D5	37	DADD1
16	D6	38	DADD0
17	D7	39	$\overline{INTR}$
18	$\overline{CCLK}$	40	LPS
19	BLANK	41	A0
20	VSYNC/CSYNC	42	A1
21	HSYNC	43	A2
22	GND	44	V_{CC}

ORDERING INFORMATION

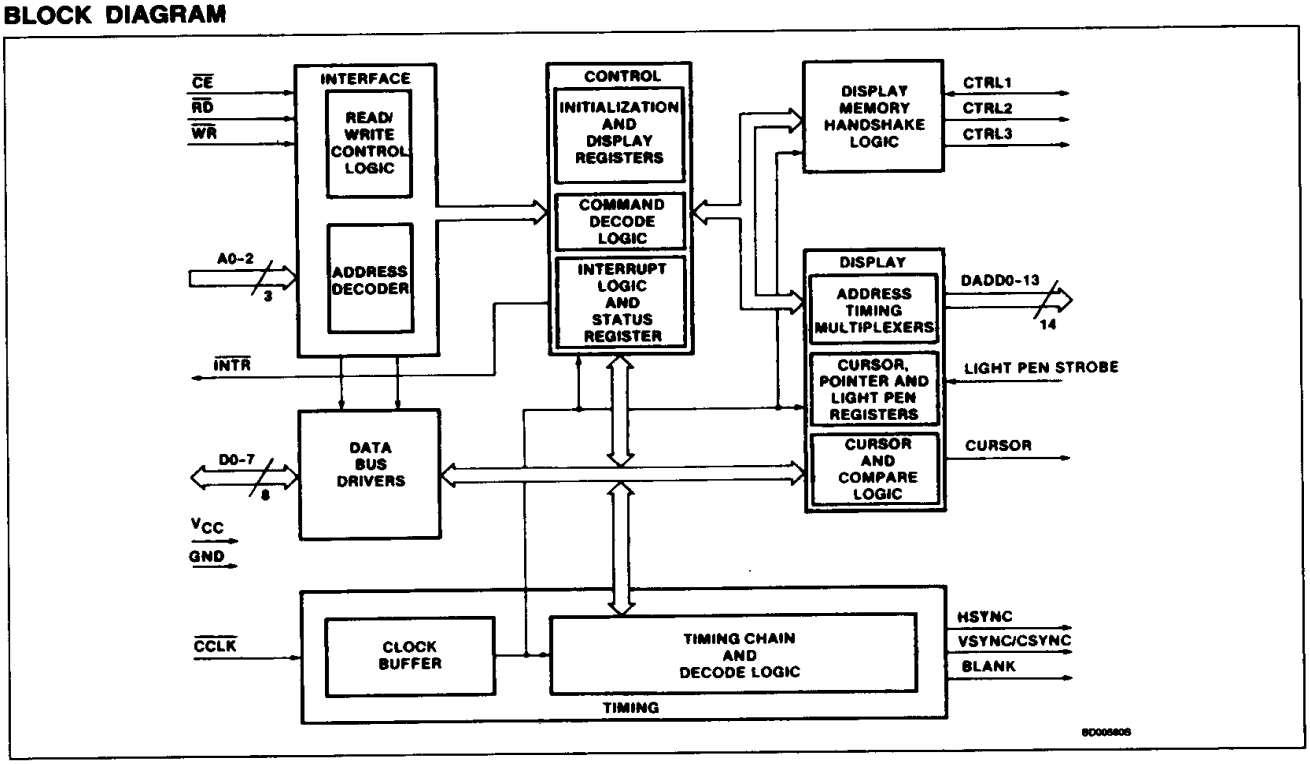
PACKAGES	V_{CC} = +5V ±5%, T_A = 0°C to +70°C	
	4MHz	2.7MHz
Ceramic DIP	SCN2672BC4I40	SCN2672BC3I40
Plastic DIP	SCN2672BC4N40	SCN2672BC3N40
Plastic LCC	SCN2672BC4A44	SCN2672BC3A44

FUNCTIONAL DESCRIPTION

As shown on the block diagram, the PVTC contains the following major blocks:

- Data bus buffer
- Interface Logic
- Operation Control
- Timing
- Display Control
- Buffer Control

BLOCK DIAGRAM



Data Bus Driver

The data bus buffer provides the interface between the external and internal data busses. It is controlled by the operation control block to allow read and write operations to take place between the controlling CPU and the PVTC.

Interface Logic

The interface logic contains address decoding and read and write circuits to permit communications with the microprocessor via the data bus buffer. The functions performed by the CPU read and write operations are as shown in Table 1.

Table 1. PVTC Addressing

A2	A1	A0	READ ($\overline{RD}$ = 0)	WRITE ($\overline{WR}$ = 0)
0	0	0	Interrupt register	Initialization registers[1]
0	0	1	Status register	Command register
0	1	0	Screen start address lower register	Screen start address lower reg.
0	1	1	Screen start address upper register	Screen start address upper reg.
1	0	0	Cursor address lower register	Cursor address lower register
1	0	1	Cursor address upper register	Cursor address upper register
1	1	0	Light pen address lower register	Display pointer address lower reg.
1	1	1	Light pen address upper register	Display pointer address upper reg.

NOTE:

1. There are 11 initialization registers which are accessed sequentially via a single address. The PVTC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR10, the split screen register) is accessed. The pointer then continues to point to the split screen register. Upon power-up or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command.

PIN DESCRIPTION

MNEMONIC	PIN NO.		TYPE	NAME AND FUNCTION
	DIP	PLCC		
A0 – A2	37 – 39	41 – 43	I	**Address Lines:** Used to select PVTC internal registers for read/write operations and for commands.
D0 – D7	8 – 15	9 – 11, 13 – 17	I/O	**8-Bit Bidirectional 3-State Data Bus:** Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the PVTC take place over this bus. The direction of the transfer is controlled by the $\overline{RD}$ and $\overline{WR}$ inputs when the $\overline{CE}$ input is low. When the $\overline{CE}$ input is high, the data bus is in the 3-State condition.
$\overline{RD}$	1	2	I	**Read Strobe:** Active low input. A low on this pin while $\overline{CE}$ is low causes the contents of the register selected by A0 – A2 to be placed on the data bus. The read cycle begins on the leading (falling) edge of $\overline{RD}$.
$\overline{WR}$	3	4	I	**Write Strobe:** Active low input. A low on this pin while $\overline{CE}$ is also low causes the contents of the data bus to be transferred to the register selected by A0 – A2. The transfer occurs on the trailing (rising) edge of $\overline{WR}$.
$\overline{CE}$	2	3	I	**Chip Enable:** Active low input. When low, data transfers between the CPU and the PVTC are enabled on D0 – D7 as controlled by the $\overline{WR}$, $\overline{RD}$, and A0 – A2 inputs. When $\overline{CE}$ is high, the PVTC is effectively isolated from the data bus and D0 – D7 are placed in the 3-State condition.
$\overline{CCLK}$	16	18	I	**Character Clock:** Timing signal derived from the video dot clock which is used to synchronize the PVTC's timing functions.
HSYNC	19	21	O	**Horizontal Sync:** Active high output which provides video horizontal sync pulses. The timing parameters are programmable.
VSYNC/CSYNC	18	20	O	**Vertical Sync/Composite Sync:** A control bit selects either vertical or composite sync pulses on this active high output. When CSYNC is selected, equalization pulses are included. The timing parameters are programmable.
BLANK	17	19	O	**Blank:** This active high output defines the horizontal and vertical borders of the display. Display control signals which are output on DADD3 through DADD13 are valid on the trailing edge of BLANK.
CURSOR	7	8	O	**Cursor Gate:** This active high output becomes active for a specified number of scan lines when the address contained in the cursor registers match the address output on DADD0 through DADD13. The first and last lines of the cursor and a blink option are programmable.
$\overline{INTR}$	35	39	O	**Interrupt Request:** Open drain output which supplies an active low interrupt request from any of five maskable sources. This pin is inactive after power-on reset or a master reset command.
LPS	36	40	I	**Light Pen Strobe:** Positive edge-triggered input indicating a light pen hit. Causes the current value of the display address to be strobed into the light pen register.
CTRL1	4	5	I/O	**Handshake Control 1:** In independent mode, provides an active low write data buffer ($\overline{WDB}$) output which strobes data from the interface latch into the display memory. In transparent and shared modes, this is an active low processor bus request ($\overline{PBREQ}$) input which indicates that the CPU desires to access the display memory. This pin must be tied high when operating in row buffer mode.
CTRL2	5	6	O	**Handshake Control 2:** In independent mode, provides an active low read data buffer ($\overline{RDB}$) output which strobes data from the display memory into the interface latch. In transparent and shared modes, this is an active low bus external enable ($\overline{BEXT}$) output which indicates that the PVTC has relinquished control of the display memory (DADD0 – DADD13 are in the 3-State condition) in response to a CPU bus request. $\overline{BEXT}$ also goes low in response to a 'display off and float DADD' command. In row buffer mode, it is an active low bus request ($\overline{BREQ}$) output which halts the CPU during a line DMA.
CTRL3	6	7	O	**Handshake Control 3:** In independent mode, provides the active low buffer chip enable ($\overline{BCE}$) signal to the display memory. In transparent and shared modes provides an active low bus acknowledge ($\overline{BACK}$) output which serves as a ready signal to the CPU in response to a processor bus request. In row buffer mode, this is an active high memory bus control

PIN DESCRIPTION (Continued)

MNEMONIC	PIN NO. DIP	PIN NO. PLCC	TYPE	NAME AND FUNCTION
DADD0 – DADD13	34 – 21	38 – 35 33 – 24	O	(MBC) output which configures the system for the DMA transfer of one row of character codes from system memory to the row display buffer. **Display Address:** Used by the PVTC to address up to 16k of display memory. These outputs are floated at various times depending on the buffer mode. Various control signals are multiplexed on DADD3 thru DADD13 and are valid at the trailing edge of BLANK. These control signals are: **DADD3/LI** **Line Interlace:** Replaces DADD4/LA0 as the least significant line address for the interlaced sync and video applications. A low indicates an even row of an even field or an odd row of an odd field. **DADD4 – DADD7/LA0 – LA3** **Line Address:** Provides the number of the current scan line within each character row. **DADD8/LNZ** **Line Zero:** Asserted before the first scan line in each character row. **DADD9/LPL** **Light Pen Line:** Asserted before the scan line which matches the programmed light pen line position (line 3, 5, 7, or 9). **DADD10/UL** **Underline:** Asserted before the scan line which matches the programmed underline position (lines 0 thru 15). **DADD11/BLINK** **Blink frequency:** Provides an output divided down from the vertical sync rate. **DADD12/ODD** **Odd Field:** Active high signal which is asserted before each scan line of the odd field when interlace is specified. **DADD13/LL** **Last Line:** Asserted before the last scan line of each character row.
V_{CC}	40	44	I	**Power Supply:** +5V ±5% power input.
GND	20	22	I	**Ground:** Signal and power ground input.

Operation Control

The operation control section decodes configuration and operation commands from the CPU and generates appropriate signals to other internal sections to control the overall device operation. It contains the timing and display registers which configure the display format and operating mode, the interrupt logic, and the status register which provides operational feedback to the CPU.

Timing

The timing section contains the counters and decoding logic necessary to generate the monitor timing outputs and to control the display format. These timing parameters are selected by programming of the initialization registers.

Display Control

The display control section generates linear addressing for up to 16k bytes of display memory. Internal comparators limit the portion of the memory which is displayed to programmed values. Additional functions performed in this section include cursor positioning, storage of light pen 'hit' location, and address comparisons required for generation of timing signals and the split screen interrupt.

Buffer Control

The buffer control section generates three signals which control the transfer of data between the CPU and the display buffer memory. Four system configurations requiring four different 'handshaking' schemes are supported. These are described below.

SYSTEM CONFIGURATIONS

Figure 1 illustrates the block diagram of a typical display terminal using the Signetics 2670, 2671, 2672, and 2673/2677 CRT terminal devices. In this system, the CPU examines inputs from the data communications line and the keyboard and places the data to be displayed in the display buffer memory. This buffer is typically a RAM which holds the data for a single or multiple screenload (page) or for a single character row.

The PVTC supports four common system configurations of display buffer memory: the independent, transparent, shared, and row buffer modes. The first three modes utilize a single or multiple page RAM and differ primarily in the means used to transfer display data between the RAM and the CPU. The row buffer mode makes use of a single row buffer (which can be a shift register or a small RAM) that is updated in real-time to contain the appropriate display data.

The user programs bits 0 and 1 of IR0 to select the mode best suited for the system environment. The CNTRL1 – 3 outputs perform different functions for each mode and are named accordingly in the description of each mode.

Independent Mode

The CPU to RAM interface configuration for this mode is illustrated in Figure 2. Transfer of data between the CPU and display memory is accomplished via a bidirectional latched port and is controlled by the signals read data buffer ($\overline{RDB}$), write data buffer ($\overline{WDB}$), and

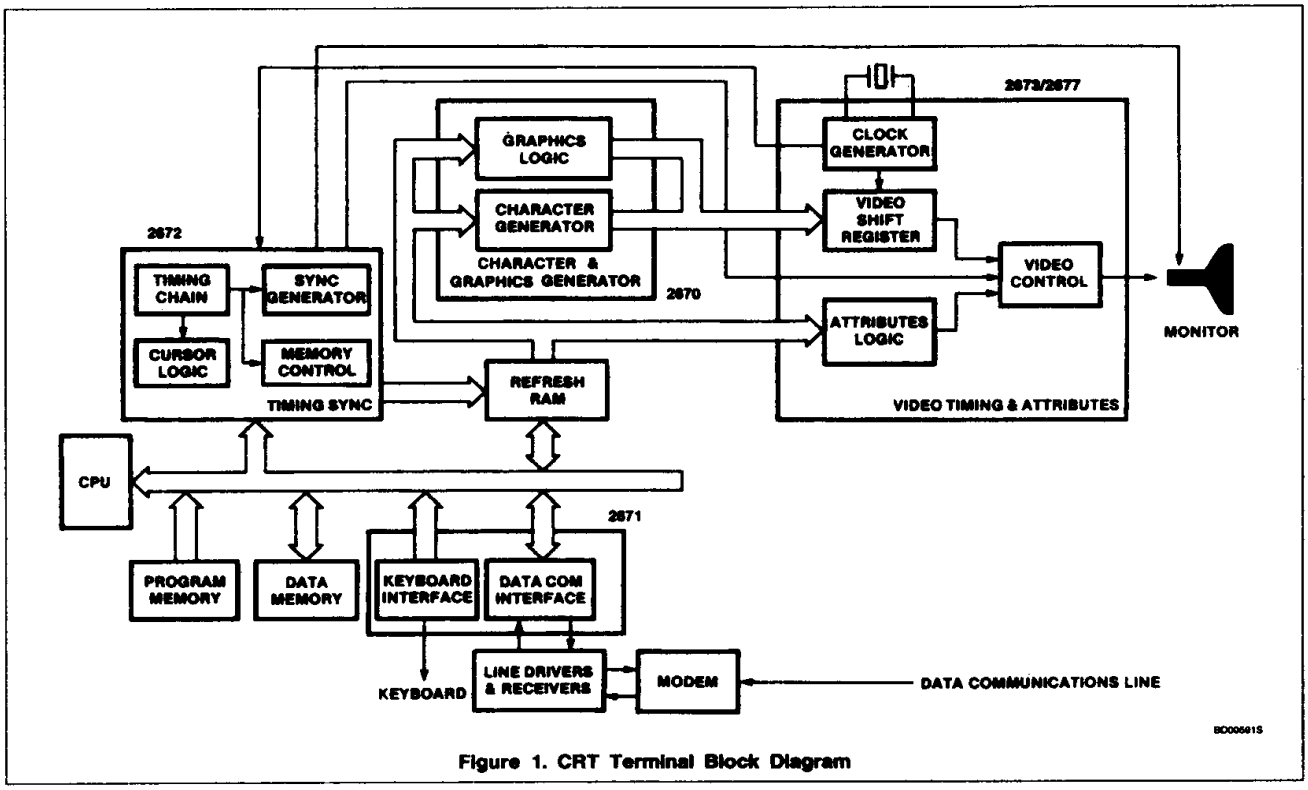


Figure 1. CRT Terminal Block Diagram

buffer chip enable ($\overline{BCE}$). This mode provides a non-contention type of operation that does not require address multiplexers. The CPU does not address the memory directly — the read or write operation is performed at the address contained in the cursor address register or the pointer address register as specified by the CPU. The PVTC enacts the data transfers during blanking intervals in order to prevent visual disturbances of the displayed data.

For a data buffer write command, the $\overline{WDB}$ signal will go active on the rising edge of character clock ($\overline{CCLK}$) and will remain so until the next $\overline{CCLK}$ rising edge. $\overline{BCE}$ is always in the active state except before and after a $\overline{WDB}$ command. When a write has been executed, $\overline{BCE}$ becomes inactive on the falling edge of $\overline{CCLK}$. When the write occurs ($\overline{WDB}$ active) on the next rising edge, $\overline{BCE}$ also becomes active. $\overline{BCE}$ and $\overline{WDB}$ both become inactive on the rising edge of $\overline{CCLK}$. $\overline{BCE}$ will then return to the active state on the next falling edge if there is no other write command to be executed.

The CPU manages the data transfers by supplying commands to the PVTC. The commands used are:

1. Read/Write at pointer address.
2. Read/Write at cursor address (with optional increment of address).
3. Write from cursor address to pointer address.

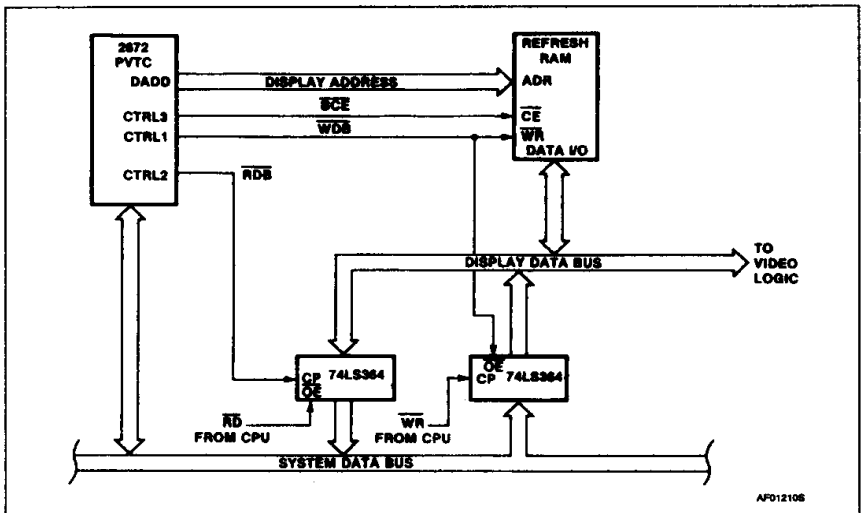
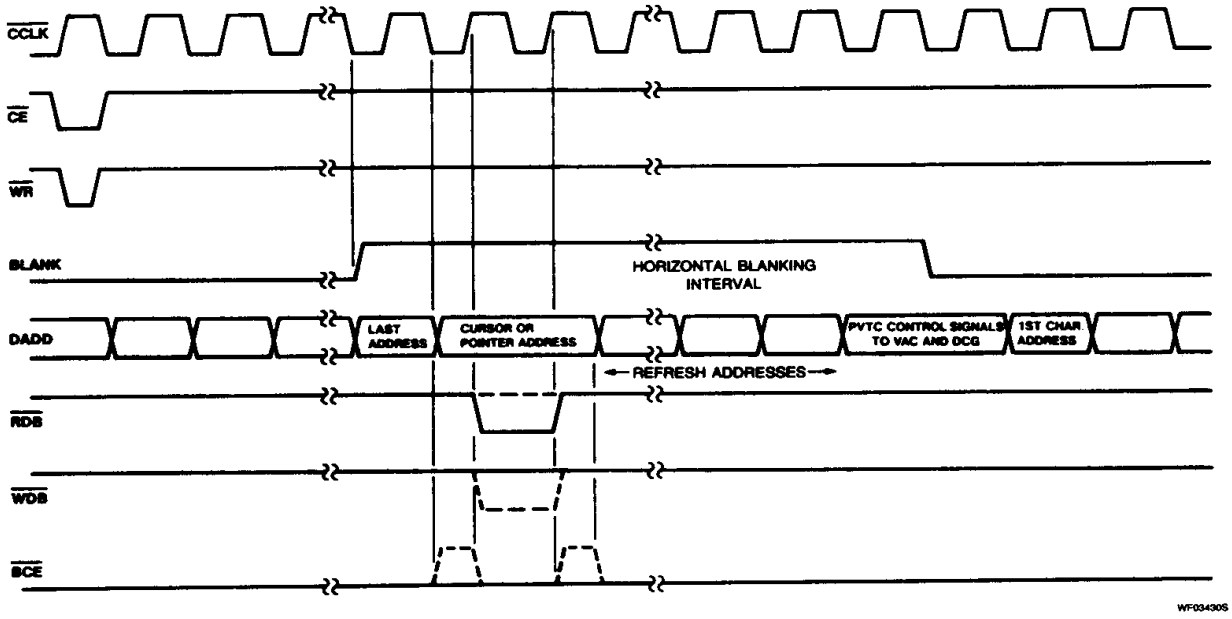


Figure 2. Independent Buffer Mode Configuration

The operational sequence for a write operation is:

1. CPU checks RDFLG status bit to assure that any previous operation has been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes address into cursor or pointer registers.



NOTE:
Write waveforms shown in dotted lines.

Figure 3. Read/Write at Cursor/Pointer Command Timing (Command Received During Active Display Window)

4. CPU issues 'write at cursor with/without increment' or 'write at pointer' command.
5. PVTC generates control signals and outputs specified address to perform requested operation. Data is copied from the interface latch into the memory.
6. PVTC sets RDFLG status to indicate that the write is completed.

Similarly, a read operation proceeds as follows:

1. Steps 1 and 3 as above.
2. CPU issues 'read at cursor with/without increment' or 'read at pointer' command.
3. PVTC generates control signals and outputs specified address to perform requested operation. Data is copied from memory to the interface latch and PVTC sets RDFLG status to indicate that the read is completed.
4. CPU checks RDFLG status to see if operation is completed.
5. CPU reads data from interface latch.

Loading the same data into a block of display memory is accomplished via the 'write from cursor to pointer' command:

1. CPU checks RDFLG status bit to assure that any previous operation has been completed.
2. CPU loads data to be written to display memory into the interface latch.
3. CPU writes beginning address of memory block into cursor address register and ending address of block into pointer address register.

   issues 'write from cursor to pointer' command.
5. PVTC generates control signals and outputs block addresses to copy data from the interface latch into the specified block of memory.
6. PVTC sets RDFLG status to indicate that the block write is completed.

Similar sequences can be implemented on an interrupt driven basis using the READY interrupt output to advise the CPU that a previously requested command has been completed.

Two timing sequences are possible for the 'read/write at cursor/pointer' commands. If the command is given during the active display window (defined as first scan line of the first character row to the last scan line of the last character row), the operation takes place during the next horizontal blanking interval, as illustrated in Figure 3. If the command is given during the vertical blanking interval, or while the display has been commanded blanked, the operation takes place immediately. In the latter case, the execution time for the command is approximately one microsecond plus six (6) character clocks (see Figure 4).

Timing for the 'write from cursor to pointer' operation is shown in Figure 5. The BLANK output is asserted automatically and remains asserted until the horizontal retrace interval following completion of the command. The memory is filled at a rate of one location per two character times, plus a small amount of overhead.

Shared And Transparent Buffer Modes

In these modes the display buffer RAM is a part of the CPU memory domain and is addressed directly by the CPU. Both modes use the same hardware configuration with the CPU accessing the display buffer via 3-State drivers (see Figure 6). The processor bus request ($\overline{PBREQ}$) control signal informs the PVTC that the CPU is requesting access to the display buffer. In response to this request, the PVTC raises bus acknowledge ($\overline{BACK}$) until its bus external ($\overline{BEXT}$) output has freed the display address and data busses for CPU access. $\overline{BACK}$, which can be used as a 'hold' input to the CPU, is then lowered to indicate that the CPU can access the buffer.

In transparent mode, the PVTC delays the granting of the buffer to the CPU until a vertical or horizontal blanking interval, thereby causing minimum disturbance of the display. In shared mode, the PVTC will blank the display and grant immediate access to the CPU. Timing for these modes is illustrated in Figures 7, 8, and 9.

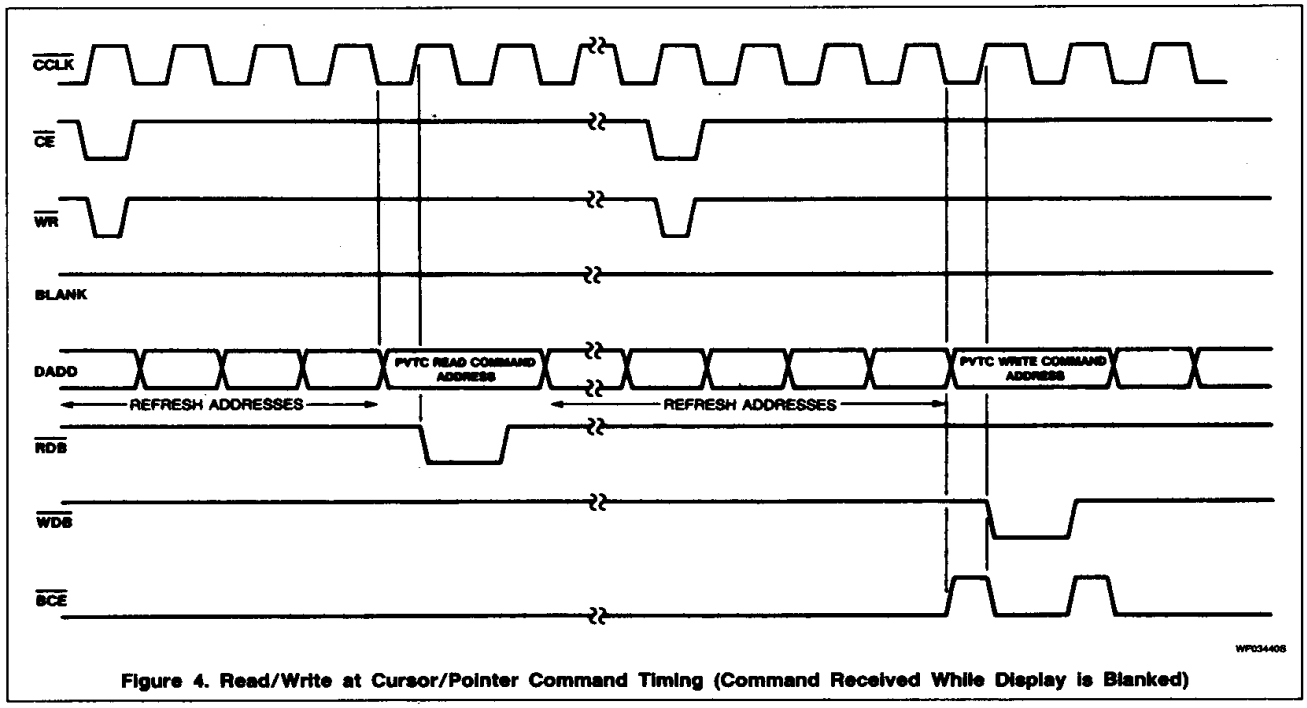


Figure 4. Read/Write at Cursor/Pointer Command Timing (Command Received While Display is Blanked)

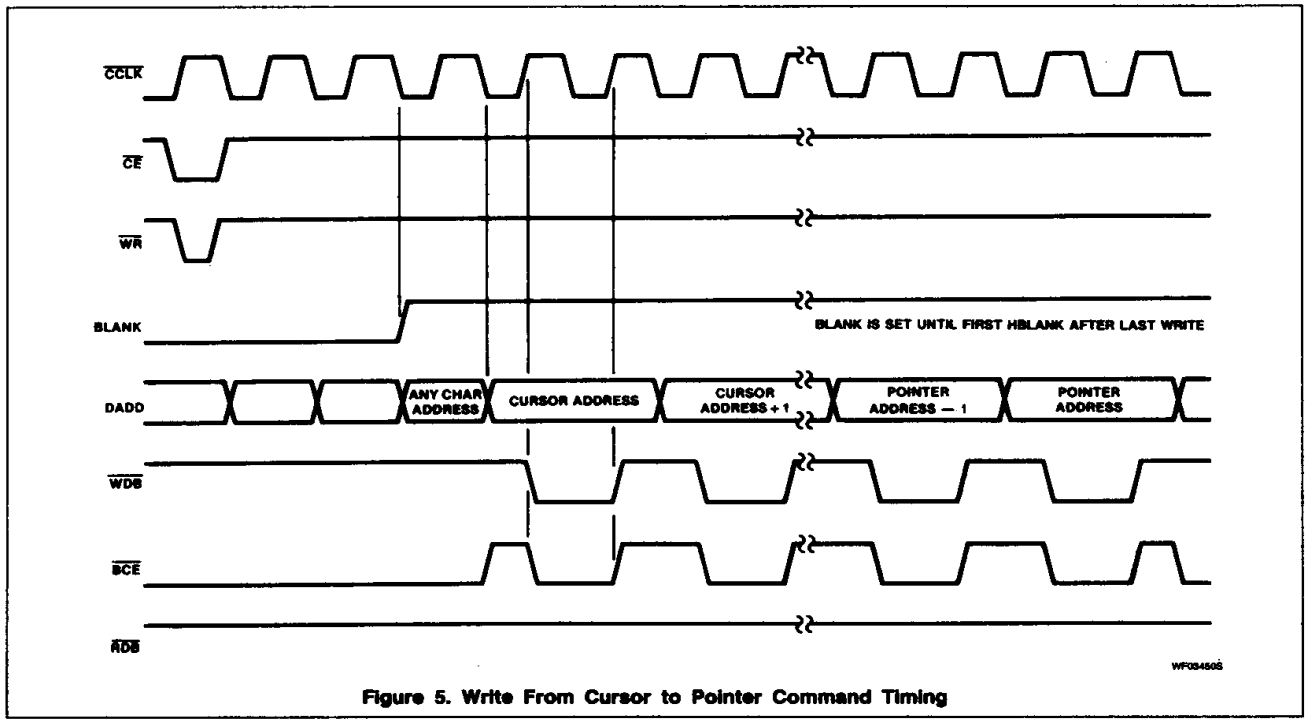


Figure 5. Write From Cursor to Pointer Command Timing

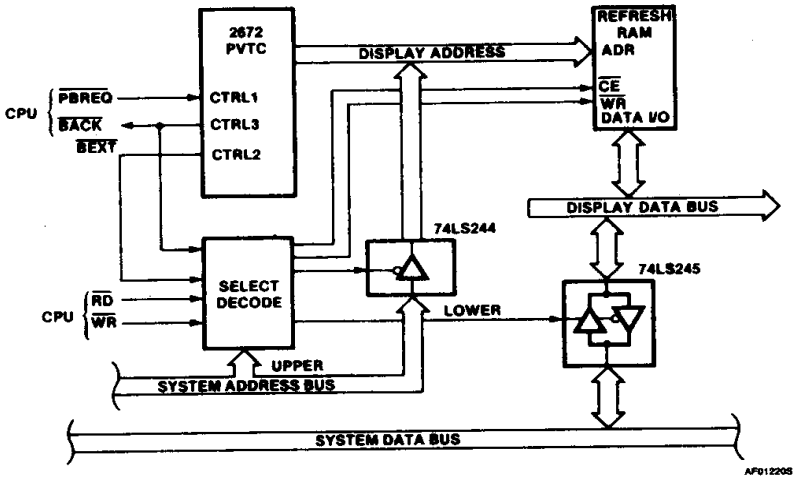
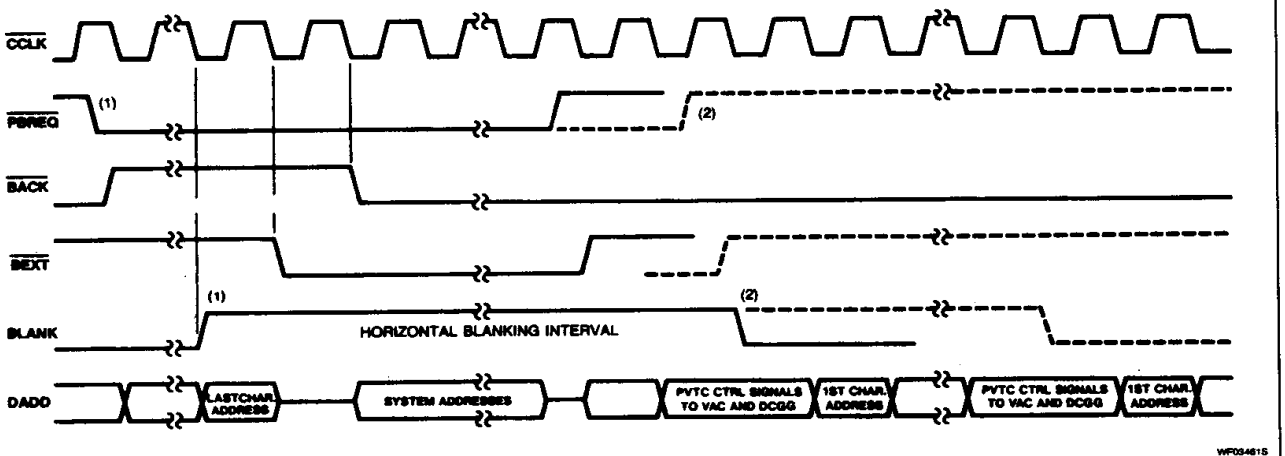
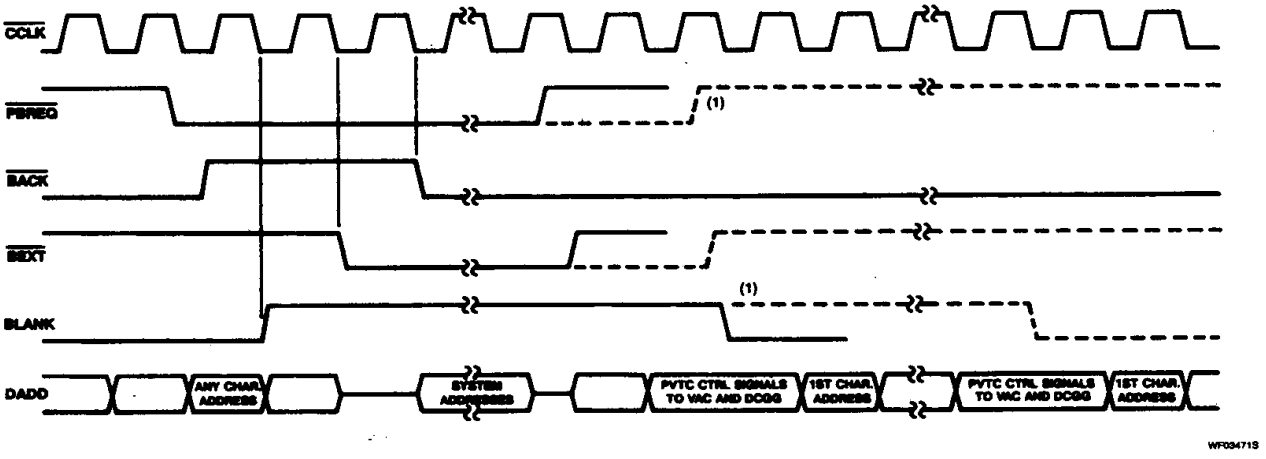


Figure 6. PVTC Shared or Transparent Buffer Modes



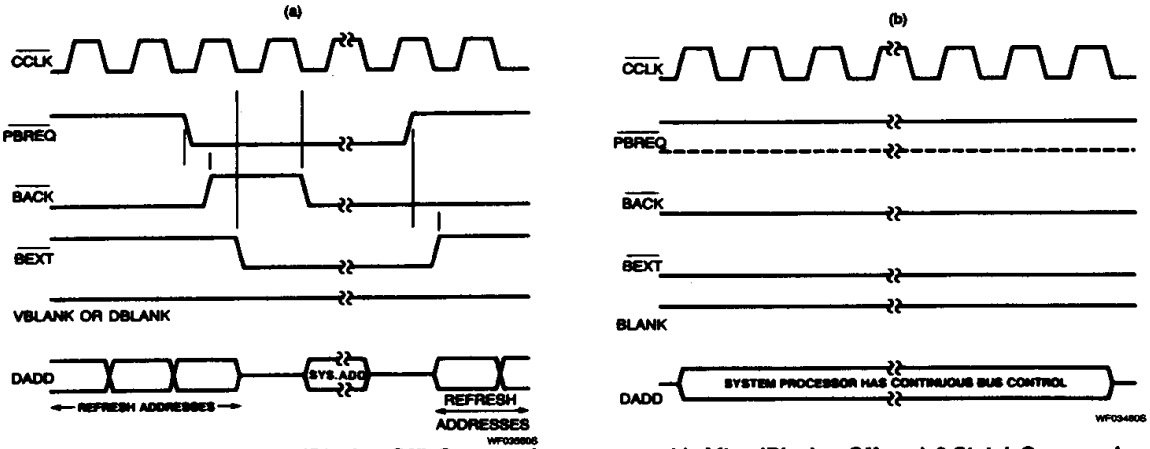
NOTES:
1. PBREQ must be asserted prior to the rising edge of BLANK in order for sequence to begin during that blanking period.
2. If PBREQ is negated after the next to last CCLK of the horizontal blanking interval, the next scan line will also be blanked.

Figure 7. Transparent Buffer Mode Timing



NOTE:
1. If $\overline{PBREQ}$ is negated after the next to last $\overline{CCLK}$ of the horizontal blanking interval, the next scan line will also be blanked.

Figure 8. Shared Buffer Mode Timing



a) During Vertical Blank or After 'Display Off' Command

b) After 'Display Off and 3-State' Command

Figure 9. Shared and Transparent Mode Timing

Row Buffer Mode

Figures 10 and 11 show the timing and a typical hardware implementation for the row buffer mode. During the first scan line (line 0) of each character row, the PVTC halts the CPU and DMAs the next row of character data from the system memory to the row buffer memory. The PVTC then releases the CPU and displays the row buffer data for the programmed number of scan lines. The bus request control ($\overline{BREQ}$) signal informs the CPU that character addresses and the memory bus control (MBC) signal will start at the next falling edge of BLANK. The CPU must release the address and data buses before this time to prevent bus contention. After the row of character data is transferred to the row buffer RAM, $\overline{BREQ}$ returns high to grant memory control back to the CPU.

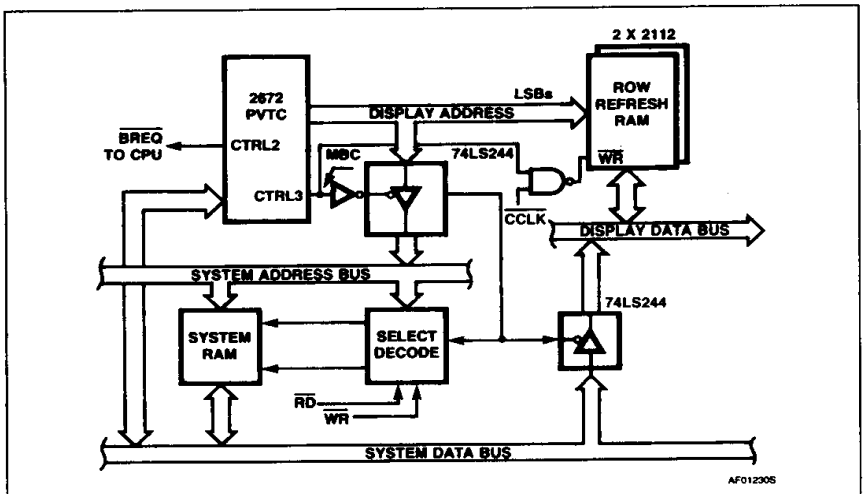


Figure 10. Row Buffer Mode Configuration

OPERATION

After power is applied, the PVTC will be in an inactive state. Two consecutive 'master reset' commands are necessary to release this circuitry and ready the PVTC for operation. Two register groups exist within the PVTC: the initialization registers and the display control registers. The initialization registers select the system configuration, monitor timing, cursor shape, display memory domain, and screen format. These are loaded first and normally require no modification except for certain special visual effects. The display control registers specify the memory address of the base character (upper left corner of screen), the cursor position, and the pointer address for independent memory access mode. These usually require modification during operation.

After initial loading of the two register groups, the PVTC is ready to control the monitor screen. Prior to executing the PVTC commands which turn on the display and cursor, the user should load the display memory with the first data to be displayed. During operation, the PVTC will sequentially address the display memory within the limits programmed into its registers. The memory outputs character codes to the system character and graphics generation logic, where they are converted to the serial video stream necessary to display the data on the CRT. The user effects changes to the display by modifying the contents of the display memory, the PVTC display control and command registers, and the initialization registers, if required. Interrupts and status conditions generated by the PVTC supply the 'handshaking' information necessary for the CPU to effect the display changes in the proper time frame.

Initialization Registers

There are 11 initialization registers (IR0 – IR10) which are accessed sequentially via a single address. The PVTC maintains an internal pointer to these registers which is incremented after each write at this address until the last register (IR10, the split screen register) is accessed. The pointer then continues to point to the split screen register. Upon power-up or a master reset command, the internal pointer is reset to point to the first register (IR0) of the initialization register group. The internal pointer can also be preset to any register of the group via the 'load IR address pointer' command. These registers are write only and are used to specify parameters such as the system configuration, display format, cursor shape, and monitor timing. Register formats are shown in Table 2.

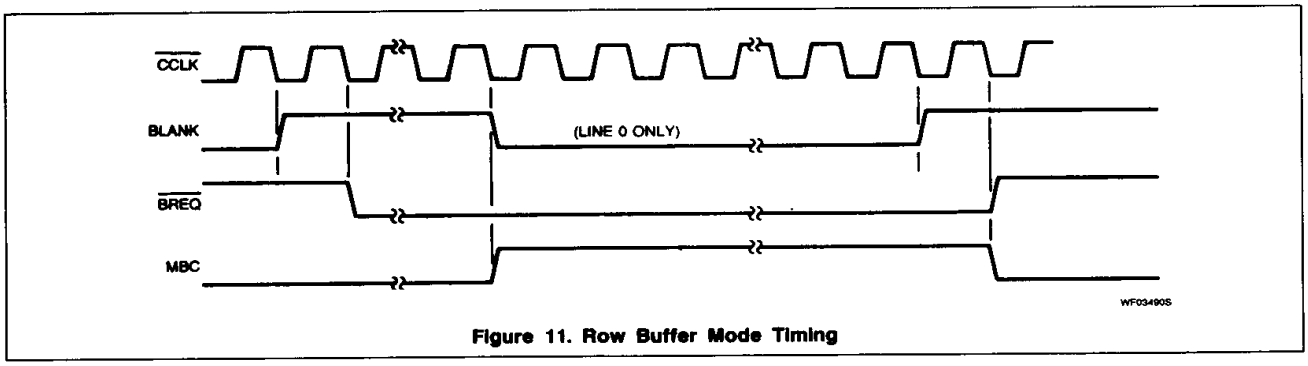


Figure 11. Row Buffer Mode Timing

Table 2. Initialization Register Bit Formats

IR0

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NOT USED	SCAN LINES PER CHARACTER ROW				SYNC SELECT	BUFFER MODE SELECT	
	NON-INTERLACED		INTERLACED				
	0000 = 1 LINE 0001 = 2 LINES 0010 = 3 LINES • • 1110 = 15 LINES 1111 = 16 LINES		0000 = UNDEFINED 0001 = 5 LINES 0010 = 7 LINES • • 1110 = 31 LINES 1111 = UNDEFINED		0 = VSYNC 1 = CSYNC	00 = INDEPENDENT 01 = TRANSPARENT 10 = SHARED 11 = ROW	

IR1

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTERLACE ENABLE	EQUALIZING CONSTANT						
0 = NON-INT 1 = INTER.	00000000 = 1 CCLK 00000001 = 2 CCLK • • 11111110 = 127 CCLK 11111111 = 128 CCLK		CALCULATED FROM: $EC = 0.5(H_{ACT} + H_{FP} + H_{SYNC} + H_{BP}) - 2(H_{SYNC})$				

IR2

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NOT USED	HORIZONTAL SYNC WIDTH				HORIZONTAL BACK PORCH		
	0000 = 2 CCLK 0001 = 4 CCLK • • 1110 = 30 CCLK 1111 = 32 CCLK				000 = 1 CCLK 001 = 5 CCLK • • 110 = 25 CCLK 111 = 29 CCLK		

IR3

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
VERTICAL FRONT PORCH			VERTICAL BACK PORCH				
000 = 4 SCAN LINES 001 = 8 SCAN LINES • • 110 = 28 SCAN LINES 111 = 32 SCAN LINES			00000 = 4 SCAN LINES 00001 = 6 SCAN LINES • • 11110 = 64 SCAN LINES 11111 = 66 SCAN LINES				

IR4

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CHARACTER BLINK RATE	ACTIVE CHARACTER ROWS PER SCREEN (NOTE 1)						
0 = 1/16 VSYNC 1 = 1/32 VSYNC	00000000 = 1 ROW 00000001 = 2 ROWS • • 11111110 = 127 ROWS 11111111 = 128 ROWS						

NOTE:
In interlace mode with odd total character rows per screen the last character row will be the programmed scan lines per character row minus one.

Table 2. Initialization Register Bit Formats (Continued)

IR5

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
ACTIVE CHARACTERS PER ROW							
00000010 = 3 CHARACTERS 00000011 = 4 CHARACTERS • • 11111110 = 255 CHARACTERS 11111111 = 256 CHARACTERS							

IR6

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
FIRST LINE OF CURSOR				LAST LINE OF CURSOR			
0000 = SCAN LINE 0 0001 = SCAN LINE 1 • • 1110 = SCAN LINE 14 1111 = SCAN LINE 15				0000 = SCAN LINE 0 0001 = SCAN LINE 1 • • 1110 = SCAN LINE 14 1111 = SCAN LINE 15			

IR7

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
LIGHT PEN LINE		CURSOR BLINK	DOUBLE HEIGHT CHAR.	UNDERLINE POSITION			
00 = SCAN LINE 3 01 = SCAN LINE 5 10 = SCAN LINE 7 11 = SCAN LINE 9		0= NO 1= YES	0= NO 1= YES	0000 = SCAN LINE 0 0001 = SCAN LINE 1 • • 1110 = SCAN LINE 14 1111 = SCAN LINE 15			

IR8

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DISPLAY BUFFER FIRST ADDRESS LSB'S							
H'000' = 0 H'001' = 1 • • H'FFE' = 4,094 H'FFF' = 4,095				NOTE: MSB'S ARE IN IR9[3:0]			

IR9

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DISPLAY BUFFER LAST ADDRESS				DISPLAY BUFFER FIRST ADDRESS MSB'S			
0000 = 1,023 0001 = 2,047 • • 1110 = 15,359 1111 = 16,383				SEE IR8			

IR10

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CURSOR BLINK RATE	SPLIT SCREEN INTERRUPT ROW						
0 = 1/16 VSYNC 1 = 1/32 VSYNC	00000000 = ROW 0 00000001 = ROW 1 • • 11111110 = ROW 126 11111111 = ROW 127						

IR0[6:3] — Scan Lines Per Character Row
Both interlaced and non-interlaced scanning are supported by the PVTC. For interlaced mode, two different formats can be implemented, depending on the interconnection between the PVTC and the character generator (see IR1[7]). This field defines the number of scan lines used to compose a character row for each technique. As scanning occurs, the scan line count is output on the LA0 – LA3 and LI pins.

IR0[2] — VS/CS Enable
This bit selects either vertical sync pulses or composite sync pulses on the VSYNC/CSYNC output (pin 18). The composite sync waveform conforms to EIA RS170 standards, with the vertical interval composed of six equalizing pulses, six vertical sync pulses, and six more equalizing pulses.

IR0[1:0] — Buffer Mode Select
Four buffer memory modes may be selectively enabled to accommodate the desired system configuration. See System Configurations.

IR1[7] — Interface Enable
Specifies interlaced or noninterlaced timing operation. Two modes of interlaced operation are available, depending on whether LA0 – LA3 or LI, LA0 – LA2 are used as the line address for the character generator. The resulting displays are shown in Figure 12.

For 'interlaced sync' operation, the same information is displayed in both odd and even fields, resulting in enhanced readability. The PVTC outputs successive line numbers in ascending order on the LA0 – LA3 lines, one per scan line for each field.

The 'interlaced sync and video' format doubles the character density on the screen. The PVTC outputs successive line numbers in ascending order on the LI, LA0 – LA2 lines, one per scan line for each field, but alternates beginning the count with even and odd line numbers. In the interlaced sync and video mode, the number of scan lines per character row is always odd. Assume that the first character row is row 0 (even). When in the odd field, the scan line numbers being displayed are even for even character rows and odd for odd character rows. When in the even field, the scan line numbers being displayed are odd for even character rows and even for odd character rows (see Figure 12c). This provides balanced beam currents in the odd and even fields, thus minimizing character variations due to different loading of the CRT anode supply between fields.

IR1[6:0] — Equalizing Constant
This field indirectly defines the horizontal front porch and is used internally to generate the equalizing pulses for the RS170 compatible CSYNC. The value for this field is the total number of character clocks ($\overline{CCLK}$) during a horizontal line period divided by two, minus two times the number of character clocks in the horizontal sync pulse:

$$EC = \frac{H_{ACT} + H_{FP} + H_{SYNC} + H_{BP}}{2} - 2(H_{SYNC})$$

The definition of the individual parameters is illustrated in Figure 13. The minimum value of H_{FP} is two character clocks.

Note that when using the 2673/2677 VAC, the blank pulse is delayed three CCLKs relative to the HSYNC pulse. Because of this delay, the actual HFP and HBP values will be different from the values programmed into the PVTC. The actual HFP will be decreased by 3 character clocks. The actual HBP will be increased by 3 character clocks.

IR2[6:3] — Horizontal Sync Pulse Width
This field specifies the width of the HSYNC pulse in $\overline{CCLK}$ periods.

IR2[2:0] — Horizontal Back Porch
This field defines the number of $\overline{CCLKs}$ between the trailing edge of HSYNC and the trailing edge of BLANK.

IR3[7:5] — Vertical Front Porch
Programs the number of scan line periods between the rising edges of BLANK and VSYNC during a vertical retrace interval. The width of the VSYNC pulse is fixed at three scan lines.

IR3[4:0] — Vertical Back Porch
This field determines the number of scan line periods between the falling edges of the VSYNC and BLANK outputs.

IR4[7] — Character Blink Rate
Specifies the frequency for the character blink attribute timing. The blink rate can be specified as 1/16 or 1/32 of the vertical field rate. The timing signal has a duty cycle of 75% and is multiplexed onto the DADD11/BLINK output at the falling edge of each BLANK.

IR4[6:0] — Character Rows Per Screen
This field defines the number of character rows to be displayed. This value multiplied by the scan lines per character row, plus the vertical front and back porch values, and the vertical sync pulse width (three scan lines) is the vertical scan period in scan lines.

IR5[7:0] — Active Characters Per Row
This field determines the number of characters to be displayed on each row of the CRT screen. The sum of this value, the horizontal front porch, the horizontal sync width, and the horizontal back porch is the horizontal scan period in $\overline{CCLKs}$.

IR6[7:4], IR6[3:0] — First and Last Scan Line of Cursor
These two fields specify the height and position of the cursor on the character block. The 'first' line is the topmost line when scanning from the top to the bottom of the screen. The value of the first line of cursor must be less than the last line of cursor value.

IR7[7:6] — Light Pen Line Position
This field defines which of four scan lines of the character row will be used for the light pen strike-through attribute by the 2673/2677 VAC. The timing signal is multiplexed onto the DADD9/LPL output during the falling edge of BLANK.

IR7[5] — Cursor Blink Enable
This bit controls whether or not the cursor output pin will be blinked at the selected rate (IR10[7]). The blink duty cycle for the cursor is 50%.

IR7[4] — Double Height Character Row Enable
If enabled, the scan line count will be repeated twice in succession, causing the height of the character row to double. This bit can be changed at any time but will only become effective at the beginning of the character row following the time it is changed. This allows selected character rows to be of double height. The split screen interrupt can be used to notify the CPU when to effectuate changes to this bit. For each double height row which replaces a normal row, one row count should be subtracted from the 'character rows per screen' field (IR4) to maintain the same total number of scan lines per field.

IR7[3:0] — Underline Position
This field defines which scan line of the character row will be used for the underline attribute by the 2673/2677 VAC. The timing signal is multiplexed onto the DADD10/UL output during the falling edge of BLANK.

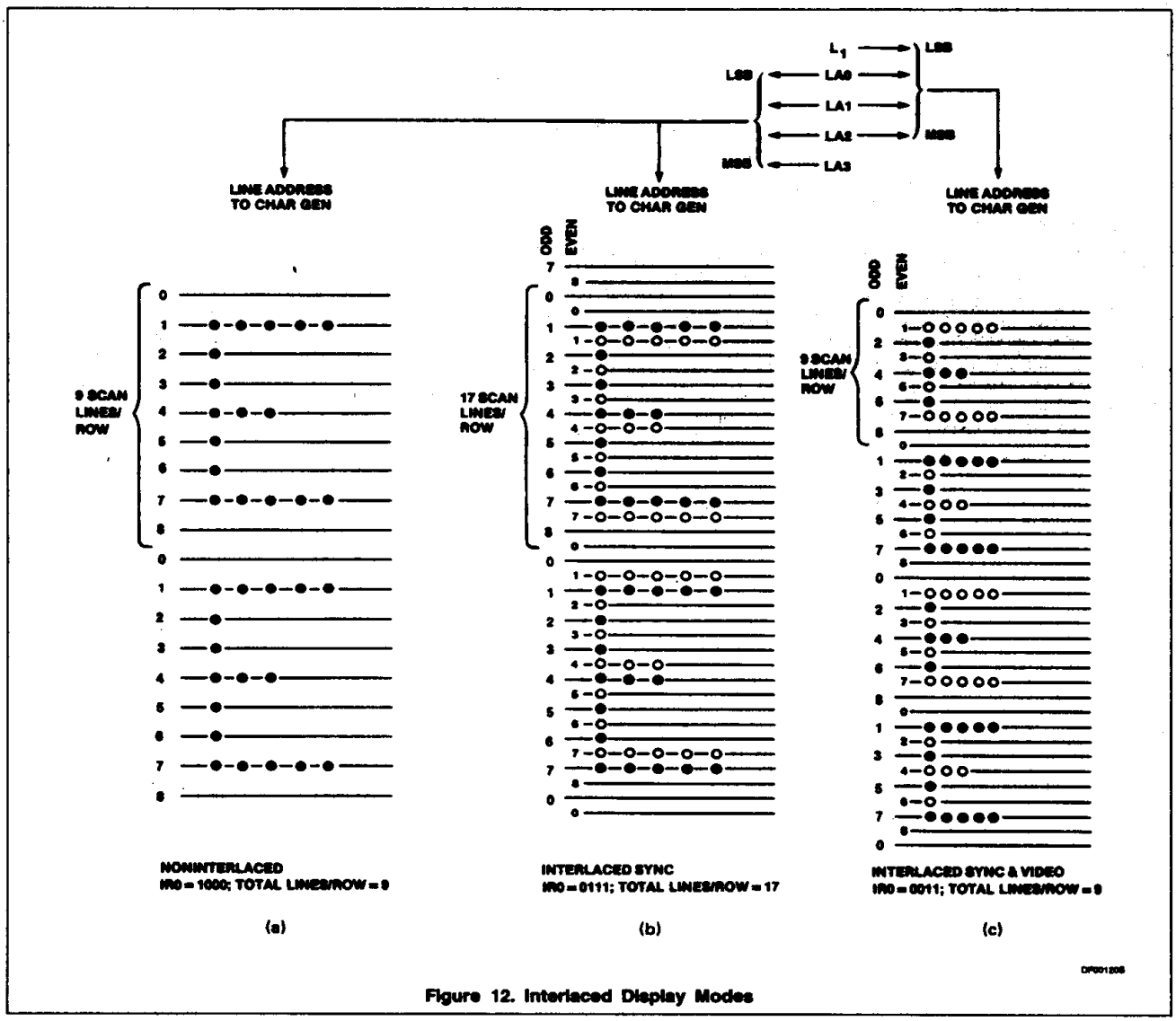


Figure 12. Interlaced Display Modes

IR9[3:0], IR8[7:0] — Display Buffer First Address

IR9[7:4] — Display Buffer Last Address
These two fields define the area within the buffer memory where the display data will reside. When the data at the 'display buffer last address' is displayed, the PVTC will wraparound and obtain the data to be displayed at the next screen position from the 'display buffer first address'. If 'last address' is the end of a character row and a new screen start address has been loaded into the screen start register, or if 'last address' is the last character position of the screen, the next data is obtained from the address contained in the screen start register.

Note that there is no restriction in displaying data from other areas of the addressable memory. Normally, the area between these two bounds is used for data which can be overwritten (e.g., as a result of scrolling), while data that is not to be overwritten would be contained outside these bounds and accessed by means of the split screen interrupt feature of the PVTC.

IR10[7] — Cursor Blink Rate
The cursor blink rate can be specified at 1/16 or 1/32 of the vertical scan frequency. Blink is effective only if blink is enabled by IR7[5].

IR10[6:0] — Split Screen Interrupt
The split screen interrupt can be used to provide special screen effects such as a row of double height characters or to change the normal addressing sequence of the display memory. The contents of this field are compared, in real-time, to the current character row number. Upon a match, the PVTC sets the split screen status bit, and issues an interrupt request if so programmed. The status change/interrupt request is made at the beginning of scan line zero of the split screen character row.

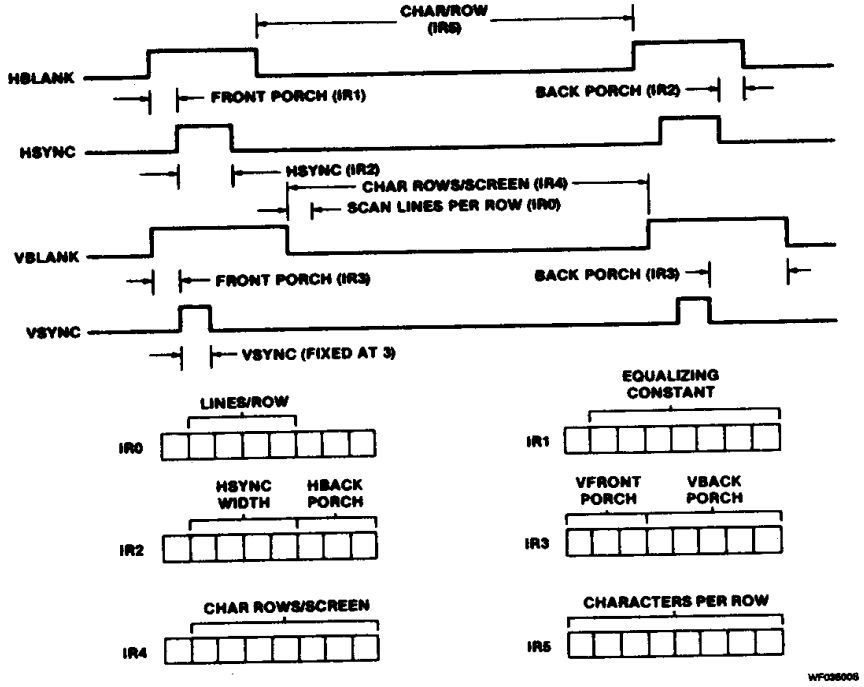


Figure 13. Horizontal and Vertical Timing

Timing Considerations

Normally, the contents of the initialization registers are not changed during operation. However, this may be necessary to implement special display features such as multiple cursors, smooth scrolling, horizontal scrolling, and double height character rows. Table 3 describes timing details for these registers which should be considered when implementing these features.

Table 3. Timing Considerations

PARAMETER	TIMING CONSIDERATIONS
First line of cursor Last line of cursor Light pen line Underline	These parameters must be established at a minimum of two character times prior to their occurrence.
Double height characters	Set/reset during the character row prior to the affected row.
Cursor blink Cursor blink rate Character blank rate	New values become effective within one field after values are changed
Split screen interrupt row	Change anytime prior to line zero of desired row
Character rows per screen	Change only during vertical blanking period
Vertical front porch	Change prior to first line of V_{FP}
Vertical back porch	Change prior to fourth line after V_{SYNC}
Screen start register	Change prior to the horizontal blanking interval of the last line of character row prior to the affected row.

Display Control Registers

There are nine registers in this group, each with an individual address. Their formats are illustrated in Table 4. The command register is used to invoke one of 16 possible PVTC commands as described in the COMMANDS section of this data sheet. The remaining registers in the group store address values which specify the cursor and buffer pointer locations, the location of the first character to be displayed on the screen, and the location of a light pen 'hit'. With the exception of the light pen register, the user initializes these registers after powering on the system and changes their values to control the data which is displayed.

Screen Start Registers

The screen start registers contain the address of the first character of the first row (upper left corner of the active display). At the beginning of the first scan line of the first row, this address is transferred to the row start register (RSR) and into the memory address counter (MAC). The counter is then advanced sequentially at the character rate the number of times programmed into the active characters per row register (IR5), thus reaching the address of the last character of the row plus one. At the beginning of each subsequent scan line of the first row, the MAC is reloaded from the RSR and the above sequence is repeated. At the end of the last scan line of the first row, the contents of the MAC are loaded into the RSR to serve as the starting memory address for the second character

row. This process is repeated for the programmed number of rows per screen. Thus, the data in the display memory is displayed sequentially starting from the address contained in the screen start register. After the ensuing vertical retrace interval the contents of the screen registers are reloaded into the RSR and MAC and the process is repeated.

The sequential operation described above will be modified upon the occurrence of either of two events. First, if during the incrementing of the memory address counter the 'display buffer last address' (IR9[7:4]) is reached, the MAC will be loaded from the 'display buffer first address' register (IR9[3:0], IR8[7:0]), at the next character clock. Sequential operation will then resume starting from this address. This wraparound operation allows portions of the display buffer to be used for purposes other than storage of displayable data and is completely automatic without any CPU intervention (see Figure 14a).

Second, the sequential row to row addressing can also be modified under CPU control. If the contents of the screen start register (upper, lower, or both) are changed during any character row (say row 'n'), the starting address of the next character row (row 'n + 1') will be the new value of the screen start register and addressing will continue sequentially from there. This allows features such as split screen operation, partial scroll, or status line display to be implemented. The split screen interrupt feature of the PVTC is useful in controlling this type of operation. Note that in order to obtain the correct screen display, the screen start register must be reloaded with the original value prior to the end of the vertical retrace. See Figure 14b.

Refresh Addressing
During vertical blanking the address counter operation is modified by stopping the automatic load of the contents of the RSR into the counter, thereby allowing the address outputs to free-run. This allows dynamic memory refresh to occur during the vertical retrace interval. The refresh addressing starts at the last address displayed on the screen and increments by one for each character clock during the retrace interval. If the display buffer last address is encountered, wraparound will occur and refreshing will continue from the display buffer first address.

Cursor Address Registers
The contents of these registers define the buffer memory address of the cursor. If enabled, the cursor output will be asserted when the memory address counter (MAC) matches the value of the cursor address registers. The cursor address registers may be read or written by the CPU or incremented via the 'increment cursor address' command. In independent buffer mode, these registers define a buffer memory address for PVTC controlled access in response to 'read/write at cursor with/without increment' commands, or the first address to be used in executing the 'write from cursor to pointer' command.

Display Pointer Address Registers
These registers define a buffer memory address for PVTC controlled accesses in response to 'read/write at pointer' commands. They also define the last buffer memory address to be written for the 'write from cursor to pointer' command.

Light Pen Address Registers
If the light pen input is enabled, these registers are used to store the current character address upon receipt of a light pen strobe input. Several sources of delay between the display of a character upon the screen and the receipt of a light pen hit can be expected to exist in a system environment. These delays include address pipelining in the character generation circuits, delays in the video generation circuits, and delays in the light detection circuitry itself. These delays cause the value stored in the light pen register to differ from the actual address of the character at which the light pen hit actually was detected. Software must be used to correct this condition.

Interrupt/Status Registers

The interrupt and status registers provide information to the CPU to allow it to interact with the PVTC to effect desired changes to implement various display operations. The interrupt register provides information on five possible interrupting conditions, as shown in Table 5. These conditions may be selectively enabled or disabled (masked) from causing interrupts by certain PVTC commands. An interrupt condition which is enabled (mask bit equal to one) will cause the $\overline{INTR}$ output to be asserted and will cause the corresponding bit in the interrupt register to be set-upon occurrence of the interrupting condition. An interrupt condition which is disabled (mask bit equal to zero) has no effect on either the $\overline{INTR}$ output or the interrupt register.

The status register provides six bits of status information: the five possible interrupting conditions plus the RDFLG bit. For this register, however, the contents are not affected by the state of the mask bits.

Descriptions of each interrupt/status register bit follow. Unless otherwise indicated, a bit, once set, will remain set until reset by the CPU by issuing a 'reset interrupt/status bits' command. The bits are also reset by a 'master reset' command and upon power-up. This bit is set to a one upon a master reset.

SR[5] — RDFLG
This bit is present in the status register only. A zero indicates that the PVTC is currently executing the previously issued command. A one indicates that the PVTC is ready to accept a new command.

Table 4. Display Control Register Formats

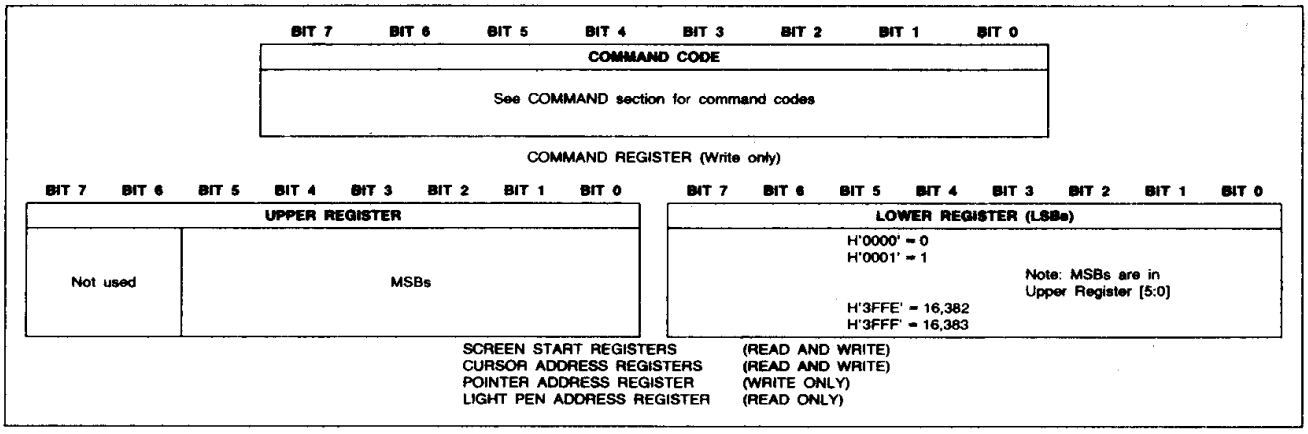


Table 5. Interrupt and Status Register Format

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Not used always read as 0		RDFLG	VBLANK	LINE ZERO	SPLIT SCREEN	READY	LIGHT PEN
		0 = Busy 1 = Ready *	0 = No 1 = Yes	0 = No 1 = Yes	0 = No 1 = Yes	0 = Busy 1 = Ready	0 = No 1 = Yes

NOTE:
*Status register only. Always 0 when reading interrupt register.

I/SR[4] — VBLANK
Indicates the beginning of a vertical blanking interval. Is set to a one at the beginning of the first scan line of the vertical front porch.

I/SR[3] — Line Zero
Is set to a one at the beginning of the first scan line (line 0) of each active character row.

I/SR[2] — Split Screen
This bit is set when a match occurs between the current character row number and the value contained in the split screen interrupts register, IR10[6:0]. The equality condition is only checked at the beginning of line zero of each character row. This bit is reset when either of the screen start registers is loaded by the CPU.

I/SR[1] — Ready
Certain PVTC commands affect the display and may require the PVTC to wait for a blanking interval before enacting the command. This bit is set to one when execution of the command has been completed. No command should be invoked until the prior command is completed. This bit is set to a zero upon a master reset.

I/SR[0] — Light Pen
A one indicates that a light pen hit has occurred and that the contents of the light pen register have been updated. This bit will be reset when either of the light pen registers is read.

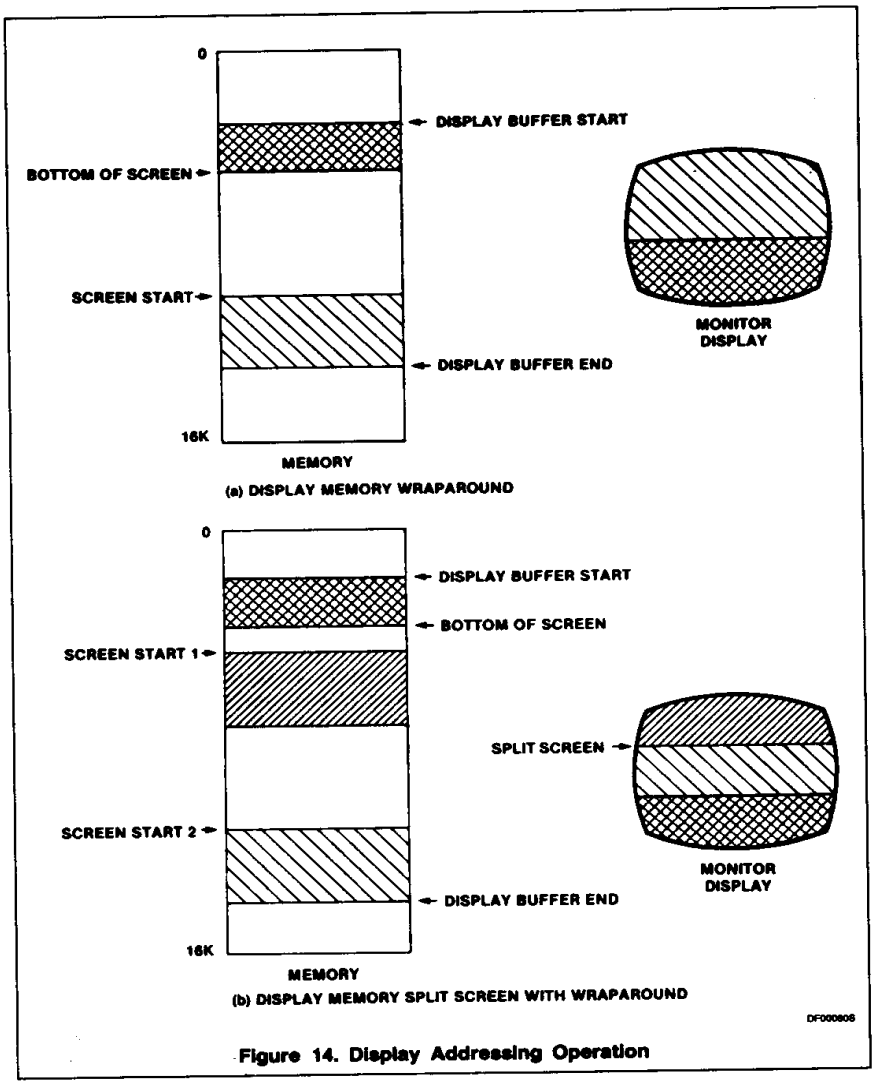


Figure 14. Display Addressing Operation

COMMANDS

The PVTC commands are divided into two classes: the instantaneous commands, which are executed immediately after they are invoked, and the delayed commands which may need to wait for a blanking interval prior to their execution. Command formats are shown in Table 6. The commands are asserted by performing a write operation to the command register with the appropriate bit pattern as the data byte.

Instantaneous Commands

The instantaneous commands are executed immediately after the trailing edge of the $\overline{WR}$ pulse during which the command is issued. These commands do not affect the state of the RDFLG or READY interrupt/status bits. However, a command should not be invoked if the RDFLG bit is low.

Master Reset
This command initializes the PVTC and may be invoked at any time to return the PVTC to its initial state. Upon power-up, two successive master reset commands must be applied to release the PVTC's internal power on circuits. In transparent and shared buffer modes, the CNTRL1 input must be high when the command is issued. The command causes the following:

1. VSYNC and HSYNC are driven low for the duration of RESET and BLANK goes

high. BLANK remains high until a 'display on' command is received.
2. The interrupt and status bits and masks are set to zero, except for the RDFLG flag which is set to a one.
3. The transparent mode, cursor off, display off, and light pen disable states are set.
4. The initialization register pointer is set to address IR0.

Load IR Address
This command is used to preset the initialization register pointer with the value 'V' defined by D3 – D0. Allowable values are 0 to 10.

Enable Light Pen
After invoking this command, receipt of a light pen strobe input will cause the light pen register to be loaded with the current buffer memory address and the corresponding interrupt and status flag to be set. Once loaded, further loads are inhibited until either one of the light pen registers are read or a reset function is performed.

Disable Light Pen
Light pen hits will not be recognized.

Display Off
Asserts the BLANK output. The DADD0 through DADD13 display address bus outputs may be optionally placed in the 3-State condition by setting bit 2 to a '1' when invoking the command.

Display On
Restores normal blanking operation either at the beginning of the next field (bit 2 = 1) or at the beginning of the next scan line (bit 2 = 0). Also returns the DADD0-DADD13 drivers to their active state.

Cursor Off
Disables cursor operation. Cursor output is placed in the low state.

Cursor On
Enables normal cursor operation.

Reset Interrupt/Status Bits
This command resets the designated bits in the interrupt and status registers. The bit positions correspond to the bit positions in the registers:

Bit 0 – Light pen

Bit 1 – Ready

Bit 2 – Split screen

Bit 3 – Line zero

Bit 4 – Vertical blank

Disable Interrupts
Sets the interrupt mask to zeros for the designated conditions, thus disabling these conditions from asserting the $\overline{INTR}$ output. Bit position correspondence is as above.

Enable Interrupts
Resets the selected interrupt and status register bits and writes the associated interrupt mask bits to a one. This enables the corresponding conditions to assert the $\overline{INTR}$ output. Bit position correspondence is as above.

Table 6. PVTC Command Formats

D7	D6	D5	D4	D3	D2	D1	D0	Hex	COMMAND
Instantaneous Commands:									
0	0	0	0	0	0	0	0		Master reset
0	0	0	1	V	V	V	V		Load IR pointer with value V (V = 0 to 10)
0	0	1	d	d	d	1	0[1]		Disable light pen
0	0	1	d	d	d	1	1[2]		Enable light pen
0	0	1	d	1	N	d	0[1]		Display off. Float DADD bus if N = 1
0	0	1	d	1	N	d	1[2]		Display on: Next field (N = 1) or scan line (N = 0)
0	0	1	1	d	d	d	0[1]		Cursor off
0	0	1	1	d	d	d	1[2]		Cursor on
0	1	0	N	N	N	N	N		Reset interrupt/status: Bit reset where N = 1
1	0	0	N	N	N	N	N		Disable interrupt: Disable where N = 1
0	1	1	N	N	N	N	N		Enable interrupt: Enables interrupts and resets the corresponding interrupt/status bits where N = 1
				VBZ	LSS	RDP	L		
Delayed Commands:								**Hex**	
1	0	1	0	0	1	0	0	A4	Read at pointer address
1	0	1	0	0	0	1	0	A2	Write at pointer address
1	0	1	0	1	0	0	1	A9	Increment cursor address
1	0	1	0	1	1	0	0	AC	Read at cursor address
1	0	1	0	1	0	1	0	AA	Write at cursor address
1	0	1	0	1	1	0	1	AD	Read at cursor address and increment address
1	0	1	0	1	0	1	1	AB	Write at cursor address and increment address
1	0	1	1	1	0	1	1	BB	Write from cursor address to pointer address

NOTES:
1. Any combination of these three commands is valid.
2. Any combination of these three commands is valid.
3. d = Don't care.

Delayed Commands

This group of commands is utilized for the independent buffer mode of operation, although the 'increment cursor' command can also be used in other modes. With the exception of the 'write from cursor to pointer' and 'increment cursor' commands, all the commands of this type will be executed immediately or will be delayed depending on when the command is invoked. If invoked during the active screen time, the command is executed at the next horizontal blanking interval. If invoked during a vertical retrace interval or a 'display off' state, the command is executed immediately.

The 'increment cursor' and 'write from cursor to pointer' commands are executed immediately after they are issued. 'Increment cursor' requires approximately three $\overline{CCLK}$ periods for completion. 'Write from cursor to pointer' asserts the BLANK output during its execution. BLANK will not be released until the beginning of the horizontal blanking interval following the last write operation. This will allow more than one 'write from cursor to pointer' command to be executed during one frame and will blank the screen for the time required to execute the command.

In all cases, the PVTC will assert the READY/RDFLG status to signify completion of the command. No other commands should be given until the current command is completed. Therefore, the READY interrupt or RDYFLG status flag should be used for handshaking control between the PVTC and CPU when using these commands.

Read/Write at Pointer
Transfers data between the display buffer the bus interface latch using the address contained in the pointer register.

Read/Write at Cursor
Transfers data between the display buffer and the bus interface latch using the address contained in the cursor register.

Increment Cursor
Adds one (modulo 16k) to the cursor address register.

Read/Write at Cursor and Increment
Transfers data between the display buffer and the bus interface latch using the address contained in the cursor register and then adds one (modulo 16k) to the cursor address register.

Write from Cursor to Pointer
Writes the data contained in the bus interface latch into the block of display memory designated by the cursor address and pointer address registers, inclusive. After completion of the command, the pointer address will be unchanged, but the cursor register contents will be equal to the pointer address.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING	UNIT
T_A	Operating ambient temperature[2]	0 to +70	°C
T_{STG}	Storage temperature range	−65 to +150	°C
	All voltages with respect to ground[3]	−0.5 to +6	V

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = +5.0V \pm 5\%$[4, 5, 6]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IL} V_{IH}	Input low voltage Input high voltage		 0.2		0.8	V V
V_{OL} V_{OH}	Output low voltage Output high voltage (except $\overline{INTR}$ output)	$I_{OL} = 2.4mA$ $I_{OH} = -200\mu A$	 2.4		0.4	V V
I_{IL} I_{LL}	Input leakage current Data bus 3-State leakage current	$V_{IN} = 0$ to V_{CC} $V_O = 0$ to V_{CC}	−10 −10		10 10	μA μA
I_{OD} I_{CC}	$\overline{INTR}$ open drain output leakage current Power supply current	$V_O = 0$ to V_{CC}			10 160	μA mA

NOTES:
1. Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying voltages greater than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND).
6. Typical values are at +25°C, typical processing parameters.
7. For testing, all input signals swing between 0.4V and 2.4V with a transition time of 20ns maximum. All time measurements are referenced at input voltages of 0.8V and 2V and output voltages of 0.8V and 2V as appropriate.
8. Test condition for outputs: $C_L = 150pF$.
9. Timing is illustrated and specified to $\overline{WR}$ and $\overline{RD}$ inputs. Device may also be operated with $\overline{CE}$ as the 'strobing' input. In this case, all timing specifications apply referenced to falling and rising edges of $\overline{CE}$.
10. This specification requires that the $\overline{CE}$ input be negated (high) between read and/or write cycles.
11. $\overline{BCE}$, $\overline{WDB}$,and $\overline{RDB}$ delays track each other within 10ns. Also, these output delays will tend to follow direction (min/max) of DADD0 – 13 delays.
12. These values were measured with a capacitance load of 150pF. To adjust the output delay,use the following correction factor: $50pF \leq C_L < 150pF$: −0.15ns/pF.

AC ELECTRICAL CHARACTERISTICS T_A = 0 to +70°C, V_{CC} = +5.0V ±5%[4, 5, 6, 7, 8]

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS				UNIT
			2.7MHz		4.0MHz		
			Min	Max	Min	Max	
Bus timing (Figure 15)[9]							
t_{AS}	A0 – A2 setup time to $\overline{WR}$,$\overline{RD}$ low		30		30		ns
t_{AH}	A0 – A2 hold time from $\overline{WR}$,$\overline{RD}$ high		0		0		ns
t_{CS}	$\overline{CE}$ setup time to $\overline{WR}$,$\overline{RD}$ low		0		0		ns
t_{CH}	$\overline{CE}$ hold time from $\overline{WR}$,$\overline{RD}$ high		0		0		ns
t_{RW}	$\overline{WR}$,$\overline{RD}$ pulse width		250		250		ns
t_{DD}	Data valid after $\overline{RD}$ low			200		200	ns
t_{DF}	Data bus floating after $\overline{RD}$ high			100		100	ns
t_{DS}	Data setup time to $\overline{WR}$ high		150		150		ns
t_{DH}	Data hold time from $\overline{WR}$ high		10		5		ns
t_{CC}	High time from $\overline{CE}$ to $\overline{CE}$[10]						
	Consecutive commands		600		600		ns
	Other accesses		300		300		ns
$\overline{CCLK}$ timing (Figures 16 and 17)							
t_{CCP}	$\overline{CCLK}$ period		370		250		ns
t_{CCH}	$\overline{CCLK}$ high time		125		100		ns
t_{CCL}	$\overline{CCLK}$ low time		125		100		ns
	Output delay from $\overline{CCLK}$ edge[12]						ns
t_{CCD1}	DADD0-13,MBC		40	175	40	150	ns
t_{CCD2}	BLANK,HSYNC,VSYNC/CSYNC, CURSOR, $\overline{BEXT}$,$\overline{BREQ}$,$\overline{BACK}$, $\overline{BCE}$,$\overline{WDB}$, $\overline{RDB}$[11]		40	225	40	200	ns
Other timings (Figures 17 and 18)							
t_{RDL}	READY/RDFLG low from $\overline{WR}$ high[9]			t_{CCP} + 30		t_{CCP} + 30	ns
t_{BAK}	$\overline{BACK}$ high from $\overline{PBREQ}$ low			225		200	ns
t_{BEXT}	$\overline{BEXT}$ high from $\overline{PBREQ}$ high			225		200	ns
t_{LPS}	Light pen strobe setup time to $\overline{CCLK}$ low		120		120		ns
t_{LPH}	Light pen strobe hold time from $\overline{CCLK}$ low		–10		–10		ns
t_{IRL}	$\overline{INTR}$ low from $\overline{CCLK}$ low			225		200	ns
t_{IRH}	$\overline{INTR}$ high from $\overline{WR}$,$\overline{RD}$ high[9]			600		600	ns

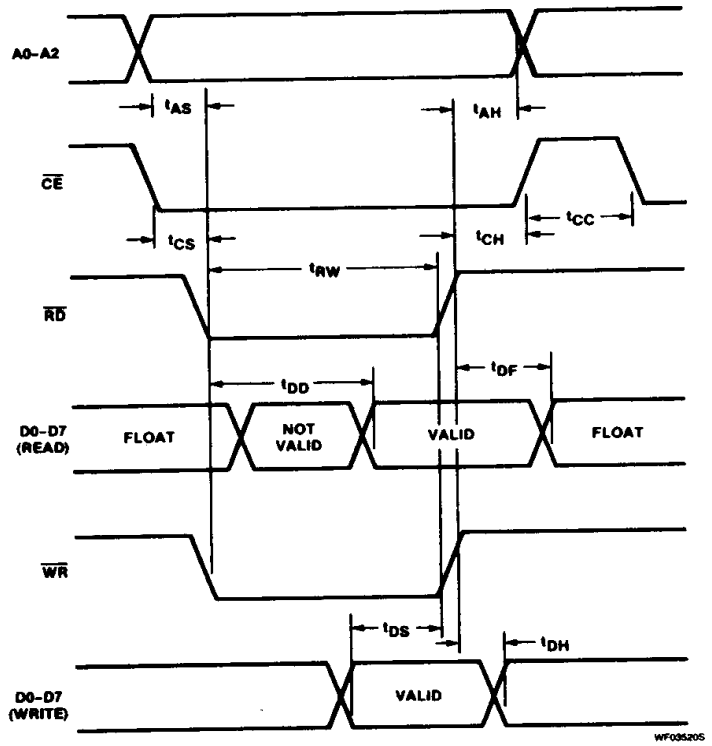
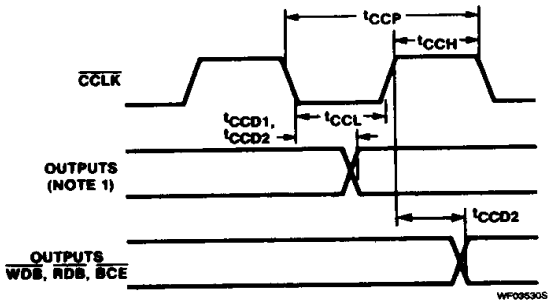


Figure 15. Bus Timing



NOTES:
1. DADD0 - DADD13, BLANK, HSYNC, CSYNC/VSYNC, CURSOR, BEXT, BREQ, BCE, MBC, BACK.
2. BCE changes state on both CCLK edges — (see Figures 3 and 4).

Figure 16. CCLK Timing

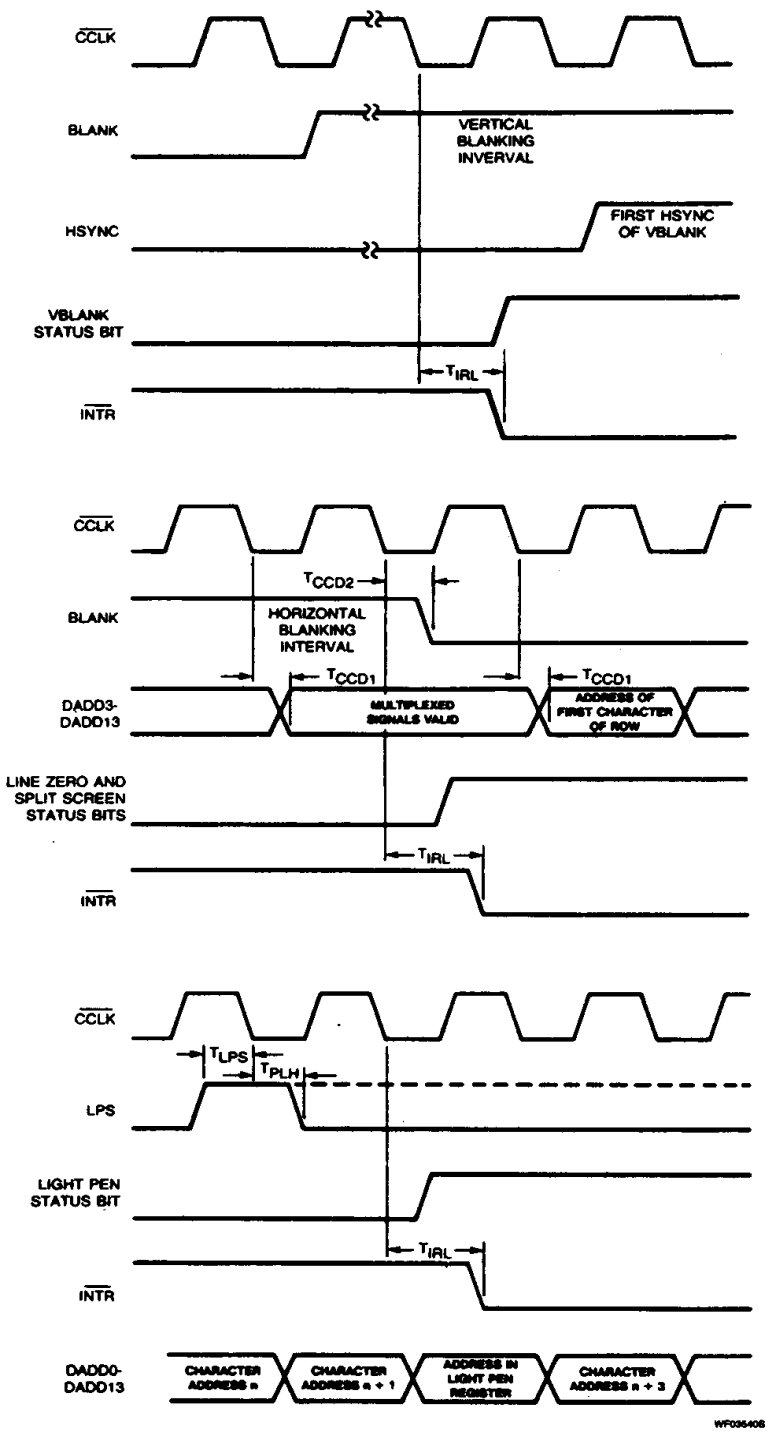


Figure 17. Other Timings

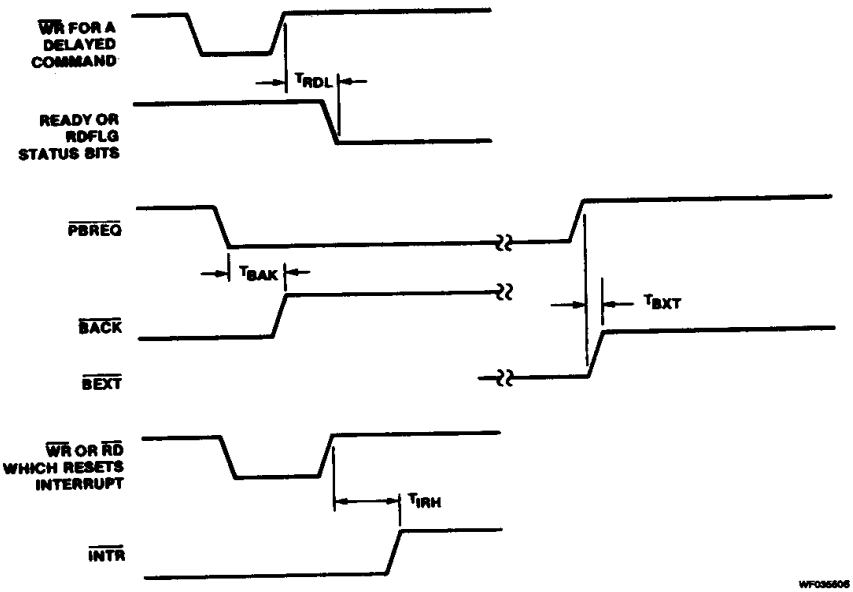
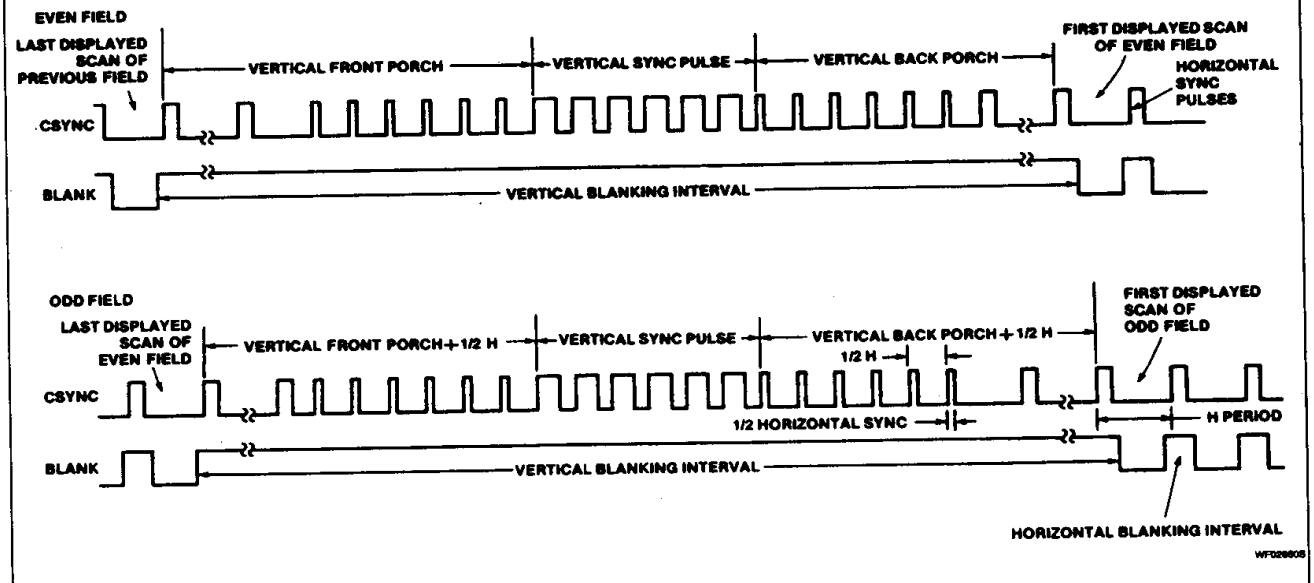


Figure 18. Other Timings



NOTES:
1. In non-interlaced operation the even field is repeated continuously, and the odd field is not.
2. In interlaced operation the even field alternates with the odd field.

Figure 19. Composite Sync Timing