250mA / 3.3V SmartOR™ POWER REGULATOR

Features

- Automatic detection of V_{CC} input supply
- Drive output logic to control external switch
- Glitch-free output during supply transitions
- 250mA output maximum load current
- Built-in hysteresis during supply selection
- Controller operates from either V_{CC} or V_{OUT}
- 8-pin SOIC Narrow package

Applications

- PCI adapter cards
- Network Interface Cards (NIC's)
- Dual power systems
- Systems with standby capabilities
- See Application Note AP-211

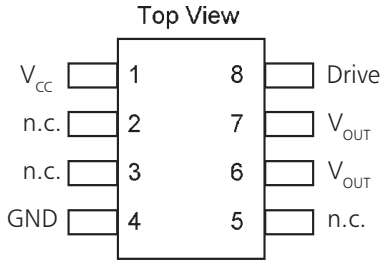
Product Description

California Micro Devices' SmartOR™ CMPWR120 is a low dropout regulator that delivers up to 250mA of load current at a fixed 3.3V output. An internal threshold level (typically 4.1V) is used to prevent the regulator from being operated below dropout voltage. The device continuously monitors the input supply and will automatically disable the regulator when V_{CC} falls below the threshold level. When the regulator is disabled, the control signal "Drive" (Active Low) is enabled, which allows an external PMOS switch to power the load from an auxiliary 3.3V supply.

When V_{CC} is restored to a level above the select threshold, the control signal for the external PMOS switch is disabled and the regulator is once again enabled.

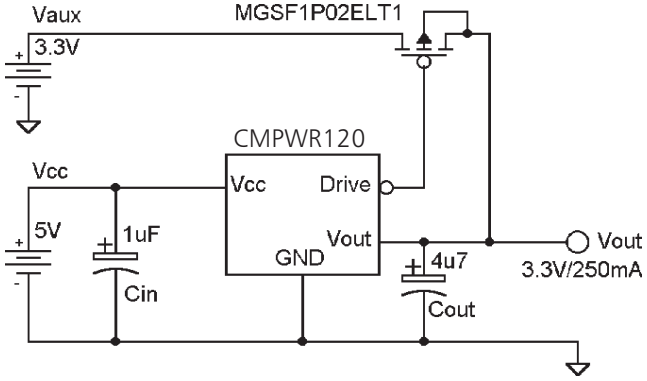
All the necessary control circuitry needed to provide a smooth and automatic transition between the supplies has been incorporated. This allows V_{CC} to be dynamically switched without loss of output voltage.

Pin Diagram

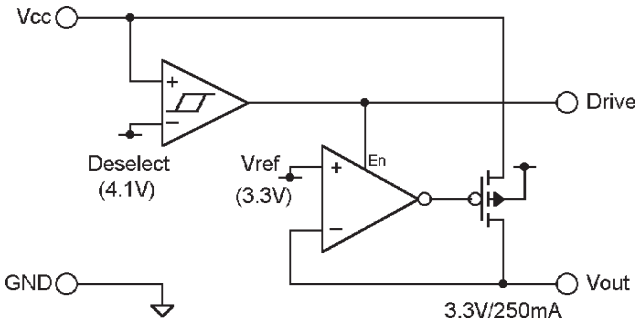


CMPWR120
8-pin SOIC Narrow Package

Typical Application Circuit



Simplified Electrical Schematic



STANDARD PART ORDERING INFORMATION				
Package			Ordering Part Number	
Pins	Style	Part Marking	Tape & Reel	Tubes
8	SOIC Narrow	CMPWR120S	CMPWR120S/R	CMPWR120S/T

C0610999

ABSOLUTE MAXIMUM RATINGS		
Parameter	**Rating**	**Unit**
ESD Protection (HBM)	2000	V
V_{CC} Input Voltage	+6.0, Gnd -0.5	V
Drive Logic Voltage	V_{CC} +0.5, Gnd -0.5	V
Storage Temperature Range	-40 to +150	°C
Operating Ambient	0 to +70	
Operating Junction	0 to +125	
Power Dissipation: SOIC Note 1	0.5	W

OPERATING CONDITIONS		
Parameter	**Range**	**Unit**
V_{CC}	5.0 ± 0.5	V
Temperature (Ambient)	0 to +70	°C
Load Current	0 to 250	mA
C_{EXT}	4.7 ± 10%	µF

ELECTRICAL OPERATING CHARACTERISTICS (over operating conditions unless specified otherwise)						
Symbol	**Parameter**	**Conditions**	**MIN**	**TYP**	**MAX**	**UNIT**
V_{OUT}	Regulator Output Voltage	250mA > I_{LOAD} >0mA	3.135	3.30	3.465	V
I_{OUT}	Regulator Output Current		250			mA
V_{CCSEL}	Select Voltage	Regulator Enabled		4.35	4.45	
V_{CCDES}	Deselect Voltage	Regulator Disabled	3.90	4.10		V
V_{CCHYST}	Hysteresis Voltage	Hysteresis Note 2		0.25		
$I_{S/C}$	Short Circuit Output Current	V_{CC} = 5V, V_{OUT} = 0V		1200		mA
I_{RCC}	V_{CC} Pin Reverse Leakage	V_{OUT} = 3.3V, V_{CC} = 0V		5	50	µA
$V_{R\ LOAD}$	Load Regulation	V_{CC} = 5V, I_{LOAD} = 20mA to 250mA		35		mV
$V_{R\ LINE}$	Line Regulation	V_{CC} = 4.5V to 5.5V, I_{LOAD} = 5mA		2		mV
I_{CC}	Quiescent Supply Current	V_{CC} > V_{CCSEL}, I_{LOAD} = 0mA		1.0	3.0	
		V_{CCDES} > V_{CC} > V_{OUT}		0.15	0.25	mA
		V_{OUT} > V_{CC}		0.01	0.02	
I_{GND}	Ground Pin Current Note 3	V_{CCSEL} (Regulator Disabled)		0.15	0.30	
		V_{CC} = 5V, I_{LOAD} = 5mA		1.0	2.5	mA
		V_{CC} = 5V, I_{LOAD} = 250mA		1.2	3.0	
R_{OH}	Drive Pull-up Resistance	R_{PULLUP} to V_{CC} , V_{CC} > V_{CCSEL}		100	400	Ω
R_{OL}	Drive Pull-down Resistance	$R_{PULLDOWN}$ to GND, V_{CCDES} > V_{CC}		200	400	
t_{DH}	Drive High Delay	C_{DRIVE}=1nF, V_{CC} t_{RISE} < 100ns		1.0		µs
t_{DL}	Drive Low Delay	C_{DRIVE}=1nF, V_{CC} t_{FALL} < 100ns		0.2		

Note 1: The power rating is based on a printed circuit board heat spreading capability equivalent to 2 square inches of copper connected to the GND pins. Typical multi-layer boards using power plane construction will provide this heat spreading ability without the need for additional dedicated copper area. (Please consult with factory for thermal evaluation assistance.)

Note 2: The hysteresis defines the maximum level of acceptable disturbance on V_{CC} during switching. It is recommended that the V_{CC} source impedance be kept below 0.25Ω to ensure the switching disturbance remains below the hysteresis during select/deselect transitions. An input capacitor may be required to help minimize the switching transient.

Note 3: Ground pin current consists of controller current (0.15mA) and regulator current if enabled. The controller always draws 0.15mA from either V_{CC} or V_{OUT}, whichever is greater. All regulator current is supplied exclusively from V_{CC}. At high load currents a small increase occurs due to current limit protection circuitry.

Interface Signals

V_{CC} is the power source for the internal regulator and is monitored continuously by an internal controller circuit.

Whenever V_{CC} exceeds V_{CCSEL} (4.35V typically), the internal regulator (250mA max) will be enabled and deliver a fixed 3.3V at V_{OUT}. When V_{CC} falls below V_{CCDES} (4.10V typically) the regulator will be disabled

Internal loading on this pin is typically 1.0mA when the regulator is enabled, which reduces to 0.15mA whenever the regulator is disabled. If V_{CC} falls below the voltage on the V_{OUT} pin the V_{CC} loading will further reduce to only a few microamperes.

During a V_{CC} power up sequence, there will be an effective step increase in V_{CC} line current when the regulator is enabled. The amplitude of this step increase will depend on the dc load current and any necessary current required for charging/discharging the load capacitance. This line current transient will cause a voltage disturbance at the V_{CC} pin. The magnitude of the disturbance will be directly proportional to the effective power supply source impedance being delivered to the V_{CC} input.

To prevent chatter during Select and Deselect transitions, a built-in hysteresis voltage of 250mV has been incorporated. It is recommended that the power supply connected to the V_{CC} input should have a source resistance of less than 0.25Ω to minimize the event of chatter during the enabling/disabling of the regulator.

An input filter capacitor in close proximity to the V_{CC} pin will reduce the effective source impedance and help minimize any disturbances. If the V_{CC} pin is within a few inches of the main input filter, a capacitor may not be necessary. Otherwise an input filter capacitor in the range of 1uF to 10uF will ensure adequate filtering.

GND is the negative reference for all voltages. The current that flows in the ground connection is very low (typically 1.0mA) and has minimal variation over all load conditions. **V_{OUT}** is the regulator output voltage connection used to power the load. An output capacitor of ten microfarads is used to provide the necessary phase compensation, thereby preventing oscillation. The capacitor also helps to minimize the peak output disturbance during power supply changeover.

When V_{CC} falls below V_{OUT}, then V_{OUT} will be used to provide the necessary quiescent current for the internal reference circuits. This ensures excellent start-up characteristics for the regulator.

DRIVE is an active LOW logic output intended to be used as the control signal for driving an external PFET whenever the regulator is disabled. This will allow the voltage at V_{OUT} to be powered from an auxiliary supply voltage (3.3V).

The Drive pin is pulled HIGH to V_{CC} whenever the regulator is enabled. This ensures that the auxiliary remains isolated during normal regulator operation.

Output Current sinking and sourcing ability of this logic signal is equivalent to 400Ω.

n.c. pins are electrically isolated from the internal circuitry. These pins can be connected to any external voltage level without impacting the device functionality.

PIN FUNCTIONS

Symbol	Description
V_{CC}	Positive Supply input for regulator. When V_{CC} falls below 4.1V, the regulator is disabled.
GND	Negative reference for all voltages.
V_{OUT}	Regulator voltage output (3.3V) regulator when V_{CC} is present. When V_{CC} is not present, the voltage on V_{OUT} is used to bias the internal references.
Drive	CMOS Logic Output intended to control external PMOS switch for selecting an auxiliary voltage supply when V_{CC} is not present.
n.c.	Unconnected pins which are electrically isolated from internal circuitry.

Typical DC Characteristics

Unless stated otherwise, all DC characteristics were measured at room temperature with a nominal V_{CC} supply voltage of 5.0 volts and an output capacitance of 4.7µF. The external PMOS switch was present and resistive load conditions were used.

With normal production devices, the $V_{DESELECT}$ voltage prevents the regulator from operating in dropout mode. For the purposes of obtaining full dropout characteristics, the evaluation test device had access to the $V_{DESELECT}$ voltage. By forcing this voltage artificially low, full dropout characteristics were obtained.

Dropout Characteristics of the regulator are shown in Figure 1. Output regulation under full load conditions is maintained down the line at voltages of 3.6V.

In normal operation, the regulator is deselected at 4.1V, which ensures a regulation output droop of less than 20mV is maintained.

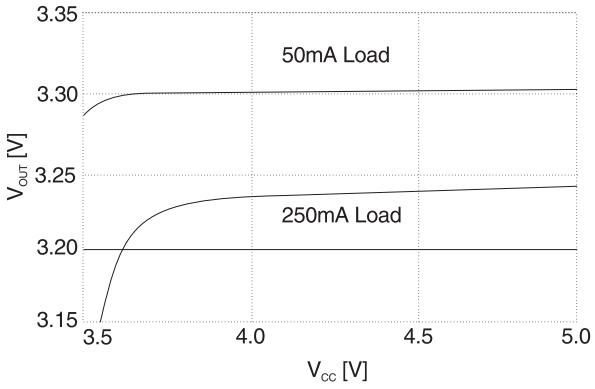


Figure 1. Dropout Characteristics.

Load Regulation performance is shown from zero to maximum rated load in Figure 2. A change in load from 10% to 100% of rated, results in an output voltage change of less than 35mV. This translates into an effective output impedance of approximately 0.15Ω.

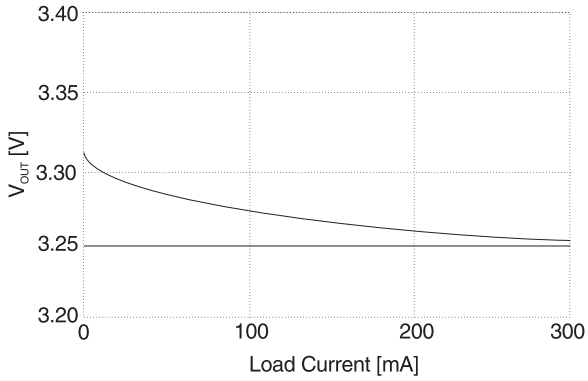


Figure 2. Load Regulation.

Ground Current is shown across the entire range of load conditions. The ground current has minimal variation across the range of load conditions and shows only a slight increase at maximum load. This slight increase at rated load is due to the current limit protection circuitry becoming active.

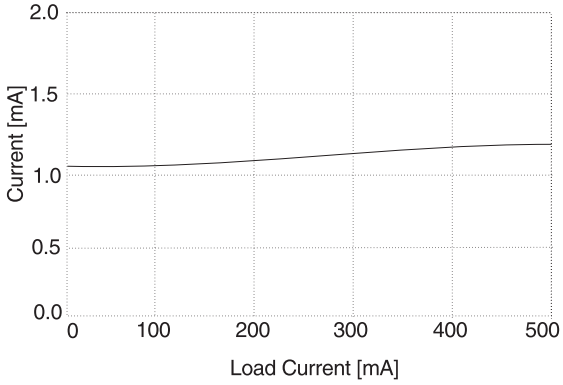


Figure 3. Ground Current.

Typical DC Characteristics (continued)

V_{CC} Supply Current of the device is shown across the entire V_{CC} range for both V_{AUX} present (3.3V) and absent (0V).

In the absence of V_{AUX}, the supply current remains fixed at approximately 0.15mA until V_{CC} reaches the Select voltage threshold of 4.35V. At this point the regulator is enabled and a supply current of 1.0mA is conducted.

When V_{AUX} is present, the V_{CC} supply current is less than 10uA until V_{CC} exceeds V_{AUX}, at which point V_{CC} then powers the controller (0.15mA). When V_{CC} reaches V_{SELECT}, the regulator is enabled.

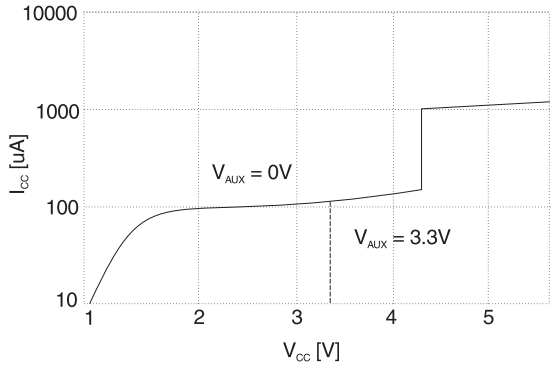


Figure 4. V_{CC} Supply Current (No Load).

Typical Transient Characteristics

The transient characterization test setup shown below includes the effective source impedance of the V_{CC} supply (R_S). This was measured to be approximately 0.2Ω. It is recommended that this effective source impedance be no greater than 0.25Ω to ensure that precise switching is maintained during V_{CC} selection and deselection.

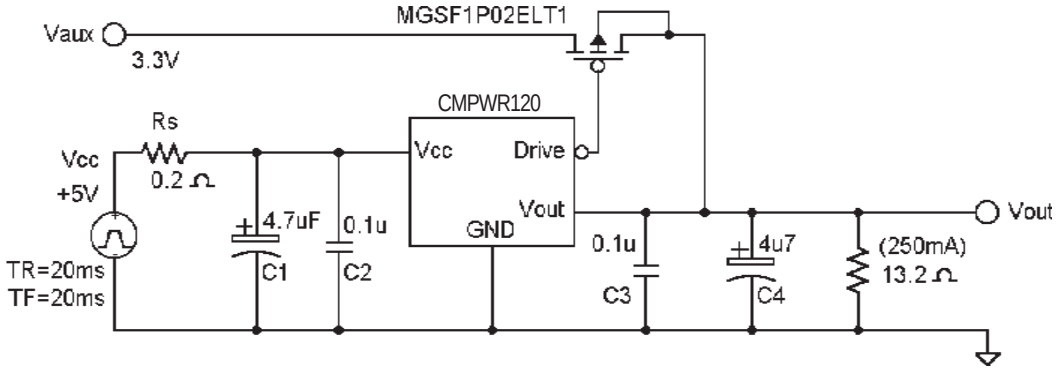
Both the rise and fall times during V_{CC} power-up/down sequencing were controlled at a 20 millisecond duration. This is considered to represent worst case conditions for most application circuits.

A maximum rated load current of 250mA was used during characterization, unless specified otherwise.

During a selection or deselection transition, the DC load current is switching from V_{AUX} to V_{CC} and vice versa. In addition to the normal load current, there may also be an in-rush current for charging/discharging the load capacitor. The total current pulse being applied to either V_{AUX} or V_{CC} is equal to the sum of the dc load and the corresponding in-rush current. Transient currents in excess of 0.5 amps can readily occur for brief intervals when either supply commences to power the load.

The oscilloscope traces of V_{CC} power-up/down show the full bandwidth response at the V_{CC} and V_{OUT} pins under full load (250mA) conditions.

See Application Note AP-211 for more information.



Transient Characteristics Test Setup

Typical Transient Characteristics (continued)

V_{CC} Power-up Cold Start. Figure 5 shows the output response during an initial V_{CC} power-up with V_{AUX} not present. When V_{CC} reaches the select threshold, the regulator turns on. The uncharged output capacitor causes maximum in-rush current to flow, resulting in a large voltage disturbance at the V_{CC} pin of about 200mV. The built-in hysteresis of 250mV ensures the regulator remains enabled throughout the transient.

Prior to V_{CC} reaching an acceptable logic supply level (2V), a disturbance on the Drive pin can be observed.

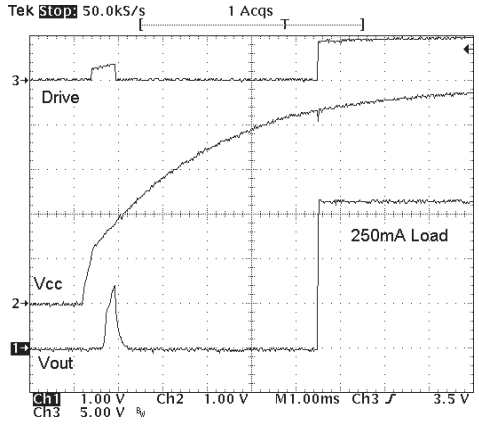


Figure 5. V_{CC} Power-up Cold Start.

V_{CC} Power-up (V_{AUX} =3.3V). Figure 6 shows the output response as V_{CC} approaches the select threshold during a power-up when V_{AUX} is present (3.3V). The output capacitor is already fully charged. When V_{CC} reaches the select threshold, the in-rush current is minimal and the V_{CC} disturbance is only 130mV. The built-in hysteresis of 250mV ensures the regulator remains enabled throughout the transient.

V_{OUT} offset = 3.3V, V_{CC} offset = 4.3V

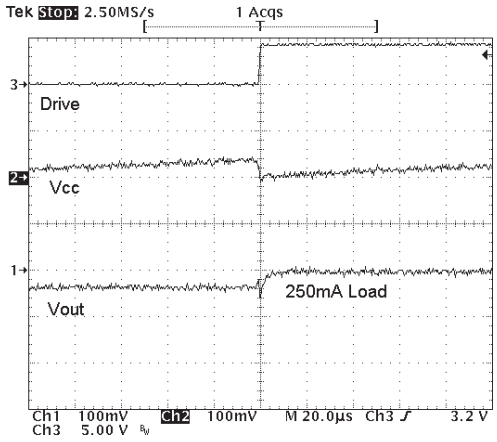


Figure 6. V_{CC} Power-up (V_{AUX} = 3.3V).

V_{CC} Power-up (V_{AUX} = 3.0V). Figure 7 shows the output response as V_{CC} approaches the select threshold during power-up. The auxiliary voltage input is set to the low level of 3.0V. When V_{CC} reaches the select threshold, a modest level of in-rush current is required to further charge the output capacitor resulting in V_{CC} disturbance of 150mV. The built-in hysteresis of 250mV ensures the regulator remains enabled throughout the transient.

The output shows a smooth transition as it ramps from the V_{AUX} voltage up to the regulator output.

V_{OUT} offset = 3.3V, V_{CC} offset = 4.3V

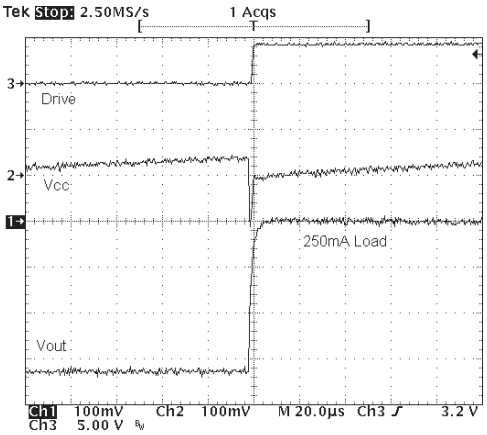


Figure 7. V_{CC} Power-up (V_{AUX} = 3.0V).

V_{CC} Power-down (V_{AUX} = 3.3V). Figure 8 shows the output response as V_{CC} approaches the deselect voltage during a power-down transition with V_{AUX} set to 3.3V. When V_{CC} reaches V_{CCDES} (4.1V), a disturbance of 70mV is observed due to the step change reduction in V_{CC} line current. The built-in hysteresis of 250mV ensures the regulator remains disabled throughout the transient.

(continued)

V_{OUT} offset = 3.3V, V_{CC} offset = 4.3V

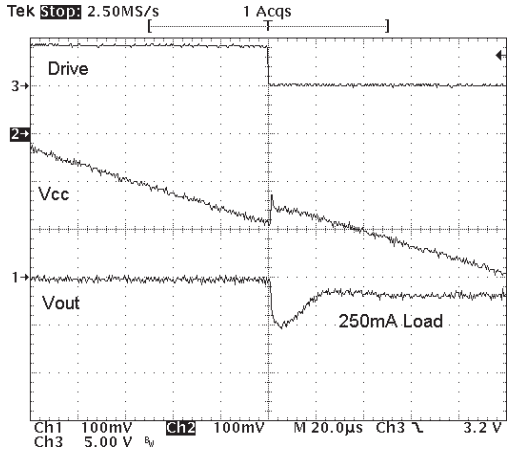


Figure 8. V_{CC} Power-down (V_{AUX} = 3.3V).

Typical Transient Characteristics (continued)

V_{CC} Power-down (V_{AUX} = 3.3V) (continued). The output voltage experiences a disturbance of approximately 100mV during the transient. Some of this disturbance is attributed to the response at V_{AUX} input pin.

V_{CC} Power-down (V_{AUX} = 0V). Figure 9 shows the output response of the regulator during a complete power-down situation under full load conditions.

Regulation on the output is fully maintained until V_{CC} falls below the deselect voltage.

When V_{CC} eventually collapses below an acceptable logic supply level (2V), a disturbance on the Drive pin can be observed.

V_{CC} offset = 5.0V

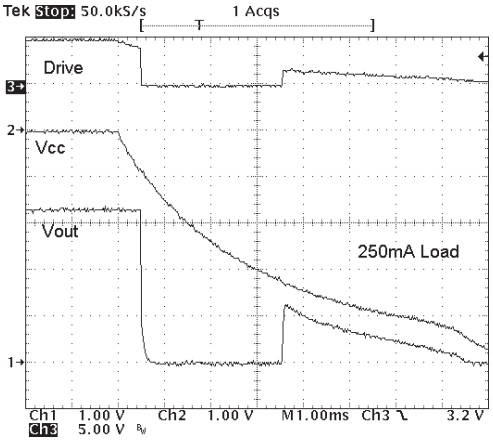


Figure 9. V_{CC} Power-down (V_{AUX} = 0V).

Load Step Response. Figure 10 shows the output response of the regulator during a step load change from 5mA to 250mA.

During the application and removal of the step load minimal overshoot is observed and transient has settled within 10µs.

The dc voltage change on the output is approximately 40mV, which demonstrates the regulator output impedance of 0.15Ω.

V_{OUT} offset = 3.3V

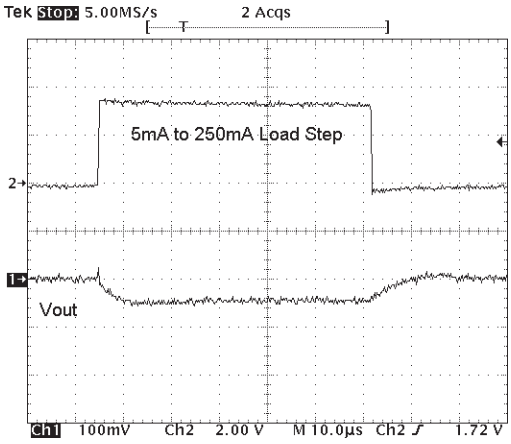


Figure 10. Load Step Response.

Line Step Response. Figure 11 shows the regulator output response to a step transient (1Vpp) on the V_{CC} input. The load condition applied is 5mA.

A disturbance of less than 30mV is observed on the output during the transient.

V_{OUT} offset = 3.3V

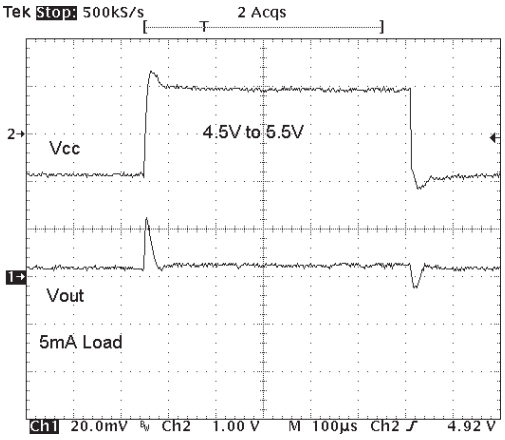


Figure 11. Line Step Response.

Typical Thermal Characteristics (continued)

Thermal dissipation of junction heat consists primarily of two paths in series. The first path is the junction to the case (θ_{JC}) thermal resistance, which is defined by the package style, and the second path is the case to ambient (θ_{CA}) thermal resistance, which is dependent on board layout and construction.

For a given package style and board layout, the operating junction temperature is a function of junction power dissipation P_{JUNC} and the ambient temperature, resulting in the following thermal equation:

$$T_{JUNC} = T_{AMB} + P_{JUNC}(\theta_{JC}) + P_{JUNC}(\theta_{CA})$$

The 8-pin SOIC Narrow style package has θ_{JC} of 60°C/W. When mounted on a printed circuit board with a heat-spreading ability equivalent to 2 square inches of copper, the resulting θ_{CA} is approximately 40°C/W.

Based on maximum power dissipation of 0.5W (2Vx250mA) with an ambient of 70°C, the resulting junction temperature will be:

$$\begin{aligned} T_{JUNC} &= T_{AMB} + P_{JUNC}(\theta_{JC}) + P_{JUNC}(\theta_{CA}) \\ &= 70°C + 0.5W\ (60°C/W) + 0.5W\ (40°C/W) \\ &= 70°C + 30°C + 20°C \\ &= 120°C \end{aligned}$$

The CMPWR120 can therefore be operated at full rated load conditions when provided with a case to ambient thermal resistance of 40°C/W. Most multilayer boards using power plane construction will readily provide this acceptable thermal environment.

Measurements showing performance up to maximum junction temperature of 125°C were performed under light load conditions (5mA). This allows the ambient temperature to be representative of the internal junction temperature.

Output Voltage vs. Temperature. Figure 12 shows the regulator V_{OUT} performance up to the maximum rated junction temperature. The overall 100°C variation in junction temperature causes an output voltage change of about 30mV, reflecting a voltage temperature coefficient of 90ppm/°C.

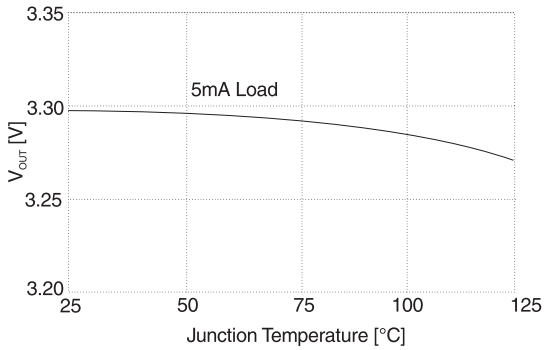


Figure 12. Output Voltage vs. Temperature.

Thresholds vs. Temperature. Figure 13 shows the regulator select/deselect threshold variation up to the maximum rated junction temperature. The overall 100°C change in junction temperature causes a 30mV variation in the select threshold voltage (regulator enable). The deselect threshold level varies about 50mV over the 100°C change in junction temperature. This results in the built-in hysteresis having minimal variation over the entire operating junction temperature range.

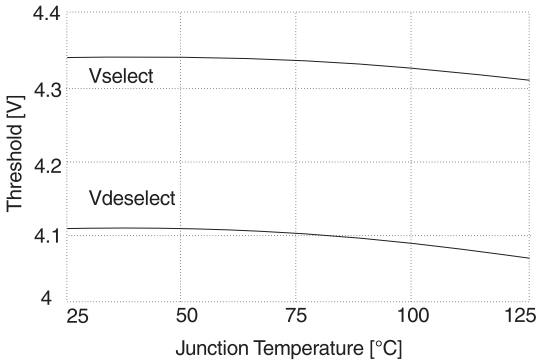


Figure 13. Threshold vs. Temperature.