80C521/80C321/80C541

CMOS Single-Chip Microcontroller

FINAL

DISTINCTIVE CHARACTERISTICS

- Software and pin-compatible with 80C51
- Dedicated Watchdog Timer
  - — Robust: immune to software disables
  - — Flexible: user programmable from 128 microseconds to 4 seconds at 12 MHz
- Dual Data Pointers
  - — Faster external memory access
- Software Reset

	RAM (bytes)	ROM (bytes)
80C321	256	—
80C521	256	8K
80C541	256	16K

80C521 = 80C321 + 8K bytes ROM
80C541 = 80C321 + 16K bytes ROM

GENERAL DESCRIPTION

The 80C521 Family (80C521, 80C321, and 80C541) is a fully instruction-set-compatible and pin-compatible enhancement of the industry-standard 80C51 architecture. These products include a programmable Watchdog Timer and Dual Data Pointers to enhance reliability and improve performance.

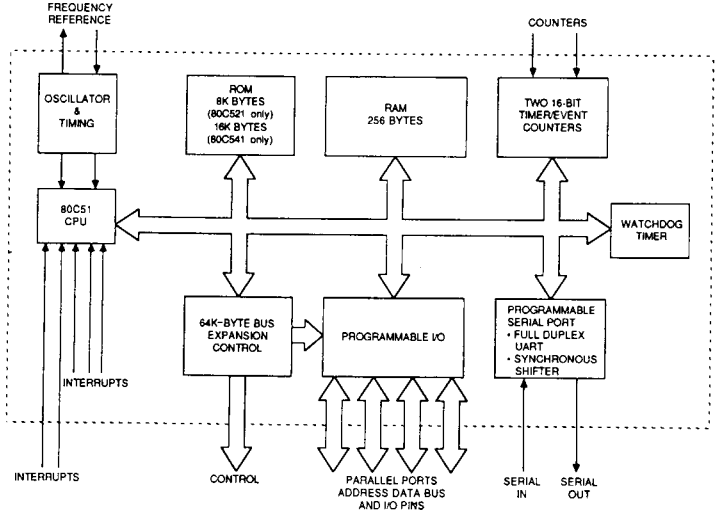
The 80C521, 80C321, and 80C541 include 256 bytes of RAM. The 80C521 has 8K bytes of on-chip custom ROM, the 80C541 has 16K bytes of ROM, and the 80C321 has no on-chip ROM.

A dedicated Watchdog Timer was added to provide enhanced system reliability by increasing tolerance to noise, ESD, and software failures. This robust timing circuit has special software and electrical isolation features. For example, it cannot be disabled by potentially corrupted software. It is user programmable from 128 microseconds to 4 seconds at 12 MHz.

The Dual Data Pointers structure speeds access to external memory by providing two identical 16-bit data pointers with a fast switching mechanism. This overcomes a traditional 8051 limitation of only a single data pointer and can improve performance of tasks such as block transfers by over 100%. For more information consult the Software Routines section in this chapter.

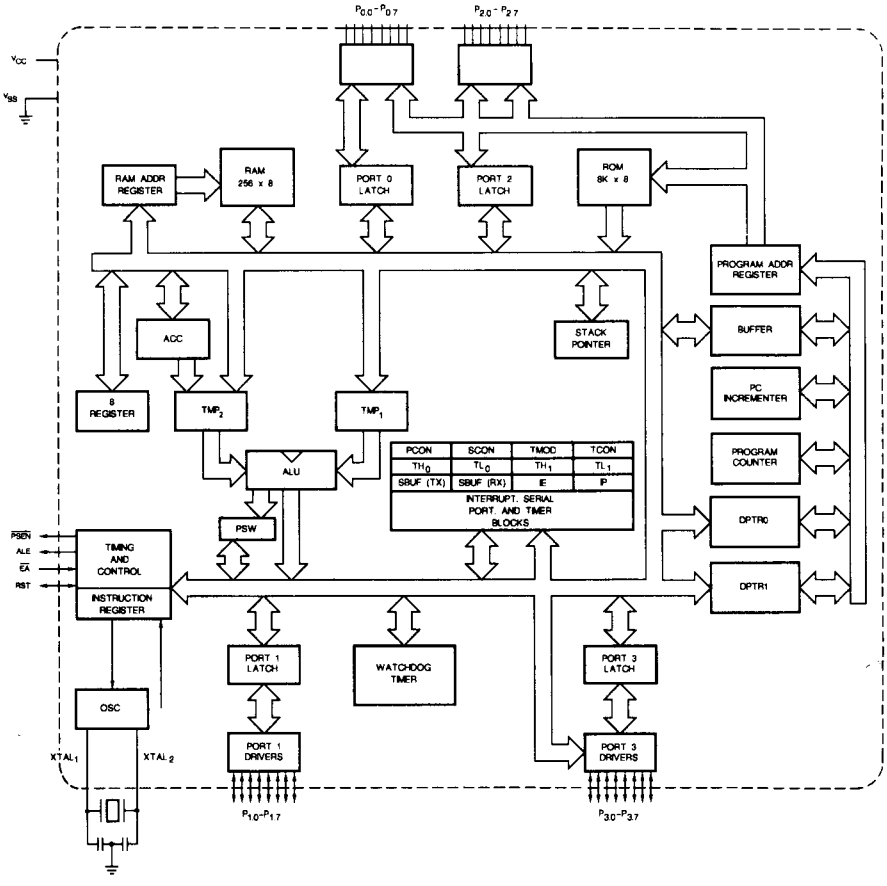
The 80C521 Family is offered in 40-pin plastic DIP and 44-pin PLCC packages. As with the 80C52T2/80C32T2, the PLCC package contains three additional supply connections (pins 1, 23, and 44) that greatly improve noise tolerance over packages with a single V_{CC} and V_{SS} connection.

SIMPLIFIED BLOCK DIAGRAM



BD007216

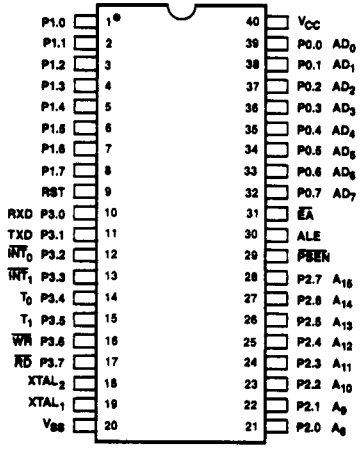
DETAILED BLOCK DIAGRAM



BD004097

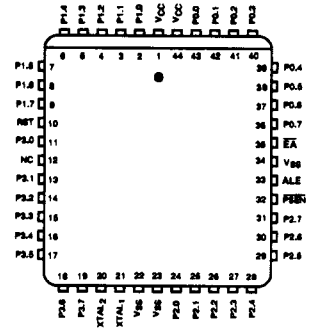
CONNECTION DIAGRAMS
Top View

DIPs



CD005554

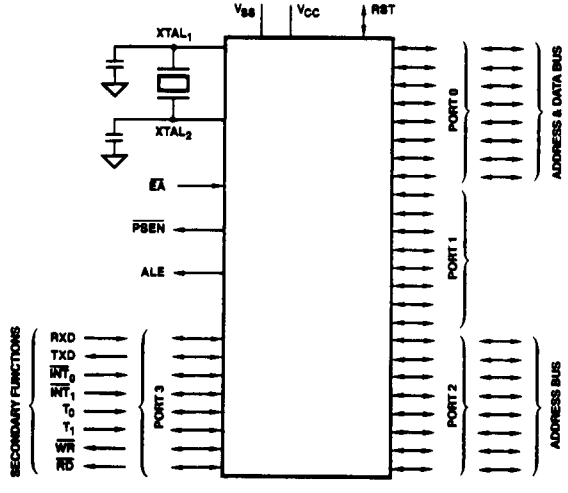
PLCC



CD009444

Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

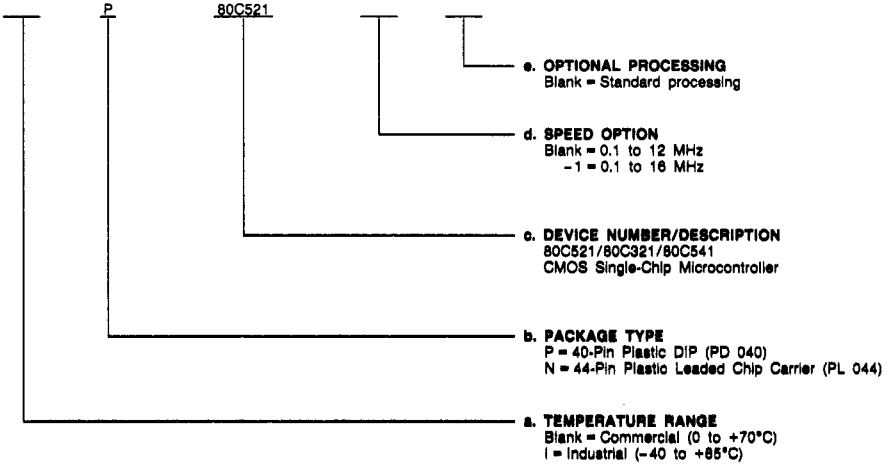


LS001324

ORDERING INFORMATION

Commodity Products

AMD commodity products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:
a. Temperature Range
b. Package Type
c. Device Number
d. Speed Option
e. Optional Processing



Valid Combinations	
P, N IP, IN	80C521
	80C521-1
	80C321
	80C321-1
	80C541
	80C541-1

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released valid combinations, and to obtain additional data on AMD's standard military grade products.

PIN DESCRIPTION

Port 0 (Bidirectional, Open Drain)

Port 0 is an open-drain bidirectional I/O port. Port 0 pins that have 1s written to them float, and in that state can be used as high-impedance inputs.

Port 0 is also the multiplexed Low-order address and data bus during accesses to external Program and Data Memory. In this application it uses strong internal pullups when emitting 1s. Port 0 also outputs the code bytes during program verification in the 80C521. External pullups are required during program verification.

Port 1 (Bidirectional)

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four LSTTL inputs. Port 1 pins that have 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 1 pins that are externally being pulled Low will source current (I_{IL} on the data sheet) because of the internal pullups.

Port 1 also receives the Low-order address bytes during program verification.

Port 2 (Bidirectional)

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four LSTTL inputs. Port 2 pins having 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 2 pins externally being pulled Low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the High-order address byte during fetches from external Program Memory and during accesses to external Data Memory that use 16-bit addresses (MOVX @DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @Ri), Port 2 emits the contents of the P2 Special Function Register. Port 2 also receives the High-order address bits during ROM verification.

Port 3 (Bidirectional)

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four LSTTL inputs. Port 3 pins that have 1s written to them are pulled High by the internal pullups and can be used as inputs while in this state. As inputs, Port 3 pins externally being pulled Low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features as listed below:

Port Pin	Alternate Function
$P_{3.0}$	RxD (serial input port)
$P_{3.1}$	TxD (serial output port)
$P_{3.2}$	$\overline{INT_0}$ (external interrupt 0)
$P_{3.3}$	$\overline{INT_1}$ (external interrupt 1)
$P_{3.4}$	T_0 (Timer 0 external input)
$P_{3.5}$	T_1 (Timer 1 external input)
$P_{3.6}$	$\overline{WR}$ (external Data Memory write strobe)
$P_{3.7}$	$\overline{RD}$ (external Data Memory read strobe)

RST Reset (Input/Output, Active High)

A High on this pin (for two machine cycles while the oscillator is running) resets the device. An internal diffused resistor to V_{SS} permits power-on reset, using only an external capacitor to V_{CC}.

Immediately prior to a Watchdog Reset or Software Reset, this pin is pulled High for one state time. The internal pull-up can be overdriven by an external driver capable of sinking/sourcing 2.5 mA (see Figure 6 for possible circuit configurations).

ALE Address Latch Enable (Output, Active High)

Address Latch Enable is the output pulse for latching the Low byte of the address during accesses to external memory.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, allowing use for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

$\overline{PSEN}$ Program Store Enable (Output, Active Low)

$\overline{PSEN}$ is the read strobe to external Program Memory. When the 80C521 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external Data Memory. $\overline{PSEN}$ is not activated during fetches from internal Program Memory.

$\overline{EA}$ External Access Enable (Input, Active Low)

$\overline{EA}$ must be externally held Low to enable the device to fetch code from external Program Memory locations 0000H to 1FFFH. If $\overline{EA}$ is held High, the device executes from internal Program Memory unless the program counter contains an address greater than 1FFFH.

The 80C521 internally latches the value of the $\overline{EA}$ pin at the falling edge of the reset pulse on the RST pin during a Hardware or Power-on Reset. Once latched, the $\overline{EA}$ value cannot be changed except by a Hardware reset.

$XTAL_1$ Crystal (Input)

Input to the inverting-oscillator amplifier, and input to the internal clock-generator circuits.

$XTAL_2$ Crystal (Output)

Output from the inverting-oscillator amplifier.

V_{CC} Power Supply

Supply voltage during normal, idle, and power-down operations.

V_{SS} Circuit Ground

FUNCTIONAL DESCRIPTION

Program Memory

The 80C521 has 64K bytes of Program Memory space. The lower 8K bytes (addresses 0000H to 1FFF) may reside on-chip. Instructions residing at addresses beyond 1FFF will always be fetched externally. When the External Access ($\overline{EA}$) pin is held Low, all code-fetch operations take place externally to the 80C521.

Data Memory

The 80C521 can address 64K bytes of Data Memory external to the chip. The MOVX instructions are used to access the external Data Memory.

The internal data memory comprises three physically distinct memory spaces. They are the lower 128 bytes of RAM, the upper 128 bytes of RAM, and the 128-byte Special Function Register (SFR) space. The lower 128 bytes of RAM can be accessed through direct addressing (i.e., MOV addr, data), or indirect addressing (i.e., MOV @ Ri). The upper 128 bytes of RAM (locations 80H through FFH) can be accessed only through indirect addressing modes. The Special Function Register space, while physically distinct from the upper 128 bytes of RAM, shares addresses with the upper 128 bytes of RAM. The SFR space may be accessed through direct addressing modes only.

The first 32 bytes of RAM contain four register banks, each of which contains eight general-purpose registers. The next 16 bytes (locations 20H through 2FH) contain 128 directly addressable bit locations. The stack may be located anywhere in the internal RAM space and may be up to 256 bytes in length.

SPECIAL FUNCTION REGISTER MAP

Addr (HEX)	Symbol	Name	Default After Power-On Reset
* 80	P0	Port 0	11111111
81	SP	Stack Pointer	00000111
82	DPL	Data Pointer Low	00000000
83	DPH	Data Pointer High	00000000
+ 84	DPL1	Data Pointer Low 1	00000000
+ 85	DPH1	Data Pointer High 1	00000000
+ 86	DPS	Data Pointer Selection	00000000
87	PCON	Power Control	0XXX0000
* 88	TCON	Timer/Counter Control	00000000
89	TMOD	Timer/Counter Mode Control	00000000
8A	TL0	Timer/Counter 0 Low Byte	00000000
8B	TL1	Timer/Counter 1 Low Byte	00000000
8C	TH0	Timer/Counter 0 High Byte	00000000
8D	TH1	Timer/Counter 1 High Byte	00000000
* 90	P1	Port 1	11111111
* 98	SCON	Serial Control	00000000
99	SBUF	Serial Data Buffer	Indeterminate
* A0	P2	Port 2	11111111
* A8	IE	Interrupt Enable Control	0XX00000
+ A9	WDS	Watchdog Selection	00000000
+ AA	WDK	Watchdog Key	00000000
* B0	P3	Port 3	11111111
* B8	IP	Interrupt Priority Control	XXX00000
* D0	PSW	Program Status Word	00000000
* E0	ACC	Accumulator	00000000
* F0	B	B Register	00000000

* Bit Addressable

\+ New SFRs defined on the 80C521/80C321

Basic Timing Definitions

Instructions in the 8051 family execute in either one, two, or four machine cycles. A machine cycle comprises six state times with each state made up of two clock cycles; thus, a machine cycle lasts 12 clock cycles. With an external oscillator running at 12 MHz, a machine cycle lasts 1 μs. At 16 MHz, a machine cycle lasts 750 ns.

Reset Operation

The 80C521/80C321 may be reset by four different methods: (1) Power-On Reset, (2) Hardware Reset, (3) Watchdog Reset, and (4) Software Reset.

1. **Power-On Reset** occurs when the RST pin is wired to V_{CC} using an external capacitor, and V_{CC} is activated.

2. **Hardware Reset** occurs when the oscillator is running and the RST pin is held High for two or more machine cycles.

3. **Watchdog Reset** occurs when the count value of the Watchdog Timer is allowed to exceed the programmed value, resulting in an overflow signal that resets the chip in two machine cycles.

4. **Software Reset** occurs when the software writes a keyed sequence to the key register of the Watchdog Timer. This causes a Watchdog Reset to be immediately generated.

After Power-On Reset, the SFRs have the values indicated in the Special Function Register Map Section, and the contents of the internal RAM are undefined. Hardware Reset is the same as Power-On Reset except that the contents of the internal RAM are preserved. A Hardware Reset has priority over a Watchdog Reset or a Software Reset. The Watchdog Reset puts the 80C521 into the same state as the Hardware Reset except that the Reset Cause (RC) bit in the Watchdog Selection (WDS) register is set to a 1. The Software Reset is functionally equivalent to the Watchdog Reset.

Watchdog Timer

The Watchdog Timer (WDT) is a specially designed timer unit that will reset the chip upon reaching a pre-programmed time interval. It operates independently of the two general purpose timer/counters and is dedicated specifically to the watchdog function. The Watchdog Timer allows safe recovery from problems resulting from unexpected input conditions, external events, or programming anomalies.

The WDT is disabled following any reset. While disabled, the WDT time interval may be programmed. The WDT is enabled by a sequence of two write operations.

Once enabled, the WDT cannot be stopped (i.e., disabled) except by one of the four Reset types described in the last section. Furthermore, while the WDT is enabled, the WDT time interval cannot be modified. The WDT, however, may be cleared by software at any time with the same sequence of two write operations. The clearing operation causes the present count of the WDT to be set to zero, but it does not stop the WDT from incrementing.

If the count in the WDT ever reaches the pre-programmed value, the WDT will overflow, resetting the chip in two machine cycles. This is a Watchdog Reset. Additionally, if a system error condition is discovered, software may intentionally generate an immediate reset via the WDT, using a special sequence of write operations. This is a Software Reset.

A Watchdog Reset or Software Reset will set a special "cause" bit, allowing differentiation between these two Reset types and the Hardware or Power-On Reset types. Neither Watchdog Reset nor the Software Reset modify the contents of the internal RAM. The Watchdog Reset will cause the RST pin to be pulled High during S2P1 and S2P2 of the first cycle of the two-cycle reset, providing a hardware indication that a reset is imminent.

Two 8-bit Special Function Registers are associated with the WDT. They are as follows:

Watchdog Selection (WDS) — Address: A9 (Hex)

Watchdog Key (WDK) — Address: AA (Hex)

Watchdog Selection (WDS) — Address: A9H

The Watchdog Selection register allows the time interval of the WDT to be programmed and retains the cause of the most recent reset. This register is Read/Write, but its contents cannot be changed once the WDT has been enabled. Its default value after a Hardware or Power-On Reset = 00H. Its default value after a Watchdog Reset or Software Reset = 80H. This is the only register on the 80C521 whose initialization value differs between the two reset groups.

(MSB)							(LSB)
RC	-	TV	-	PT3	PT2	PT1	PT0
7	6	5	4	3	2	1	0

Bits 3 - 0 — Programmed Time (PT3 - PT0)

The value contained in these bits at the time the Watchdog Timer is enabled determines the time interval of the WDT. The time interval is a multiple of the input clock period. The times are decoded in the following table.

Programmable Watchdog Timing Intervals

PT3-PT0	12 MHz	16 MHz	Clock Divide Ratio
0 0000	128 μs	96 μs	1536
1 0001	256 μs	192 μs	3072
2 0010	512 μs	384 μs	6144
3 0011	1.024 ms	768 μs	12288
4 0100	2.048 ms	1.536 ms	24576
5 0101	4.096 ms	3.072 ms	49152
6 0110	8.192 ms	6.144 ms	98304
7 0111	16.384 ms	12.288 ms	196608
8 1000	32.768 ms	24.576 ms	393216
9 1001	65.536 ms	49.152 ms	786432
A 1010	131.072 ms	98.304 ms	1572864
B 1011	262.144 ms	196.608 ms	3145728
C 1100	524.288 ms	393.216 ms	6291456
D 1101	1.049 sec	786.432 ms	12582912
E 1110	2.097 sec	1.573 sec	25165824
F 1111	4.194 sec	3.146 sec	50331648

If the Programmed Time bits are read while the WDT is disabled, they will show the last value written. Once the WDT is enabled, these bits will show the programmed time of the WDT and cannot be modified.

Bit 4

Reserved. Will return an unidentified value when read.

Bit 5 — Timer Verification (TV)

This bit reflects Bit 11 of the internal counter within the Watchdog Timer. It will toggle every 4.096 ms at 12 MHz. This bit is Read-only.

Bit 6

Reserved. Will return an unidentified value when read.

Bit 7 — Reset Cause (RC)

The Reset Cause bit indicates the cause of the last reset of the 80C521. If a Power-On or Hardware Reset occurs, the bit is set to a 0 by the reset circuitry. If a Watchdog or Software Reset occurs, the bit is set to a 1 by the reset circuitry. Like the Programmed Time bits, this bit may not be modified once the WDT is enabled. Writing this bit does not affect any chip function.

Watchdog Key (WDK) — Address: AAH

This register controls the enabling and clearing of the Watchdog Timer. The writing of an A5H followed by the writing of a 5AH to this register enables the WDT to begin incrementing. It is not a requirement that the writes be on consecutive instructions, thus interrupts do not have to be disabled. Once the WDT is enabled, it may be cleared at any time by the writing of the same sequence. The clearing operation causes the present count of the WDT to be cleared, but does not stop the WDT from incrementing.

This is a Write-only register. Read operations are not defined and will not affect the WDT circuitry.

(MSB)							(LSB)
7	6	5	4	3	2	1	0

The enabling/clearing operation of the Watchdog Timer is accomplished by writing a keyed sequence of values to the WDK register. The Keyed Sequence is composed of two stages (see Figure 1).

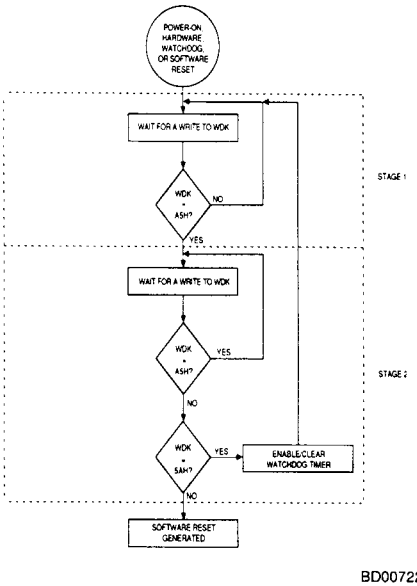


Figure 1. WDT Keyed Sequence Flowchart

The Keyed Sequence is in Stage 1 after all forms of reset, or following any Watchdog enable or clear operation. In Stage 1 all values written to the WDK register are ignored except A5H. An A5H causes the Keyed Sequence to enter Stage 2.

Once Stage 2 is entered, the next write to the WDK register prompts one of the following actions: (1) If the next write is again an A5H, the Keyed Sequence remains in Stage 2; (2) If the next write is a 5AH, the WDT is enabled/cleared, and the Keyed Sequence reenters Stage 1; or, (3) If the next write is any other value, a Software Reset via the WDT is generated.

Example of Write Operations to WDK:

Write 1st	Write 2nd	Action Taken After Second Write
11	18	No action taken, Keyed Sequence still in Stage 1
A5	A5	Keyed Sequence enters Stage 2 and remains there
A5	5A	WDT is enabled/cleared, Sequence reenters Stage 1
A5	11	Software Reset occurs via the WDT

The two-stage feature, together with the Software Reset, greatly reduces the chance of an instruction sequence accidentally clearing the Watchdog Timer. Furthermore, while still allowing a Software Reset to be initiated, the two-stage feature reduces the chance of unintentionally generating a Software Reset.

Software Reset

A Software Reset may be accomplished through the Watchdog Timer. If an A5H is written to the Watchdog Key (WDK) register, followed by the write of a value other than A5H or 5AH, a Software Reset will be generated. This software-generated Watchdog Reset occurs regardless of whether or not the Watchdog Timer was previously enabled.

After the second value is written to the WDK register, program execution continues for one machine cycle before the reset operation begins. During S2P1 and S2P2 of this last machine cycle, the RST pin is pulled High (see Figure 6). The reset operation lasts two machine cycles and does not modify the contents of the internal RAM.

The Software Reset is functionally equivalent to the Watchdog Reset. For instance, the Reset Cause bit in WDS will be set to 1, indicating a Watchdog Reset occurred (see the Watchdog Timer section for more details).

The following code may be used to generate a Software Reset.

```
MOV WDK,#A5H ; Write A5 (Hex) to WDK
MOV WDK,#11H ; Write 11 (Hex) to WDK
               Software Reset generated via WDT
```

Dual Data Pointers

The Dual Data Pointer structure is the means by which the 80C521 family may specify the address of an external Data Memory location. The Dual Data Pointer structure consists of two 16-bit registers that address external memory, and a single 8-bit register that allows the program code to selectively switch between them. They are located in the Special Function Register space at the following addresses:

82H Data Pointer Low	–(DPL)	Data Pointer 0 (DPTR0)
83H Data Pointer High	–(DPH)	
84H Data Pointer Low 1	–(DPL1)	Data Pointer 1 (DPTR1)
85H Data Pointer High 1	–(DPH1)	
86H Data Pointer Selection	–(DPS)	

Data Pointer 0 (DPTR0) is the original data pointer on the standard 80C51 (formerly referred to as DPTR). Data Pointer 1 (DPTR1) is an additional data pointer with identical characteristics. Instructions that refer to DPTR refer to the data pointer that is currently selected in the Data Pointer Selection (DPS) register. The six instructions that reference DPTR are as follows:

INC DPTR	;Increments the data pointer by 1
MOV DPTR, #data16	;Loads DPTR with a 16-bit constant
MOVC A, @A + DPTR	;Move code byte relative to DPTR to Acc
MOVX A, @DPTR	;Move external RAM (16-bit address) to Acc
MOVX @DPTR, A	;Move Acc to external RAM (16-bit address)
JMP @A + DPTR	;Jump indirect relative to DPTR

It is also possible to access each data pointer on a byte-by-byte basis by specifying its low or high byte in an instruction that accesses the Special Function Registers. These instructions can be executed at any time regardless of which of the two data pointers is currently selected. Three examples are as follows:

MOV DPH,R3	;Move the contents of Register 3 into DPH
MOV A,DPL1	;Move the contents of DPL1 into the Acc
PUSH DPH1	;Push the contents of DPH1 onto the stack

The Dual Data Pointer structure saves both time and code space by eliminating the need for frequent loading and unloading of a single data pointer. For instance, block move operations in external memory can be more efficiently implemented by using DPTR0 as the source address, and DPTR1 as the destination address. The Dual Data Pointer structure enhances this operation considerably.

Data Pointer Selection (DPS) — Address: 86H

This register determines which of the two data pointers is currently selected. Once a data pointer is selected, the six DPTR instructions refer only and always to that data pointer until another data pointer is selected. Upon reset, the default data pointer (DPTR0) will be selected, thus retaining compatibility with existing 8051-family devices. The switch between data pointers may be accomplished with a single cycle instruction (such as: INC DPS or MOV DPS,A). The default value at reset = 00H. This is a Read/Write register.

(MSB)							(LSB)
0	0	0	0	0	0	0	SEL0
7	6	5	4	3	2	1	0

Bit 0 — Select 0 (SEL0)

If this bit is 0, the original data pointer, DPTR0, is selected. If this bit is 1, DPTR1 is selected. This bit may be written by software at any time. When read, its current value is presented.

Bits 7 – 1

Reserved. Will return 0 when read.

Data Pointer Low (DPL) — Address: 82H

DPL is a Read/Write register that contains the low byte of Data Pointer 0. It may be accessed at any time with an instruction that specifies a direct byte as a source of destination. However, SEL0 in the DPS register must be set to 0 before any of the six explicit DPTR instructions will access this register. The default at reset = 00H.

(MSB)							(LSB)
7	6	5	4	3	2	1	0

Data Pointer High (DPH) — Address: 83H

DPH is a Read/Write register that contains the high byte of Data Pointer 0. It may be accessed at any time with an instruction that specifies a direct byte as a source or destination. However, SEL0 in the DPS register must be set to 0 before any of the six explicit DPTR instructions will access this register. The default at reset = 00H.

(MSB)							(LSB)
7	6	5	4	3	2	1	0

Data Pointer Low 1 (DPL1) — Address: 84H

DPL1 is a Read/Write register that contains the low byte of Data Pointer 1. It may be accessed at any time with an instruction that specifies a direct byte as a source or destination. However, SEL0 in the DPS register must be set to 1 before any of the six explicit DPTR instructions will access this register. The default at reset = 00H.

(MSB)							(LSB)
7	6	5	4	3	2	1	0

Data Pointer High 1 (DPH1) — Address: 85H

DPH1 is a Read/Write register that contains the high byte of Data Pointer 1. It may be accessed at any time with an instruction that specifies a direct byte as a source or destination. However, SEL0 in the DPS register must be set to 1 before any of the six explicit DPTR instructions will access this register. The default at reset = 00H.

(MSB)							(LSB)
7	6	5	4	3	2	1	0

Dual Data Pointer Example

To load both data pointers after reset:

Method 1:

```
MOV DPL ,#data8      ;load low byte of DPTR0
MOV DPH ,#data8      ;load high byte of DPTR0
MOV DPL1,#data8      ;load low byte of DPTR1
MOV DPH1,#data8      ;load high byte of DPTR1
```

(Data Pointer 0 is still selected.)

Method 2:

```
MOV DPTR,#data16     ;load DPTR0 with 16-bit const.
INC DPS              ;switch data pointers
MOV DPTR,#data16     ;load DPTR1 with 16-bit const.
```

(Data Pointer 1 is now selected.)

Oscillator Characteristics

$XTAL_1$ and $XTAL_2$ are the input and output, respectively, of an inverting amplifier which is configured for use as an on-chip oscillator (see Figure 2). Either a quartz crystal or ceramic resonator may be used.

To drive the device from an external clock source, $XTAL_1$ should be driven while $XTAL_2$ is left unconnected (see Figure 3). There are no requirements on the duty cycle of the external clock signal since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum High and Low times specified on the data sheet must be observed.

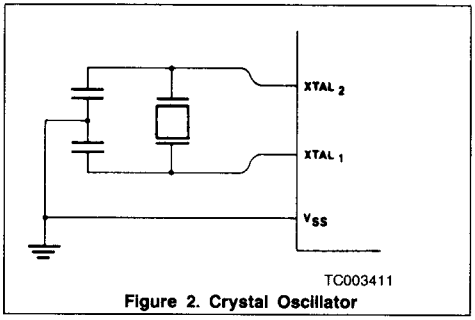
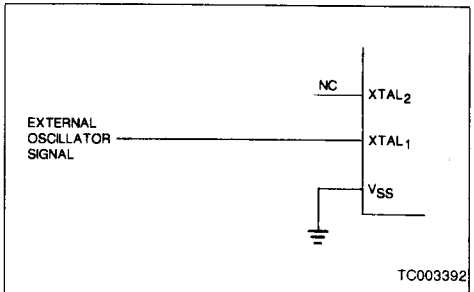


Figure 2. Crystal Oscillator



Note: Different from NMOS 8051

Figure 3. External Drive Configuration

Idle and Power-Down Operation

Figure 4 shows the internal operation of the Idle and Power-Down circuitry. Power-Down operation disconnects the clock source from all internal chip circuitry. Idle mode operation allows the interrupt, serial port, timers, and watchdog circuitry to continue to function while the CPU is stopped. If the Watchdog Timer is enabled, Power-Down operation is not possible.

These special modes are activated by software via the Special Function Register, PCON (Table 1). Its hardware address is 87H; PCON is not bit-addressable.

If 1s are written to PD and IDL at the same time, PD takes precedence. The reset value of PCON is 0XXX0000.

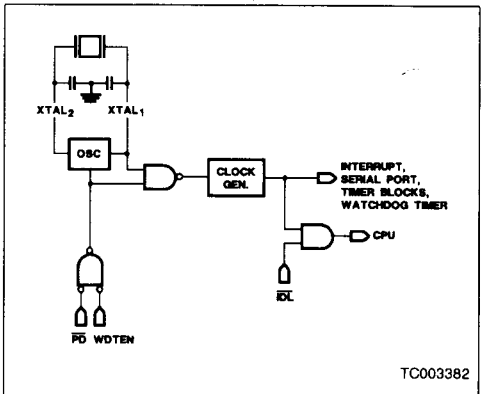


Figure 4. Idle and Power-Down Hardware

TABLE 1. PCON (Power Control Register)

(MSB)							(LSB)
SMOD	-	-	-	GF1	GF0	PD	IDL

Symbol	Position	Name and Description
SMOD	PCON.7	Double-baud-rate bit. When set to a 1, the baud rate is doubled when the serial port is being used in either modes 1, 2, or 3.
-	PCON.6	(Reserved)
-	PCON.5	(Reserved)
-	PCON.4	(Reserved)
GF1	PCON.3	General-purpose flag bit
GF0	PCON.2	General-purpose flag bit
PD	PCON.1	Power-Down bit. Setting this bit activates power-down operation.
IDL	PCON.0	Idle-mode bit. Setting this bit activates idle-mode operation.

Idle Mode

The instruction that sets PCON.0 is the last instruction executed in the normal operating mode before the Idle mode is activated. Once in the Idle mode, the CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator, RAM, and all other registers in the 80C521 maintain their data during Idle. Table 2 describes the status of the external pins during Idle mode.

There are three possible ways to terminate the Idle mode. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt is serviced, and following RETI, the next instruction to be executed will be the one following the instruction that wrote a 1 to PCON.0.

The flag bits GF0 and GF1 may be used to determine whether the interrupt was received during normal execution or during the idle mode. For example, the instruction that writes to PCON.0 can also set or clear one or both flag bits. When Idle mode is terminated by an enabled interrupt, the service routine can examine the status of the flag bits.

The second way of terminating the Idle mode is with a Hardware Reset.

The third way of terminating the Idle mode is with the Watchdog Timer. If the WDT is not enabled, then it has no effect on subsequent Idle mode operations. If the WDT is enabled before Idle mode is entered, it will continue to increment in the normal fashion. If the WDT overflows, the 80C521 will experience a Watchdog Reset and Idle mode will be terminated. If Idle mode is terminated by any method other than a reset, the Watchdog Timer will continue to run.

Power-Down Mode

The instruction that sets PCON.1 is the last executed prior to going into Power-Down. Once in Power-Down, the oscillator is stopped. The contents of the on-chip RAM are preserved. The Special Function Registers are saved until a Hardware Reset is generated. A hardware reset is the only way of exiting the Power-Down mode.

Power-Down mode cannot be entered while the Watchdog Timer is enabled. If a write of the value 1 is attempted into the PD bit of the PCON register, its value will remain 0, and no Power-Down operation will take place. To enter Power-Down mode, the Watchdog Timer must first be disabled via a Hardware Reset, Software Reset, or Watchdog Reset. After reset, the Watchdog Timer is disabled, allowing Power-Down mode to be entered.

In the Power-Down mode, V_{CC} may be lowered to minimize circuit power consumption. Care must be taken to ensure the voltage is not reduced until the Power-Down mode is entered, and that the voltage is restored before the Hardware Reset is applied. Hardware Reset frees the oscillator and should not be released until the oscillator has restarted and stabilized.

Table 2 describes the status of the external pins while in the Power-Down mode. It should be noted that if the Power-Down mode is activated while in external program memory, the port data that is held in the Special Function Register P_2 is restored to Port 2. If the data is a 1, the port pin is held High during the Power-Down mode by the strong pullup, P_1, shown in Figure 5.

80C521 I/O Ports

The I/O port drive of the 80C521 is similar to the 8051. The I/O buffers for Ports 1, 2, and 3 are implemented as shown in Figure 5.

When the port latch contains a 0, all pFETS in Figure 5 are off while the nFET is turned on. When the port latch makes a 0-to-1 transition, the nFET turns off. The strong pullup pFET, P_1, turns on for two oscillator periods, pulling the output High very rapidly. As the output line is drawn High, pFET P_3 turns on through the inverter to supply the I_{OH} source current. This inverter and P_3 form a latch that holds the 1 and is supported by P_2.

When Port 2 is used as an address port, for access to external program or data memory, any address bit that contains a 1 will have its strong pullup turned on for the entire duration of the external memory access.

When an I/O pin on Ports 1, 2, or 3 is used as an input, the user should be aware that the external circuit must sink current during the logical 1-to-0 transition. The maximum sink current is specified as I_{TL} under the D.C. specifications. When the input goes below approximately 2 V, P_3 turns off to save I_{CC} current. Note, when returning to a logical 1, P_2 is the only internal pullup that is on. This will result in a slow rise time if the user's circuit does not force the input line High.

TABLE 2. STATUS OF THE EXTERNAL PINS DURING IDLE AND POWER-DOWN MODES

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power-Down	Internal	0	0	Port Data	Port Data	Port Data	Port Data
Power-Down	External	0	0	Floating	Port Data	Port Data	Port Data

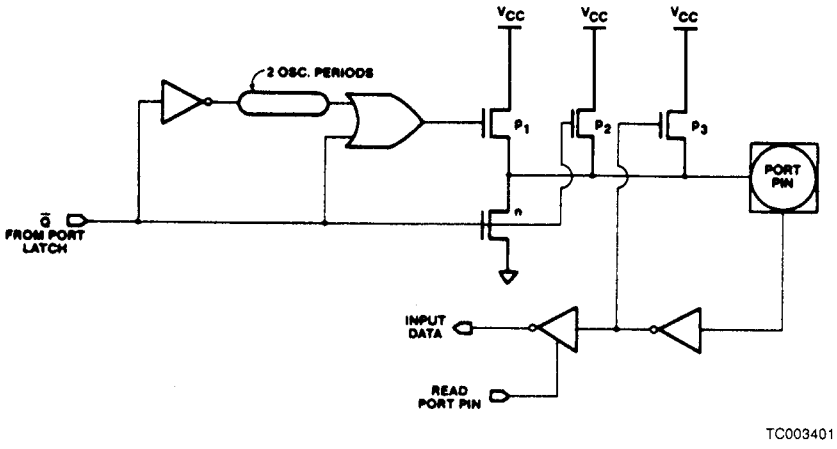
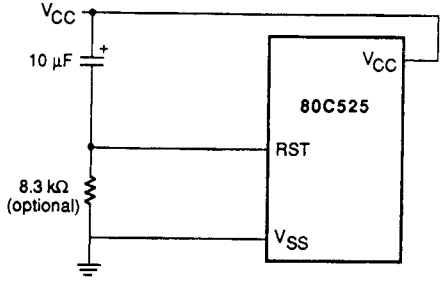
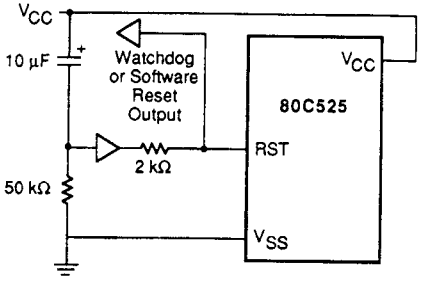


Figure 5. I/O Buffers in the 80C521 (Ports 1, 2, 3)





TC004320

Standard (80C51) Reset Circuit

Neither a Watchdog nor a Software Reset will affect the Standard reset circuitry, nor can they be sensed by the Standard (80C51) reset circuitry.

Watchdog Reset Circuit

The reset circuit shown above may be used to sense a Watchdog or Software Reset. For $V_{CC} = 5$ V, the driver output must be able to source/sink 2.5 mA.

Figure 6. RESET Configurations

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Voltage on Any
Pin to V_{SS} ..... −0.5 V to V_{CC} +0.5 V
Voltage on V_{CC} to V_{SS} ..... −0.5 V to 6.5 V
Power Dissipation .....200 mW

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature (T_A)..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Ground (V_{SS}).....0 V

Industrial (I) Devices
Temperature (T_A).....−40 to +85°C
Supply Voltage (V_{CC}) ..... +4.5 V to +5.5 V
Ground (V_{SS}).....0 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage (Except $\overline{EA}$)		−0.5	0.2 V_{CC} − 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		−0.5	0.2 V_{CC} − 0.3	V
V_{IH}	Input High Voltage (Except $XTAL_1$, RST)		0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage ($XTAL_1$ RST)		0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage (Ports 1, 2, 3)	I_{OL} = 1.6 mA (Note 1)		0.45	V
V_{OL1}	Output Low Voltage (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA (Note 1)		0.45	V
V_{OH}	Output High Voltage (Ports 1, 2, 3)	I_{OH} = −60 μA, V_{CC} = 5 V±10%	2.4		V
		I_{OH} = −25 μA	0.75 V_{CC}		V
		I_{OH} = −10 μA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode, ALE $\overline{PSEN}$)	I_{OH} = −800 μA, V_{CC} = 5 V±10%	2.4		V
		I_{OH} = −300 μA	0.75 V_{CC}		V
		I_{OH} = −80 μA (Note 2)	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)	V_{IN} = 0.45 V		−50	μA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)	V_{IN} = 2 V		−650	μA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	μA
RRST	Reset Pulldown Resistor		50	150	kΩ
CIO	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{PD}	Power-Down Current	V_{CC} = 2 to 6 V (Note 3)		50	μA

MAXIMUM I_{CC} (mA)

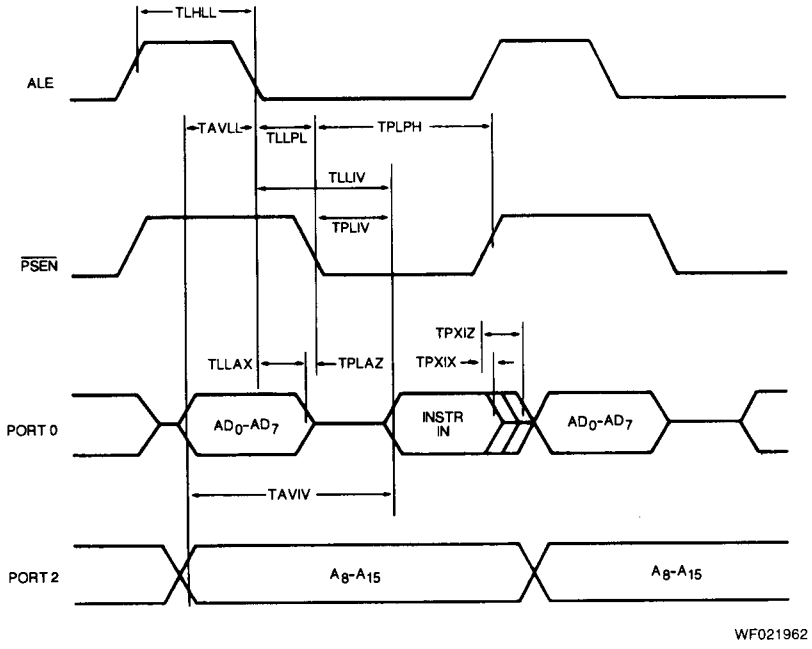
	Operating (Note 4)			Idle (Note 5)		
Freq. V_{CC}	4.5 V	5 V	5.5 V	4.5 V	5 V	5.5 V
0.1 MHz	2.2	3.1	3.8	0.7	0.9	1.4
3.5 MHz	6	8	10	1.5	2	3
8.0 MHz	11	14	18	2.5	3.5	5
12 MHz	15	20	25	3.5	5	6
16 MHz	19	25	32	4.5	6.5	8.5

Notes:
1. Capacitive loading on ports may cause spurious noise pulses to be superimposed on the V_{OL}S of ALE and other ports. The noise is due to external bus capacitance discharging into the port pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8 V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt-Trigger STROBE input. This note pertains to dual-in-line packages only. The additional V_{CC} and V_{SS} connections on the PLCC package from AMD removes this design consideration.
2. Capacitive loading on ports may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing. This note pertains to dual-in-line packages only. The additional V_{CC} and V_{SS} connections on the PLCC package from AMD remove this design consideration.
3. Power-Down I_{CC} is measured with all output pins disconnected: $\overline{EA}$ = Port 0 = V_{CC}; $XTAL_2$ NC; RST = V_{SS}.
4. I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; $XTAL_2$ NC; $\overline{EA}$ = RST = Port 0 = V_{CC}. Typical values are approximately 50% lower. I_{CC} would be slightly higher if a crystal oscillator was used.
5. Idle I_{CC} is measured with all output pins disconnected; $XTAL_1$ driven with TCLCH, TCHCL = 5 ns, V_{IL} = V_{SS} + 0.5 V, V_{IH} = V_{CC} − 0.5 V; $XTAL_2$ NC; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS}, and the Watchdog Timer disabled.

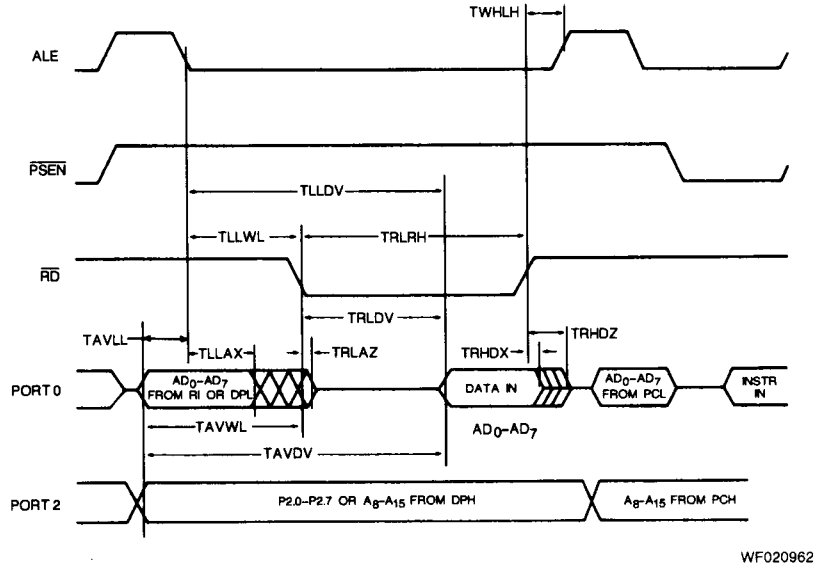
SWITCHING CHARACTERISTICS over operating range (C_L for Port 0, ALE and $\overline{PSEN}$ Outputs = 100 pF; C_L for All Other Outputs = 80 pF)

Parameter Symbol	Parameter Description	16-MHz Osc.		12-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
EXTERNAL PROGRAM AND DATA MEMORY CHARACTERISTICS								
1/TCLCL	Oscillator Frequency					0.1	16	MHz
TLHLL	ALE Pulse Width	85		127		2TCLCL – 40		ns
TAVLL	Address Valid to ALE Low	7		28		TCLCL – 55		ns
TLLAX	Address Hold After ALE Low	27		48		TCLCL – 35		ns
TLLIV	ALE Low to Valid Instr. In		150		234		4TCLCL – 100	ns
TLLPL	ALE Low to $\overline{PSEN}$ Low	22		43		TCLCL – 40		ns
TPLPH	$\overline{PSEN}$ Pulse Width	142		205		3TCLCL – 45		ns
TPLIV	$\overline{PSEN}$ Low to Valid Instr. In		83		145		3TCLCL – 105	ns
TPXIX	Input Instr. Hold After $\overline{PSEN}$	0		0		0		ns
TPXIZ	Input Instr. Float After $\overline{PSEN}$		38		59		TCLCL – 25	ns
TAVIV	Address to Valid Instr. In		208		312		5TCLCL – 105	ns
TPLAZ	$\overline{PSEN}$ Low to Address Float		10		10		10	ns
TRLRH	$\overline{RD}$ Pulse Width	275		400		6TCLCL – 100		ns
TWLWH	$\overline{WR}$ Pulse Width	275		400		6TCLCL – 100		ns
TRLDV	$\overline{RD}$ Low to Valid Data In		148		252		5TCLCL – 165	ns
TRHDX	Data Hold After $\overline{RD}$	0		0		0		ns
TRHDZ	Data Float After $\overline{RD}$		55		97		2TCLCL – 70	ns
TLLDV	ALE Low to Valid Data In		350		517		8TCLCL – 150	ns
TAVDV	Address to Valid Data In		398		585		9TCLCL – 165	ns
TLLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	137	238	200	300	3TCLCL – 50	3TCLCL + 50	ns
TAVWL	Address Valid to Read or Write Low	120		203		4TCLCL – 130		ns
TQVWX	Data Valid to $\overline{WR}$ Transition	2		23		TCLCL – 60		ns
TQVWH	Valid Data to Write High	287		433		7TCLCL –150		ns
TWHQX	Data Hold After $\overline{WR}$	12		33		TCLCL – 50		ns
TRLAZ	$\overline{RD}$ Low to Address Float		0		0		0	ns
TWHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	22	103	43	123	TCLCL – 40	TCLCL + 40	ns

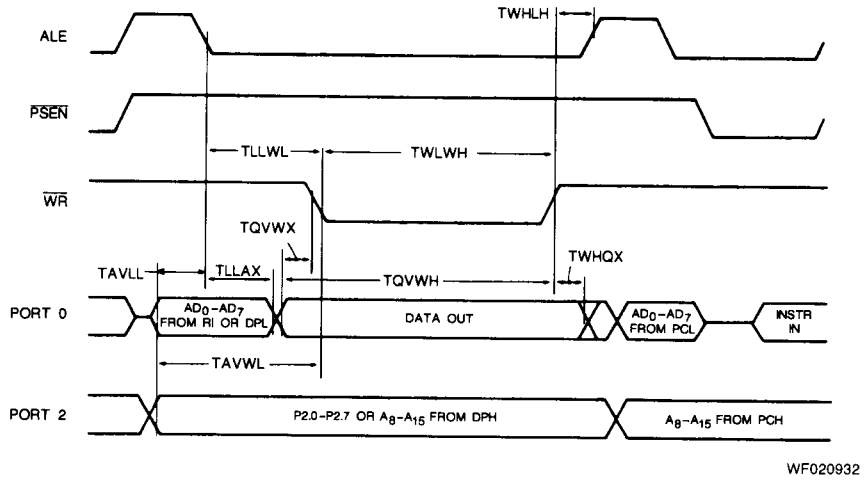
SWITCHING WAVEFORMS



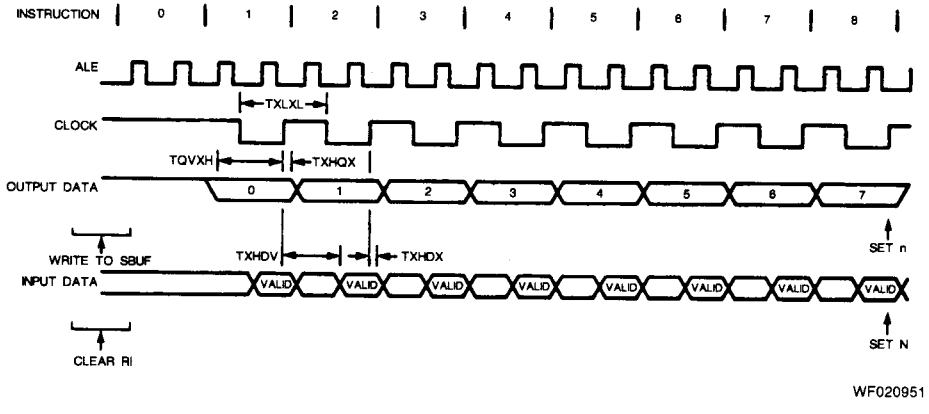
External Program Memory Read Cycle



External Data Memory Read Cycle



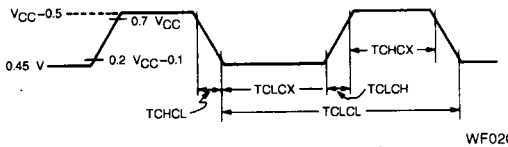
External Data Memory Write Cycle



Shift Register Timing Waveforms

EXTERNAL CLOCK DRIVE

Parameter Symbol	Parameter Description	Min.	Max.	Unit
1/TCLCL	Oscillator Frequency	0.1	16	MHz
TCHCX	High Time	20		ns
TCLCX	Low Time	20		ns
TCLCH	Rise Time		20	ns
TCHCL	Fall Time		20	ns



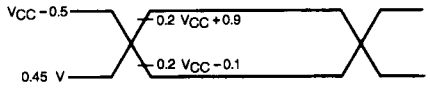
External Clock Drive Waveform

SERIAL PORT TIMING—SHIFT REGISTER MODE

Test Conditions: $T_A = 0°C$ to $70°C$; $V_{CC} = 5$ V ±10%; $V_{SS} = 0$ V; Load Capacitance = 80 pF

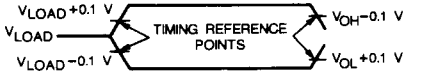
Parameter Symbol	Parameter Description	16-MHz Osc.		Variable Oscillator		Unit
		Min.	Max.	Min.	Max.	
TXLXL	Serial Port Clock Cycle Time	750		12TCLCL		ns
TQVXH	Output Data Setup to Clock Rising Edge	492		10TCLCL – 133		ns
TXHQX	Output Data Hold After Clock Rising Edge	8		2TCLCL – 117		ns
TXHDX	Input Data Hold After Clock Rising Edge	0		0		ns
TXHDV	Clock Rising Edge to Input Data Valid		492		10TCLCL – 133	ns

AC Testing



AC inputs during testing are driven at $V_{CC} - 0.5$ for a logic 1and 0.45 V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

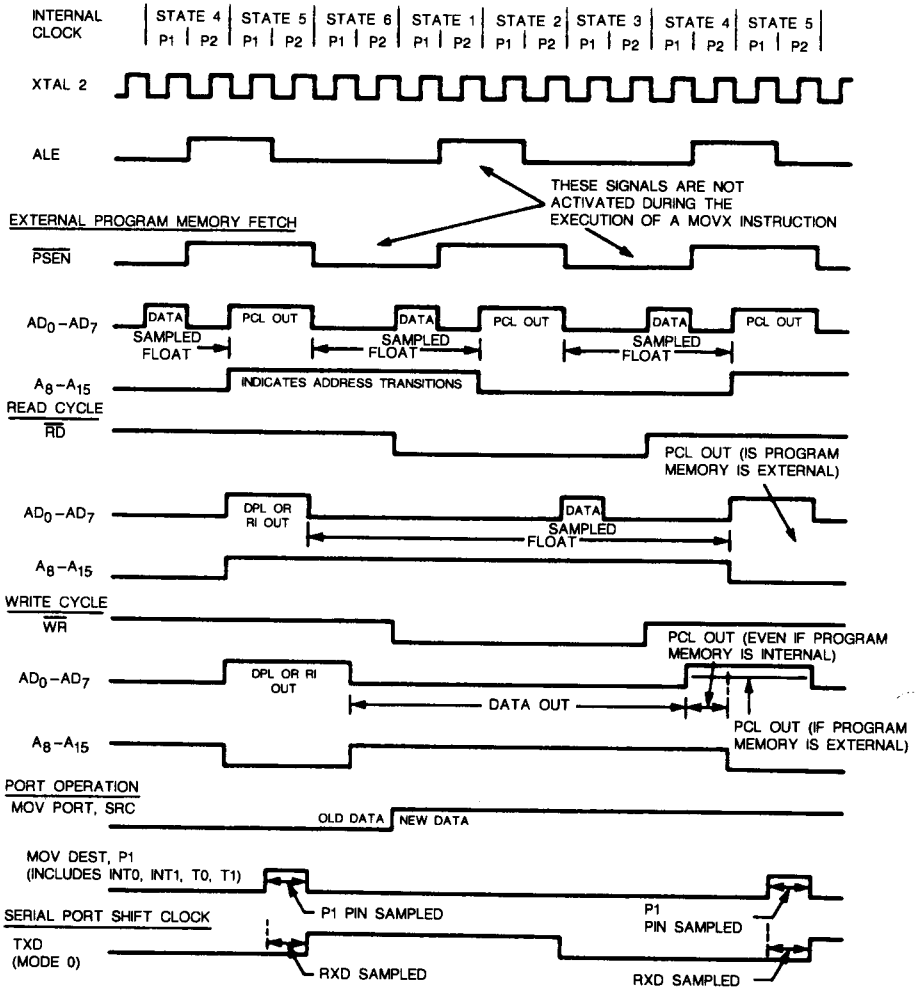
Input/Output Waveform



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

Float Waveform

CLOCK WAVEFORMS



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component to component. Typically though (T_A = 25°C, fully loaded), $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50 ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

TABLE 3. 80C521/80C321/80C541 INSTRUCTION SET

Instructions That Affect Flag Setting*

Instruction	Flag C	Flag OV	Flag AC	Instruction	Flag C	Flag OV	Flag AC
ADD	X	X	X	CLR C	O		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	O	X		ANL C,/bit	X		
DIV	O	X		ORL C, bit	X		
DA	X			ORL C,/bit	X		
RRC	X			MOV C, bit	X		
RLC	X			CJNE	X		
SETB C	1						

Interrupt Response Time: To finish execution of current instruction, respond to the interrupt request and push the PC; to vector to the first instruction of the interrupt service program requires 38 to 81 oscillator periods (2.25 to 5.25 μs at 16 MHz).

*Note that operations on SFR byte address D0H or bit addresses D0 – D7H (i.e., the PSW or bits in the PSW) will also affect flag settings.

DATA TRANSFER

Mnemonic	Description	Byte	Cyc
MOV A,Rn	Move register to Accumulator	1	1
MOV A,direct	Move direct byte to Accumulator	2	1
MOV A,@Ri	Move indirect RAM to Accumulator	1	1
MOV A,#data	Move immediate data to Accumulator	2	1
MOV Rn,A	Move Accumulator to register	1	1
MOV Rn,direct	Move direct byte to register	2	2
MOV Rn,#data	Move immediate data to register	2	1
MOV direct,A	Move Accumulator to direct byte	2	1
MOV direct,Rn	Move register to direct byte	2	2
MOV direct,direct	Move direct byte to direct byte	3	2
MOV direct,@Ri	Move indirect RAM to direct byte	2	2
MOV direct,#data	Move immediate data to direct byte	3	2
MOV @Ri,A	Move Accumulator to indirect RAM	1	1
MOV @Ri,direct	Mode direct byte to indirect RAM	2	2
MOV @Ri,#data	Move immediate data to indirect RAM	2	1
MOV DPTR,#data16	Move 16-bit constant to Data Pointer	3	2
MOVC A,@A + DPTR	Move Code byte relative to DPTR to Accumulator	1	2
MOVC A,@A + PC	Move Code byte relative to PC to Accumulator	1	2
MOVX A,@Ri	Move External RAM (8-bit address) to Accumulator	1	2
MOVX A,@DPTR	Move External RAM (16-bit address) to Accumulator	1	2
MOVX @Ri,A	Move Accumulator to External RAM (8-bit address)	1	2
MOVX @DPTR,A	Move Accumulator to External RAM (16-bit address)	1	2
PUSH direct	Push direct byte onto stack	2	2
POP direct	Pop direct byte off of stack	2	2
XCH A,Rn	Exchange register with Accumulator	1	1
XCH A,direct	Exchange direct byte with Accumulator	2	1
XCH A,@Ri	Exchange indirect RAM with Accumulator	1	1
XCHD A,@Ri	Exchange indirect RAM's least sig nibble with A's LSN	1	1

BOOLEAN VARIABLE MANIPULATION

Mnemonic	Description	Byte	Cyc
CLR C	Clear Carry Flag	1	1
CLR bit	Clear direct bit	2	1
SETB C	Set Carry Flag	1	1
SETB bit	Set direct bit	2	1
CPL C	Complement Carry Flag	1	1
CPL bit	Complement direct bit	2	1
ANL C,bit	AND direct bit to Carry Flag	2	2
ANL C,/bit	AND complement of direct bit to Carry	2	2
ORL C,bit	OR direct bit to Carry Flag	2	2
ORL C,/bit	OR complement of direct bit to Carry	2	2
MOV C,bit	Move direct bit to Carry Flag	2	1
MOV bit,C	Move Carry flag to direct bit	2	2

LOGIC

Mnemonic	Description	Byte	Cyc
ANL A,Rn	AND register to Accumulator	1	1
ANL A,direct	AND direct byte to Accumulator	2	1
ANL A,@Ri	AND indirect RAM to Accumulator	1	1
ANL A,#data	AND immediate data to Accumulator	2	1
ANL direct,A	AND Accumulator to direct byte	2	1

LOGIC (Continued)

Mnemonic	Description	Byte	Cyc
ANL direct,#data	AND immediate data to direct byte	3	2
ORL A,Rn	OR register to Accumulator	1	1
ORL A,direct	OR direct byte to Accumulator	2	1
ORL A,@Ri	OR indirect RAM to Accumulator	1	1
ORL A,#data	OR immediate data to Accumulator	2	1
ORL direct,A	OR Accumulator to direct byte	2	1
ORL direct,#data	OR immediate data to direct byte	3	2
XRL A,Rn	Exclusive-OR register to Accumulator	1	1
XRL A,direct	Exclusive-OR direct byte to Accumulator	2	1
XRL A,@Ri	Exclusive-OR indirect RAM to Accumulator	1	1
XRL A,#data	Exclusive-OR immediate data to Accumulator	2	1
XRL direct,A	Exclusive-OR Accumulator to direct byte	2	1
XRL direct,#data	Exclusive-OR immediate data to direct	3	2
CLR A	Clear Accumulator	1	1
CPL A	Complement Accumulator	1	1
RL A	Rotate Accumulator Left	1	1
RLC A	Rotate Accumulator Left through Carry Flag	1	1
RR A	Rotate Accumulator Right	1	1
RRC A	Rotate Accumulator Right through Carry Flag	1	1
SWAP A	Exchange nibbles within the Accumulator	1	1

ARITHMETIC

Mnemonic	Description	Byte	Cyc
ADD A,Rn	Add register to Accumulator	1	1
ADD A,direct	Add direct byte to Accumulator	2	1
ADD A,@Ri	Add indirect RAM to Accumulator	1	1
ADD A,#data	Add immediate data to Accumulator	2	1
ADDC A,Rn	Add register to Accumulator with carry	1	1
ADDC A,direct	Add direct byte to Accumulator with Carry Flag	2	1
ADDC A,@Ri	Add indirect RAM and Carry Flag to Accumulator	1	1
ADDC A,#data	Add immediate data and Carry Flag to Accumulator	2	1
SUBB A,Rn	Subtract register from Accumulator with Borrow	1	1
SUBB A,direct	Subtract direct byte from Accumulator with Borrow	2	1
SUBB A,@Ri	Subtract indirect RAM from Accumulator with Borrow	1	1
SUBB A,#data	Subtract immediate data from Accumulator with Borrow	2	1
INC A	Increment Accumulator	1	1
INC Rn	Increment register	1	1
INC direct	Increment direct byte	2	1
INC @Ri	Increment indirect RAM	1	1
DEC A	Decrement Accumulator	1	1
DEC Rn	Decrement register	1	1
DEC direct	Decrement direct byte	2	1
DEC @Ri	Decrement indirect RAM	1	1
INC DPTR	Increment Data Pointer	1	2
MUL AB	Multiply Accumulator times B	1	4
DIV AB	Divide Accumulator by B	1	4
DA A	Decimal Adjust Accumulator	1	1

OTHER			
Mnemonic	**Description**	**Byte**	**Cyc**
NOP	No Operation	1	1

CONTROL TRANSFER (BRANCH)			
Mnemonic	**Description**	**Byte**	**Cyc**
AJMP addr11	Absolute Jump	2	2
LJMP addr16	Long Jump	3	2
SJMP rel	Short Jump (relative addr)	2	2
JMP @A + DPTR	Jump indirect relative to the DPTR	1	2
JZ rel	Jump if Accumulator is zero	2	2
JNZ rel	Jump if Accumulator is not zero	2	2
JC rel	Jump if Carry Flag is set	2	2
JNC rel	Jump if carry is not set	2	2
JB bit,rel	Jump relative if direct bit is set	3	2
JNB bit,rel	Jump relative if direct bit is not set	3	2
JBC bit,rel	Jump relative if direct bit is set, then clear bit	3	2
CJNE A,direct,rel	Compare direct byte to Accumulator and Jump if not Equal	3	2
CJNE A,#data,rel	Compare immediate to Accumulator and Jump if not Equal	3	2
CJNE Rn,#data,rel	Compare immediate to reg and Jump if not Equal	3	2
CJNE @Ri,#data,rel	Compare immediate to indirect RAM and Jump if not Equal	3	2
DJNZ Rn,rel	Decrement register and Jump if not zero	2	2
DJNZ direct,rel	Decrement direct byte and Jump if not zero	3	2

CONTROL TRANSFER (SUBROUTINE)			
Mnemonic	**Description**	**Byte**	**Cyc**
ACALL addr11	Absolute Subroutine Call	2	2
LCALL addr16	Long Subroutine Call	3	2
RET	Return from Subroutine Call	1	2
RETI	Return from Interrupt Call	1	2

Notes on Data Addressing Modes:

Rn	–Working register R0–R7 of the currently selected Register bank.
direct	–128 internal RAM locations, any I/O port, control, or Special Function Registers.
@Ri	–Indirect internal RAM location addressed by register R0 or R1.
#data	–8-bit constant included in instruction.
#data16	–16-bit constant included as bytes 2 and 3 of instruction.
bit	–128 software flags, any I/O pin, control, or status bit.

Notes on Program Addressing Modes:

addr16	–Destination address for LCALL and LJMP may be anywhere within the 64-kilobyte program memory address space.
addr11	–Destination address for ACALL and AJMP will be within the same 2-kilobyte page of program memory as the first byte of the following instruction.
rel	–SJMP and all conditional jumps include as 8-bit offset by Range is +127, –128 bytes relative to first byte of the following instruction.

TABLE 4. INSTRUCTION OPCODES IN HEXADECIMAL ORDER

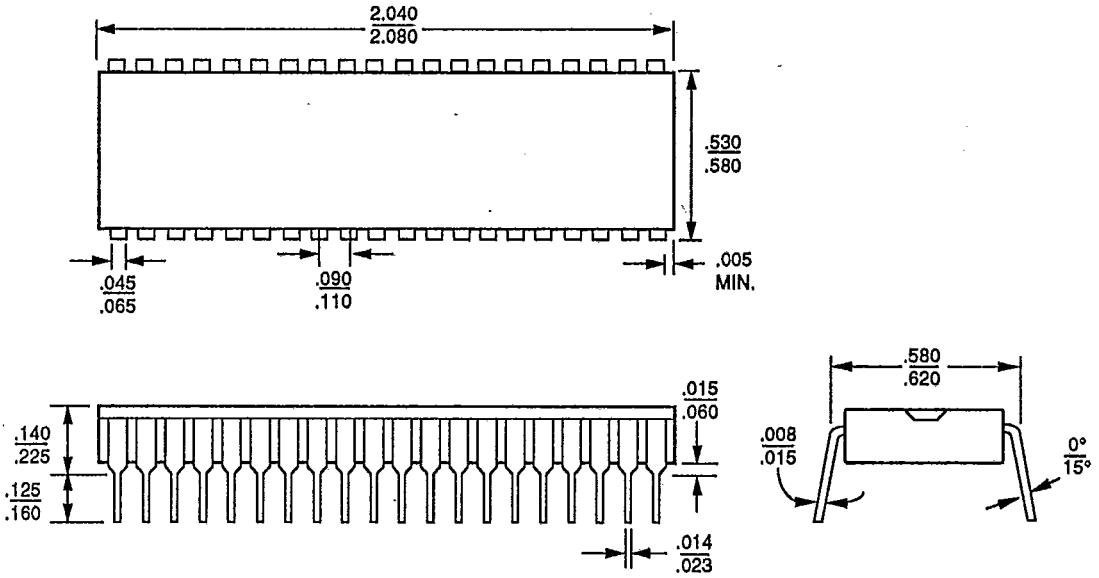
Hex Code	Bytes	Mnemonic	Operands
00	1	NOP	
01	2	AJMP	Code addr
02	3	LJMP	Code addr
03	1	RR	A
04	1	INC	A
05	2	INC	Data addr
06	1	INC	@R0
07	1	INC	@R1
08	1	INC	R0
09	1	INC	R1
0A	1	INC	R2
0B	1	INC	R3
0C	1	INC	R4
0D	1	INC	R5
0E	1	INC	R6
0F	1	INC	R7
10	3	JBC	Bit addr,code addr
11	2	ACALL	Code addr
12	3	LCALL	Code addr
13	1	RRC	A
14	1	DEC	A
15	2	DEC	Data addr
16	1	DEC	@R0
17	1	DEC	@R1
18	1	DEC	R0
19	1	DEC	R1
1A	1	DEC	R2
1B	1	DEC	R3
1C	1	DEC	R4
1D	1	DEC	R5
1E	1	DEC	R6
1F	1	DEC	R7
20	3	JB	Bit addr,code addr
21	2	AJMP	Code addr
22	1	RET	
23	1	RL	A
24	2	ADD	A,#data
25	2	ADD	A,data addr
26	1	ADD	A,@R0
27	1	ADD	A,@R1
28	1	ADD	A,R0
29	1	ADD	A,R1
2A	1	ADD	A,R2
2B	1	ADD	A,R3
2C	1	ADD	A,R4
2D	1	ADD	A,R5
2E	1	ADD	A,R6
2F	1	ADD	A,R7
30	3	JNB	Bit addr,code addr
31	2	ACALL	Code addr
32	1	RETI	
33	1	RLC	A
34	2	ADDC	A,#data
35	2	ADDC	A,data addr
36	1	ADDC	A,@R0
37	1	ADDC	A,@R1
38	1	ADDC	A,R0
39	1	ADDC	A,R1
3A	1	ADDC	A,R2
3B	1	ADDC	A,R3
3C	1	ADDC	A,R4
3D	1	ADDC	A,R5
3E	1	ADDC	A,R6
3F	1	ADDC	A,R7
40	2	JC	Code addr
41	2	AJMP	Code addr
42	2	ORL	Data addr,A
43	3	ORL	Data addr,#data
44	2	ORL	A,#data
45	2	ORL	A,data addr
46	1	ORL	A,@R0
47	1	ORL	A,@R1
48	1	ORL	A,R0
49	1	ORL	A,R1
4A	1	ORL	A,R2
4B	1	ORL	A,R3
4C	1	ORL	A,R4
4D	1	ORL	A,R5
4E	1	ORL	A,R6
4F	1	ORL	A,R7
50	2	JNC	Code addr
51	2	ACALL	Code addr

Hex Code	Bytes	Mnemonic	Operands
52	2	ANL	Data addr,A
53	3	ANL	Data addr,#data
54	2	ANL	A,#data
55	2	ANL	A,data addr
56	1	ANL	A,@R0
57	1	ANL	A,@R1
58	1	ANL	A,R0
59	1	ANL	A,R1
5A	1	ANL	A,R2
5B	1	ANL	A,R3
5C	1	ANL	A,R4
5D	1	ANL	A,R5
5E	1	ANL	A,R6
5F	1	ANL	A,R7
60	2	JZ	Code addr
61	2	AJMP	Code addr
62	2	XRL	Data addr,A
63	3	XRL	Data addr,#data
64	2	XRL	A,#data
65	2	XRL	A,data addr
66	1	XRL	A,@R0
67	1	XRL	A,@R1
68	1	XRL	A,R0
69	1	XRL	A,R1
6A	1	XRL	A,R2
6B	1	XRL	A,R3
6C	1	XRL	A,R4
6D	1	XRL	A,R5
6E	1	XRL	A,R6
6F	1	XRL	A,R7
70	2	JNZ	Code addr
71	2	ACALL	Code addr
72	2	ORL	C,bit addr
73	1	JMP	@A +DPTR
74	2	MOV	A,#data
75	3	MOV	Data addr,#data
76	2	MOV	@R0,#data
77	2	MOV	@R1,#data
78	2	MOV	R0,#data
79	2	MOV	R1,#data
7A	2	MOV	R2,#data
7B	2	MOV	R3,#data
7C	2	MOV	R4,#data
7D	2	MOV	R5,#data
7E	2	MOV	R6,#data
7F	2	MOV	R7,#data
80	2	SJMP	Code addr
81	2	AJMP	Code addr
82	2	ANL	C,bit addr
83	1	MOVC	A,@A +PC
84	1	DIV	AB
85	3	MOV	Data addr,data addr
86	2	MOV	Data addr,@R0
87	2	MOV	Data addr,@R1
88	2	MOV	Data addr,R0
89	2	MOV	Data addr,R1
8A	2	MOV	Data addr,R2
8B	2	MOV	Data addr,R3
8C	2	MOV	Data addr,R4
8D	2	MOV	Data addr,R5
8E	2	MOV	Data addr,R6
8F	2	MOV	Data addr,R7
90	3	MOV	DPTR,#data
91	2	ACALL	Code addr
92	2	MOV	Bit addr,C
93	1	MOVC	A,@A +DPTR
94	2	SUBB	A,#data
95	2	SUBB	A,data addr
96	1	SUBB	A,@R0
97	1	SUBB	A,@R1
98	1	SUBB	A,R0
99	1	SUBB	A,R1
9A	1	SUBB	A,R2
9B	1	SUBB	A,R3
9C	1	SUBB	A,R4
9D	1	SUBB	A,R5
9E	1	SUBB	A,R6
9F	1	SUBB	A,R7
A0	2	ORL	C,/bit addr
A1	2	AJMP	Code addr
A2	2	MOV	C,bit addr
A3	1	INC	DPTR
A4	1	MUL	AB
A5		Reserved	
A6	2	MOV	@R0,data addr
A7	2	MOV	@R1,data addr
A8	2	MOV	R0,data addr
A9	2	MOV	R1,data addr
AA	2	MOV	R2,data addr
AB	2	MOV	R3,data addr
AC	2	MOV	R4,data addr
AD	2	MOV	R5,data addr
AE	2	MOV	R6,data addr
AF	2	MOV	R7,data addr
B0	2	ANL	C,/bit addr
B1	2	ACALL	Code addr
B2	2	CPL	Bit addr
B3	1	CPL	C
B4	3	CJNE	A,#data,code addr
B5	3	CJNE	A,data addr,code addr
B6	3	CJNE	@R0,#data,code addr
B7	3	CJNE	@R1,#data,code addr
B8	3	CJNE	R0,#data,code addr
B9	3	CJNE	R1,#data,code addr
BA	3	CJNE	R2,#data,code addr
BB	3	CJNE	R3,#data,code addr
BC	3	CJNE	R4,#data,code addr
BD	3	CJNE	R5,#data,code addr
BE	3	CJNE	R6,#data,code addr
BF	3	CJNE	R7,#data,code addr
C0	2	PUSH	Data addr
C1	2	AJMP	Code addr
C2	2	CLR	Bit addr
C3	1	CLR	C
C4	1	SWAP	A
C5	2	XCH	A,data addr
C6	1	XCH	A,@R0
C7	1	XCH	A,@R1
C8	1	XCH	A,R0
C9	1	XCH	A,R1
CA	1	XCH	A,R2
CB	1	XCH	A,R3
CC	1	XCH	A,R4
CD	1	XCH	A,R5
CE	1	XCH	A,R6
CF	1	XCH	A,R7
D0	2	POP	Data addr
D1	2	ACALL	Code addr
D2	2	SETB	Bit addr
D3	1	SETB	C
D4	1	DA	A
D5	3	DJNZ	Data addr,code addr
D6	1	XCHD	A,@R0
D7	1	XCHD	A,@R1
D8	2	DJNZ	R0,code addr
D9	2	DJNZ	R1,code addr
DA	2	DJNZ	R2,code addr
DB	2	DJNZ	R3,code addr
DC	2	DJNZ	R4,code addr
DD	2	DJNZ	R5,code addr
DE	2	DJNZ	R6,code addr
DF	2	DJNZ	R7,code addr
E0	1	MOVX	A,@DPTR
E1	2	AJMP	Code addr
E2	1	MOVX	A,@R0
E3	1	MOVX	A,@R1
E4	1	CLR	A
E5	2	MOV	A,data addr
E6	1	MOV	A,@R0
E7	1	MOV	A,@R1
E8	1	MOV	A,R0
E9	1	MOV	A,R1
EA	1	MOV	A,R2
EB	1	MOV	A,R3
EC	1	MOV	A,R4
ED	1	MOV	A,R5
EE	1	MOV	A,R6
EF	1	MOV	A,R7
F0	1	MOVX	@DPTR,A
F1	2	ACALL	Code addr
F2	1	MOVX	@R0,A
F3	1	MOVX	@R1,A
F4	1	CPL	A
F5	2	MOV	Data addr,A
F6	1	MOV	@R0,A
F7	1	MOV	@R1,A
F8	1	MOV	R0,A
F9	1	MOV	R1,A
FA	1	MOV	R2,A
FB	1	MOV	R3,A
FC	1	MOV	R4,A
FD	1	MOV	R5,A
FE	1	MOV	R6,A
FF	1	MOV	R7,A

Package Outlines

PHYSICAL DIMENSIONS*

Plastic Dual-In-Line Package (PD)
PD 040



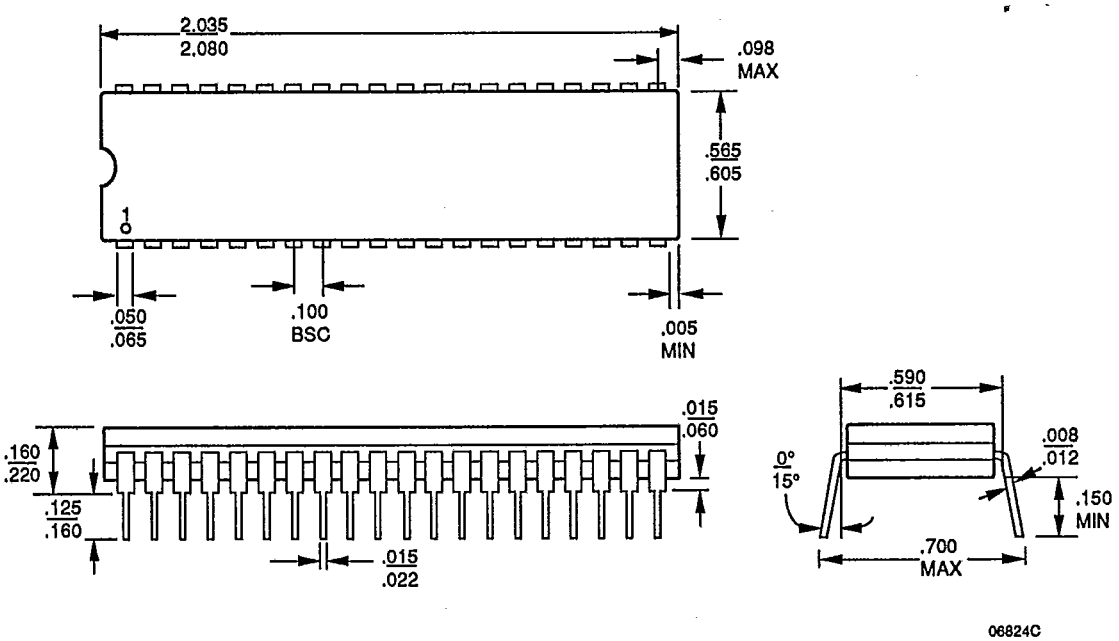
PID# 06823B

* For reference only.

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

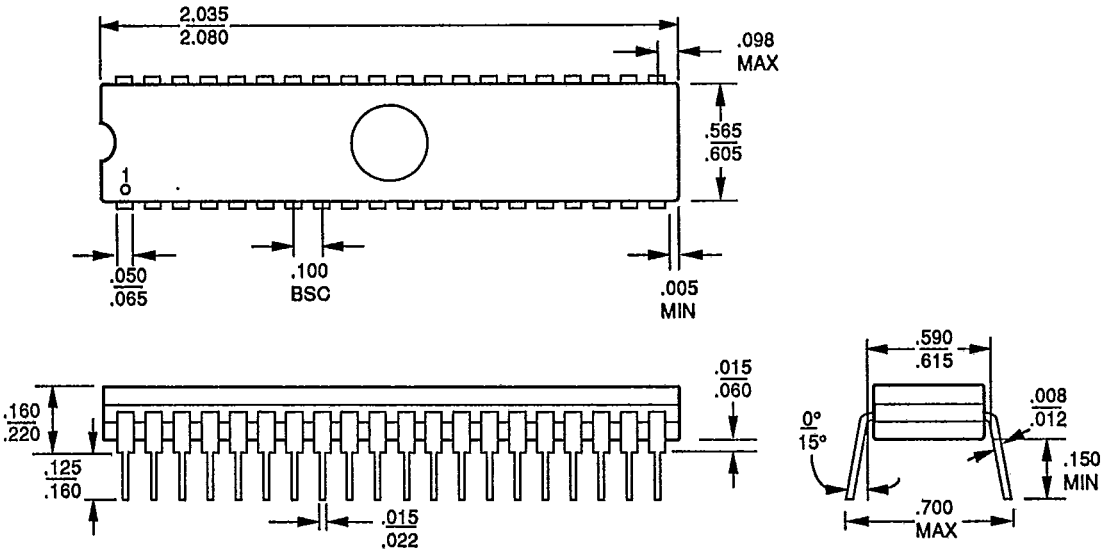
Ceramic Hermetic Dual-In-Line Packages (CD/CDV)

CD 040



06824C

CDV 040

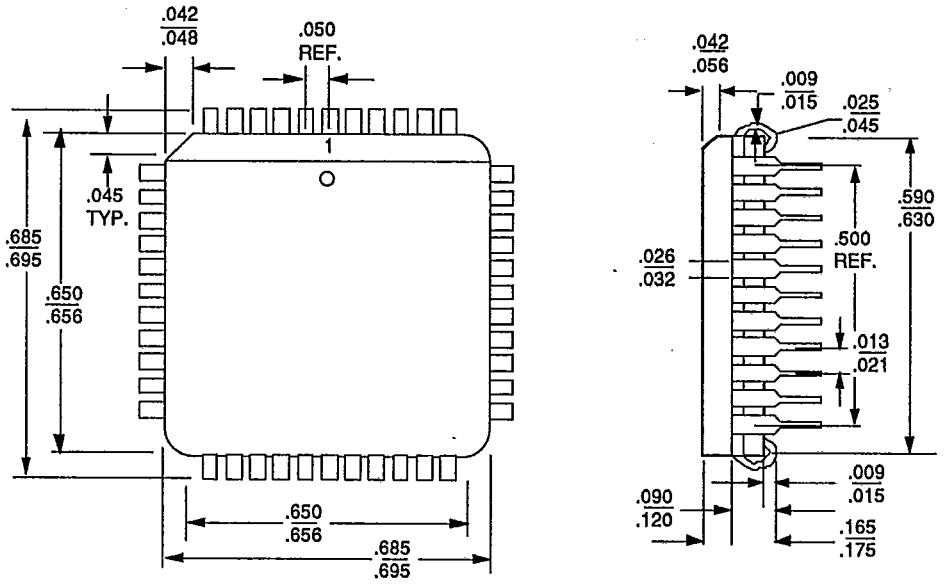


07880C

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

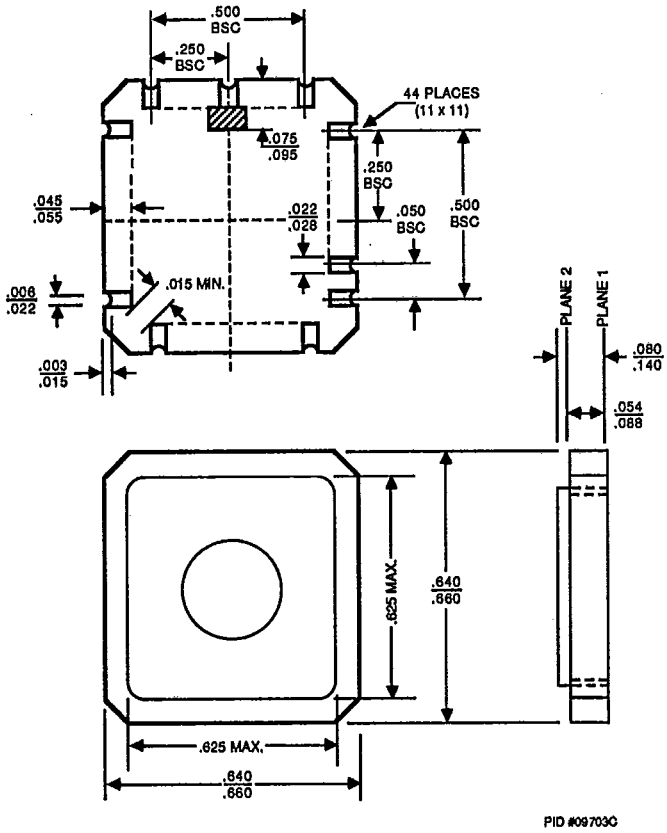
Plastic Leaded Chip Carriers (PL)
PL 044

T-90-20



NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

Ceramic Leadless Chip Carrier (CLV)
CLV 044



NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.