



# CD4541BM/CD4541BC Programmable Timer

## General Description

The CD4541B Programmable Timer is designed with a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, output control logic, and a special power-on reset circuit. The special features of the power-on reset circuit are first, no additional static power consumption and second, the part functions across the full voltage range (3V–15V) whether power-on reset is enabled or disabled.

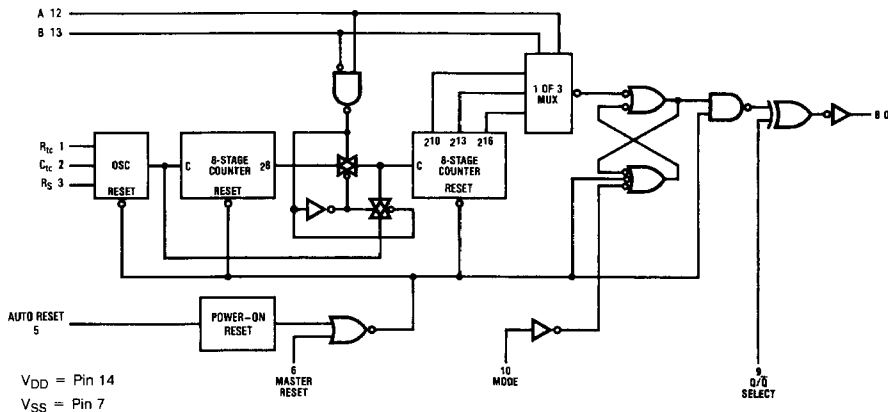
Timing and the counter are initialized by turning on power, if the power-on reset is enabled. When the power is already on, an external reset pulse will also initialize the timing and counter. After either reset is accomplished, the oscillator frequency is determined by the external RC network. The 16-stage counter divides the oscillator frequency by any of 4 digitally controlled division ratios.

## Features

- Available division ratios 2<sup>8</sup>, 2<sup>10</sup>, 2<sup>13</sup>, or 2<sup>16</sup>
- Increments on positive edge clock transitions
- Built-in low power RC oscillator ( $\pm 2\%$  accuracy over temperature range and  $\pm 10\%$  supply and  $\pm 3\%$  over processing @ < 10 kHz)

- Oscillator frequency range  $\approx$  DC to 100 kHz
- Oscillator may be bypassed if external clock is available (apply external clock to pin 3)
- Automatic reset initializes all counters when power turns on
- External master reset totally independent of automatic reset operation
- Operates at 2<sup>n</sup> frequency divider or single transition timer
- Q/ $\bar{Q}$  select provides output logic level flexibility
- Reset (auto or master) disables oscillator during resetting to provide no active power dissipation
- Clock conditioning circuit permits operation with very slow clock rise and fall times
- Wide supply voltage range—3.0V to 15V
- High noise immunity—0.45 V<sub>DD</sub> (typ.)
- 5V–10V–15V parameter ratings
- Symmetrical output characteristics
- Maximum input leakage 1  $\mu$ A at 15V over full temperature range
- High output drive (pin 8) min. one TTL load

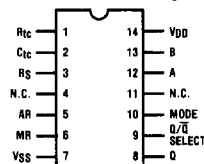
## Logic Diagram



TL/F/6001-1

## Connection Diagram

### Dual-In-Line Package



N.C.—Not connected

Top View

TL/F/6001-2

### Order Number CD4541B\*

\*Please look into Section 8, Appendix D for availability of various package types.

### Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{DD}$ )	-0.5V to +18V
Input Voltage ( $V_{IN}$ )	-0.5V to $V_{DD}$ + 0.5V
Storage Temperature Range ( $T_S$ )	-65°C to +150°C
Power Dissipation ( $P_D$ )	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temperature ( $T_L$ ) (soldering, 10 sec.)	260°C

### Recommended Operating Conditions (Note 2)

Supply Voltage ( $V_{DD}$ )	3V to 15V
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$
Operating Temperature Range	
CD4541BM	-55°C to +125°C
CD4541BC	-40°C to +85°C

CD4541BM/CD4541BC

### DC Electrical Characteristics (Note 2)—CD4541BM

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		5		0.005	5		150	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		10		0.010	10		300	$\mu A$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		20		0.015	20		600	$\mu A$
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V,  I_O  < 1 \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
$V_{OH}$	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V,  I_O  < 1 \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
$V_{IL}$	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0		6	4.0		4.0	V
$V_{IH}$	High Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or 9.0V	7.0		7.0	6		7.0		V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V	11.0		11.0	9		11.0		V
$I_{OL}$	Low Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 0.4V$	2.85		2.27	3.6		1.6		mA
		$V_{DD} = 10V, V_O = 0.5V$	4.96		4.0	9.0		2.8		mA
		$V_{DD} = 15V, V_O = 1.5V$	19.3		15.6	34.0		10.9		mA
$I_{OH}$	High Level Output Current (Note 3)	$V_{DD} = 5V, V_O = 2.5V$	7.96		6.42	13.0		4.49		mA
		$V_{DD} = 10V, V_O = 9.5V$	4.19		3.38	8.0		2.37		mA
		$V_{DD} = 15V, V_O = 3.5V$	16.3		13.2	30.0		9.24		mA
$I_{IN}$	Input Current	$V_{DD} = 15V, V_{IN} = 0V$		-0.10		$-10^{-5}$	-0.10		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.10		$10^{-5}$	0.10		1.0	$\mu A$

### DC Electrical Characteristics (Note 2)—CD4541BC

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		20		0.005	20		150	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		40		0.010	40		300	$\mu A$
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		80		0.015	80		600	$\mu A$
$V_{OL}$	Low Level Output Voltage	$V_{DD} = 5V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V,  I_O  < 1 \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15V$		0.05		0	0.05		0.05	V
$V_{OH}$	High Level Output Voltage	$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V,  I_O  < 1 \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
$V_{IL}$	Low Level Input Voltage	$V_{DD} = 5V, V_O = 0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD} = 15V, V_O = 1.5V$ or 13.5V		4.0		6	4.0		4.0	V

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## DC Electrical Characteristics (Note 2)—CD4541BC (Continued)

Symbol	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V <sub>IH</sub>	High Level Input Voltage	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I <sub>OL</sub>	Low Level Output Current (Note 3)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 0.4V	2.32		1.96	3.6		1.6		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 0.5V	3.18		2.66	9.0		2.18		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 1.5V	12.4		10.4	34.0		8.50		mA
I <sub>OH</sub>	High Level Output Current (Note 3)	V <sub>DD</sub> = 5V, V <sub>O</sub> = 2.5V	5.1		4.27	130		3.5		mA
		V <sub>DD</sub> = 10V, V <sub>O</sub> = 9.5V	2.69		2.25	8.0		1.85		mA
		V <sub>DD</sub> = 15V, V <sub>O</sub> = 13.5V	10.5		8.8	30.0		7.22		mA
I <sub>IN</sub>	Input Current	V <sub>DD</sub> = 15V, V <sub>IN</sub> = 0V		-0.3		-10 <sup>-5</sup>	-0.3		-1.0	μA
		V <sub>DD</sub> = 15V, V <sub>IN</sub> = 15V		0.3		10 <sup>-5</sup>	0.3		1.0	μA

## AC Electrical Characteristics\* T<sub>A</sub> = 25°C, C<sub>L</sub> = 50 pF (refer to test circuits)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t <sub>TLH</sub>	Output Rise Time	V <sub>DD</sub> = 5V		50	200	ns
		V <sub>DD</sub> = 10V		30	100	ns
		V <sub>DD</sub> = 15V		25	80	ns
t <sub>THL</sub>	Output Fall Time	V <sub>DD</sub> = 5V		50	200	ns
		V <sub>DD</sub> = 10V		30	100	ns
		V <sub>DD</sub> = 15V		25	80	ns
t <sub>PLH</sub> , t <sub>PHL</sub>	Turn-Off, Turn-On Propagation Delay, Clock to Q (2 <sup>8</sup> Output)	V <sub>DD</sub> = 5V		1.8	4.0	μs
		V <sub>DD</sub> = 10V		0.6	1.5	μs
		V <sub>DD</sub> = 15V		0.4	1.0	μs
t <sub>PHL</sub> , t <sub>PLH</sub>	Turn-On, Turn-Off Propagation Delay, Clock to Q (2 <sup>16</sup> Output)	V <sub>DD</sub> = 5V		3.2	8.0	μs
		V <sub>DD</sub> = 10V		1.5	3.0	μs
		V <sub>DD</sub> = 15V		1.0	2.0	μs
t <sub>WH(CL)</sub>	Clock Pulse Width	V <sub>DD</sub> = 5V	400	200		ns
		V <sub>DD</sub> = 10V	200	100		ns
		V <sub>DD</sub> = 15V	150	70		ns
f <sub>CL</sub>	Clock Pulse Frequency	V <sub>DD</sub> = 5V		2.5	1.0	MHz
		V <sub>DD</sub> = 10V		6.0	3.0	MHz
		V <sub>DD</sub> = 15V		8.5	4.0	MHz
t <sub>WH(R)</sub>	MR Pulse Width	V <sub>DD</sub> = 5V	400	170		ns
		V <sub>DD</sub> = 10V	200	75		ns
		V <sub>DD</sub> = 15V	150	50		ns
C <sub>I</sub>	Average Input Capacitance	Any Input		5.0	7.5	pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 4)			100		pF

\*AC Parameters are guaranteed by DC correlated testing.

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 2:** V<sub>SS</sub> = 0V unless otherwise specified.

**Note 3:** I<sub>OH</sub> and I<sub>OL</sub> are tested one output at a time.

**Note 4:** C<sub>PD</sub> determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

### Truth Table

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low after Reset	Output Initially High after Reset
10	Single Cycle Mode	Recycle Mode

### Division Ratio Table

A	B	Number of Counter Stages n	Count 2 <sup>n</sup>
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

### Operating Characteristics

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f = \frac{1}{2.3 R_{TC} C_{TC}} \text{ if } (1 \text{ kHz} \leq f \leq 100 \text{ kHz})$$

$$\text{and } R_S \approx 2 R_{TC} \text{ where } R_S \geq 10 \text{ k}\Omega$$

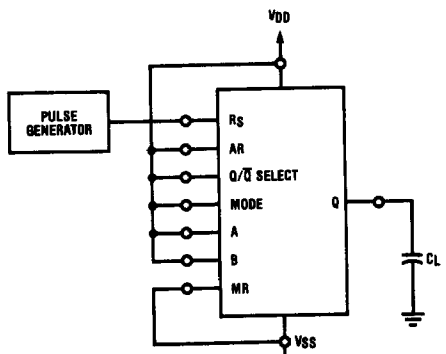
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2<sup>8</sup>, 2<sup>10</sup>, 2<sup>13</sup>, and 2<sup>16</sup>). The 2<sup>n</sup> counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is "1", 2<sup>16</sup> is selected for both states of B.

However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2<sup>8</sup>).

The Q/Q select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/Q select pin is set to a "0" the Q output is a "0". Correspondingly, when Q/Q select pin is set to a "1" the Q output is a "1".

When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after 2<sup>n-1</sup> counts the RS flip-flop sets which causes the output to change state. Hence, after another 2<sup>n-1</sup> counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

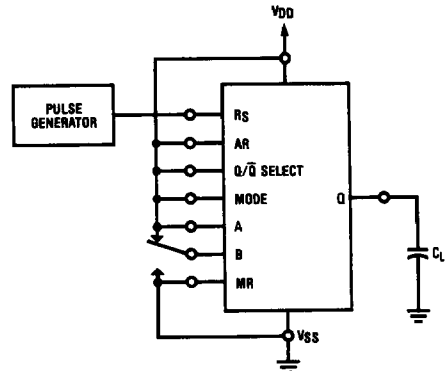
#### Power Dissipation Test Circuit and Waveforms



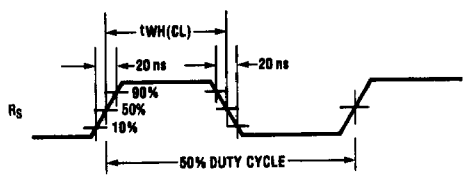
(R<sub>TC</sub> and C<sub>TC</sub> outputs are left open)

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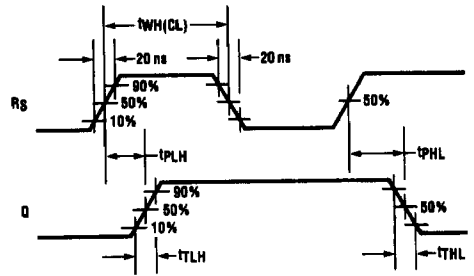
#### Switching Time Test Circuit and Waveforms



TL/F/6001-4



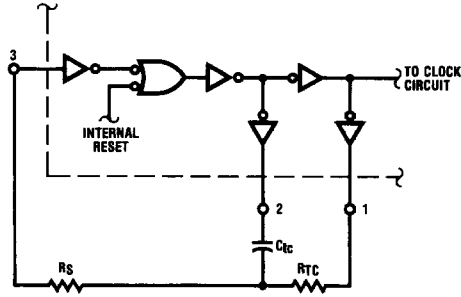
TL/F/6001-5



TL/F/6001-6

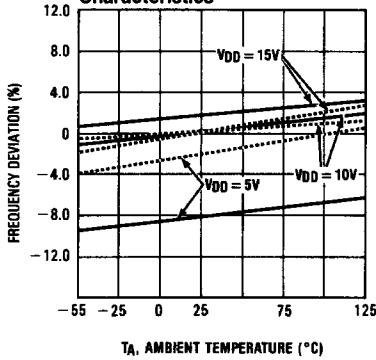
Operating Characteristics (Continued)

Oscillator Circuit Using RC Configuration



TL/F/6001-7

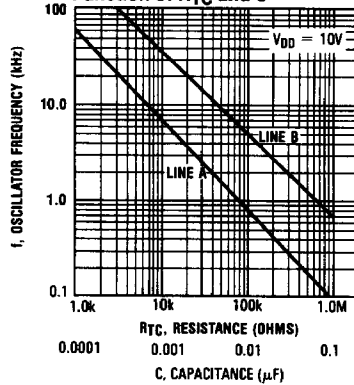
Typical RC Oscillator Characteristics



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Solid Line =  $R_{TC} = 56 \text{ k}\Omega$ ,  $R_S = 1 \text{ k}\Omega$  and  $C = 1000 \text{ pF}$   
 $f = 10.2 \text{ kHz}$  @  $V_{DD} = 10\text{V}$  and  $T_A = 25^\circ\text{C}$   
 Dashed Line =  $R_{TC} = 56 \text{ k}\Omega$ ,  $R_S = 120 \text{ k}\Omega$  and  $C = 1000 \text{ pF}$   
 $f = 7.75 \text{ kHz}$  @  $V_{DD} = 10\text{V}$  and  $T_A = 25^\circ\text{C}$

RC Oscillator Frequency as a Function of  $R_{TC}$  and C



TL/F/6001-9

Line A:  $f$  as a function of  $C$  and ( $R_{TC} = 56 \text{ k}\Omega$ ;  $R_S = 120\text{k}$ )  
 Line B:  $f$  as a function of  $R_{TC}$  and ( $C = 100 \text{ pF}$ ;  $R_S = 2 R_{TC}$ )