AP8048C Datasheet

Audio Application Processor

(ARM Cortex-M3 based)

Rev0.6

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Revision History

Date	Revision	Description
2013-10-9	V0.1	Initial
2013-10-21	V0.11	Change pin47 description
2013-11-4	V0.2	Change pin19's name
2014-03-18	V0.3	Change power supply voltage value
2014-04-11	V0.4	Add the pin function table, LDO33O V-I chart and the store/reflow requirements
2016-01-18	V0.5	Revised the description of chip features
2016-03-20	V0.6	Add the Codec's functional block

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1. Overview

As a highly integrated SoC for audio application processing, AP8048C integrates ARM Cortex-M3, OTG, SD/MMC card controller, SARADC, audio DAC, audio ADC, RTC and IR decoder in a single chip. AP8048C supports Bluetooth stack, various audio decoders，encoders，and effects. In general AP8048C offers low power consumption, flexible and more powerful wireless audio player solution.

1.1 Features

- ARM Cortex-M3, running @ 96MHz, with 128K byte SRAM
- Embedded LDO, with 3.3V output
- OTG 2.0 full-speed controller
- SD/MMC card controller
- 12-bit SARADC
- Low power RTC with NVM to save external RTC & EEPROM
- High speed UART with flow control
- Multiple PWM outputs
- IR (NEC) decoder
- Multiple GPIOs for various purposes
- Code encryption mechanism in SPI-flash
- Support FAT16/FAT32 file system
- Bluetooth stack including A2DP, AVRCP, HFP, SPP, OBEX etc
- Audio input and output
  - Stereo 20-bit high quality Audio DAC, SNR ≥95dB
  - Stereo 16-bit high quality Sigma Delta ADC, SNR ≥90dB
  - Programmable preamp gain for input from microphone and line-in
  - Programmable ALC / Noise Gate
  - Built-in headphone driver with “capless” option
    - >40mW output power into 16Ω / 3.3V
    - THD –80dB at 20mW, SNR 90dB with 16Ω load
  - Tone generator
  - I2S digital audio input/output
  - 9 sample rates supported: 8kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48kHz
- Audio Algorithms
  - Decoders: MP2/MP3, WMA, FLAC(8/16/24bit), AAC/MP4/M4A, WAV(IMA-ADPCM and raw PCM), AIF, AIFC
  - Encoder: MP2/MP3, IMA-ADPCM

- Effects:
  - Echo
  - Reverb
  - MV3D
  - MVBASS
  - Pitch shifter
  - Parametric EQ
  - Dynamic Range Compression (DRC)
  - Acoustic Echo Cancellation (AEC)
  - Programmable frequency shifter for howling prevention
  - Fast and accurate howling detection and suppression

- Serial wire debug (SWD) interface
- Firmware updatable through SD/USB drive

1.2 CODEC Functional Block

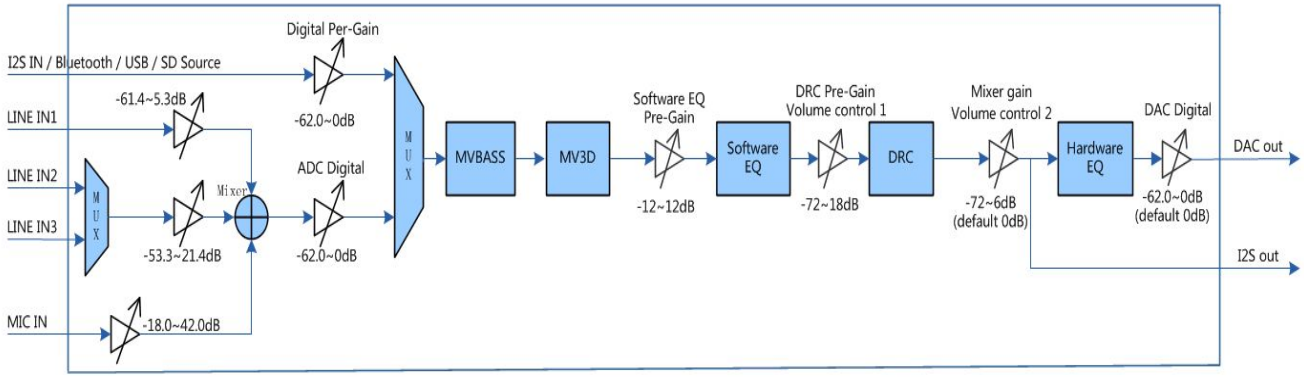


Figure 1 CODEC Functional Block

Notes.

1. Adjust the system volume either through DRC pre-gain (DRC on) or mixer gain (DRC off).
2. Direct control of DAC digital volume is NOT recommended

2. Pin Description

AP8048C is a CMOS device. Floating level on input signals causes unstable device operation and abnormal current consumption. Pull-up or Pull-down resistors should be used appropriately for input or bidirectional pins.

Notation	Description
I	Input
O	Output
I/O	Bidirectional
PWR	Power
GND	Ground

2.1 Pin Description

Table 1 Pin Description

Pin name	Pin #	Type	Description
			Audio CODEC interface pins
DAC_R	6	AO	audio right channel output
DAC_L	7	AO	audio left channel output
DACVMID	5	AI	Internal voltage reference
DAC_LINER	9	AI	Audio aux right in (high quality)
DAC_LINEL	10	AI	Audio aux left in (high quality)
MICIN	11	AI	MIC input
MICBIAS	12	AI	MIC voltage reference
			GPIO/MCU IO pins
GPIO_A[10]	20	I/O	GPIO PORT, bank A
GPIO_A[21:13]	29:21	I/O	GPIO PORT, bank A
GPIO_A[25:24]	31:30	I/O	GPIO PORT, bank A
GPIO_B[6:2]	36:32	I/O	GPIO PORT, bank B
GPIO_B[9:8]	38:37	I/O	GPIO PORT, bank B
GPIO_B[26:20]	46:40	I/O	GPIO PORT, bank B
GPIO_B[30]/ GPIO_B[27]	47	I/O	GPIO PORT, bank B
GPIO_C[11]	48	I/O	GPIO PORT, bank C
GPIO_C[14:12]	3:1	I/O	GPIO PORT, bank C
			CLK pins
XIN	14	I	32.768KHz Crystal oscillator input for PLL
XOUT	13	O	32.768KHz Crystal oscillator output for PLL
			Power/Ground pins
DVSS	39	GND	ground for digital
LDOIN	16	PWR	LDO power in
LDO33O	15	PWR	LDO 3.3V out
LDO12O	18	PWR	LDO 1.2V out
RTCVDD	19	PWR	power for RTC
DACVDD	8	PWR	power for DAC
DACAVSS	4	GND	ground for DAC
			MISC pins
POWER_KEY	17	I	Power Key

Table 2 GPIO Pin Function

Pin Name	Other Function Assignment
GPIO_A[10]	IR0 / PWC0 / PWM3 / WAKEUP
GPIO_A[13]	FSH_HOLD

GPIO_A[14]	FSH_SCK
GPIO_A[15]	FSH_SI
GPIO_A[16]	FSH_WP
GPIO_A[17]	FSH_SO
GPIO_A[18]	FSH_CS
GPIO_A[19]	SD1_DAT / SPIM1_MISO
GPIO_A[20]	SD1_CLK / SPIM1_CLK
GPIO_A[21]	SD1_CMD / SPIM1_MOSI
GPIO_A[24]	BUART_RX / USB1_DP
GPIO_A[25]	BUART_TX / USB1_DM
GPIO_B[2]	MCLK0_IN / MCLK0_OUT
GPIO_B[3]	I2S0_LRCK / PCM0_SYNC / SD2_DAT / SPIM2_MISO
GPIO_B[4]	I2S0_BCLK / PCM0_CLK / SD2_CLK / SPIM2_CLK
GPIO_B[5]	ADC0 / I2S0_DO / PCM0_DO / SD2_CMD / SPIM2_MOSI / WAKEUP
GPIO_B[6]	ADC1 / I2S0_DIN / PCM0_DIN / PWM4 / UART_RX / WAKEUP
GPIO_B[8]	BUART_RX / PWM6
GPIO_B[9]	BUART_TX / PWM7
GPIO_B[20]	PWM7 / SD3_CMD / SPIM3_MOSI / SPIS_MOSI
GPIO_B[21]	PWM6 / SD3_CLK / SPIM3_CLK / SPIS_CLK
GPIO_B[22]	ADC3 / PWM5 / SD3_DAT / SPIM3_MISO / SPIS_MISO / WAKEUP
GPIO_B[23]	ADC4 / PWM4 / SPIS_CS / WAKEUP
GPIO_B[24]	ADC5 / I2S1_LRCK / PCM1_SYNC / PWM3 / WAKEUP
GPIO_B[25]	ADC6 / I2S1_BCLK / PCM1_CLK / PWM2 / WAKEUP
GPIO_B[26]	I2S1_DO / PCM1_DO / PWM1
GPIO_B[27]	I2S1_DIN / PCM1_DIN / PWM0
GPIO_B[30]	32K_OUT1 / BUART_CTS
GPIO_C[11]	LINE2_L(normal quality)
GPIO_C[12]	LINE2_R(normal quality) / SWV
GPIO_C[13]	LINE1_L(normal quality) / SWCLK
GPIO_C[14]	LINE1_R(normal quality) / SWD

Notes.

3. 47 Pin is a double bonding pin combined from GPIO_B[27] and GPIO_B[30], so only one of them can be activated at any given time, the other one should be set as an input without pull-down or pull-up.
4. All GPIOs can be used as external interrupt pins.
5. For each of the following modules, only one port group can be activated at any given time, e.g., either I2S0 or I2S1 can be activated, but not both at the same time.

Module	Port Groups
I2S	I2S0, I2S1
PCM	PCM0, PCM1
SD	SD1, SD2, SD3
SPIM	SPIM1, SPIM2, SPIM3

6. For the following modules, there are two scenarios:
   Scenario 1, the signal bus can be activated separately, e.g., use BUART_TX or BUART_RX only;
   Scenario 2, only one port can be allocated to the signal bus at any given time, e.g., BUART_RX can be allocated to GPIO_A[24] or GPIO_B[8].

Module	Signal Bus	Ports

BUART	BUART_TX	GPIO_A[25], GPIO_B[9]
	BUART_RX	GPIO_A[24], GPIO_B[8]
	BUART_CTS	GPIO_B[30]

3. Package

3.1 Package Diagram

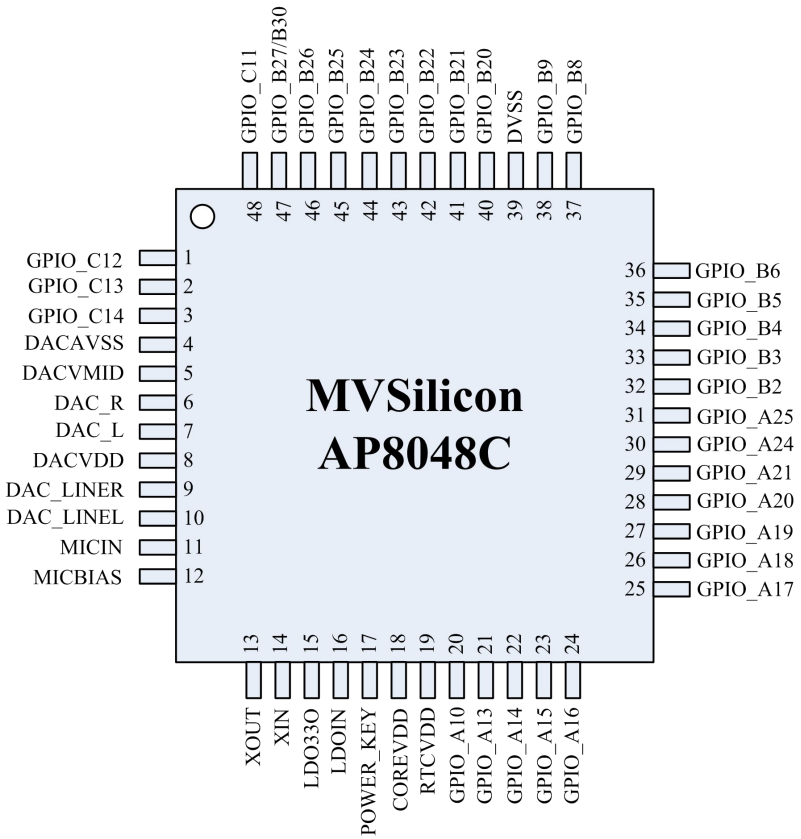


Figure 2 Package Diagram (LQFP48-7x7mm / TOP View)

3.2 Package Dimension Parameter

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.60
A1	0.05	0.15	0.25
A2	1.30	1.40	1.50
A3	0.54	0.64	0.74
b	0.19	—	0.27
b1	0.18	0.20	0.23
c	0.13	—	0.18
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.80	7.00	7.20
E	8.80	9.00	9.20
E1	6.80	7.00	7.20
e		0.50BSC	
L	0.35	0.50	0.65
L1		1.00BSC	
θ	0	—	8°

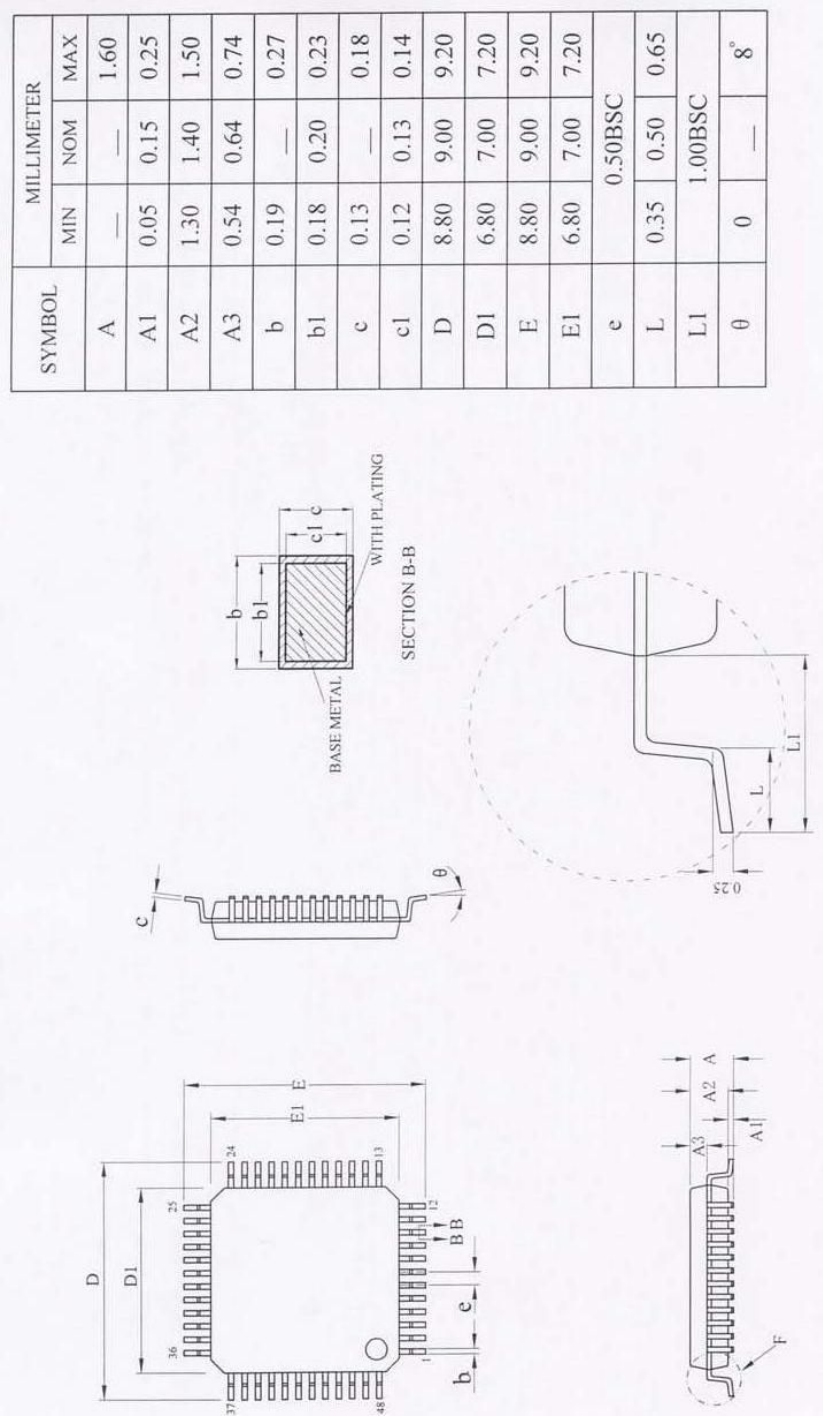


Figure 3 LQFP48-7x7mm Package Dimension Parameter

4. Electrical Specification

4.1 Absolute Maximum Ratings (Note 1)

Table 3 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Storage Temperature	TEMP_STG	-65 to 150	C

4.2 Recommended Operating Conditions

Table 4 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	LDOIN	3.35	5.0	5.5	V
IO Input Voltage	VIN	0		3.6	V
Operating_Free Air Temperature	TEMP_OPR	-40		85	C

4.3 Electrical Characteristics

Table 5 Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		1.6		3.6	V
VIL	Input Low Voltage		-0.3		1.4	V
VOH	Output high voltage	@IOH=2mA	3.0			V
VOL	Output low voltage	@IOL=2mA			0.3	V
IL	Input leakage current		-10		10	uA
P_PLAY current	Current consumption when playing	Playing mode		30		mA
RTC current	Current consumption for RTC & NVM			16		uA

4.4 LDO33O driving capability

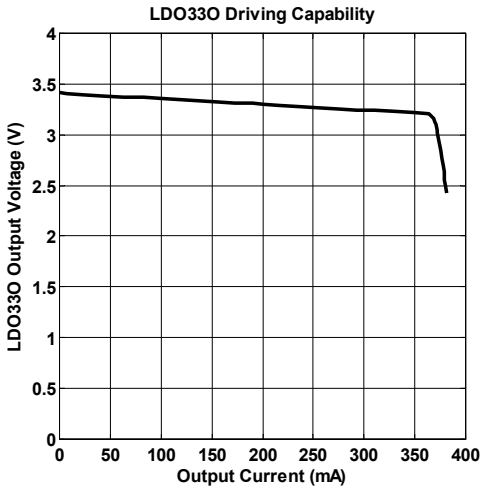


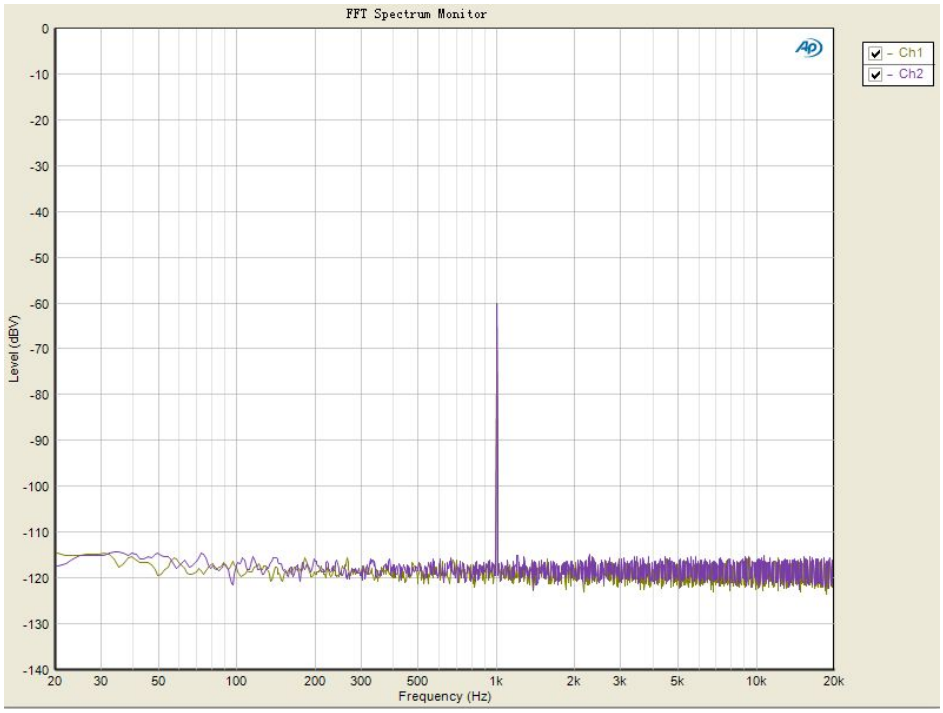
Figure 4 LDO33O driving capability

Note. Not fully tested, characterized only; 2, LDOIN=5V, T_A=25℃

4.5 Audio Performance

Table 6 Audio DAC Performance

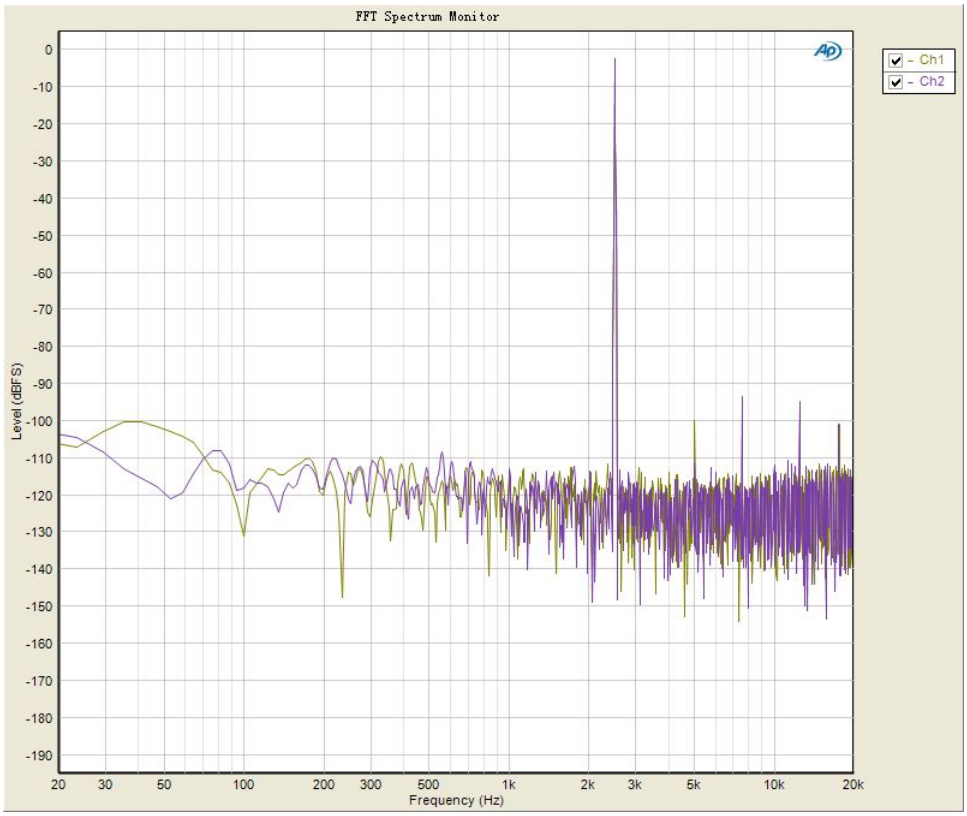
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Range	No Filter		93.6/93.6		dB
	With A-Weighted Filter		95/95		dB
Signal-to-Noise Ratio	No Filter		95.5/95.6		dB
	With A-Weighted Filter		98/98		dB
THD+N	Peak THD+N (@0dBFS)		-81/-81		dB
	0dBFS		-75/-75		dB
Frequency Response			0.06		dBV
Output Swing			0.993		Vrms
Inter-channel Gain Mismatch			0.003		dB
Volume Control Step			TBD		dB
Volume Control Range			TBD		dB
Group Delay			80		us
Inter-channel Phase Deviation			0.01		degree
Crosstalk			-99/-98		dB



The measured output audio spectrum when the output is at -60 dBV

Table 7 DAC LINE-IN (high quality) Channel Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Range	No Filter		88/88		dB
	With A-Weighted Filter		90/90		dB
Signal-to-Noise Ratio	No Filter		88/88		dB
	With A-Weighted Filter		90/90		dB
THD+N	Peak THD+N (@-2.4dBFS)		-84/-84		dB
Volume Control Step			TBD		dB
Volume Control Range			TBD		dB
Group Delay			26		fs
Power Consumption			7.6		mW
Power Supply Rejection Ratio	1kHz, 300mVrms		55		dB



The measured audio spectrum when the analog input is at -2.6 dBV

Table 8 LINE-IN (normal quality) Channel Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Range	No Filter		86		dB
	With A-Weighted Filter		88		dB
Signal-to-Noise Ratio	No Filter		85		dB
	With A-Weighted Filter		87		dB
THD+N	Peak THD+N (@-12dBFS)		-75		dB
Group Delay			26		fs
Power Consumption			7.6		mW
Power Supply Rejection Ratio	1kHz, 300mVrms		55		dB

Table 9 MIC Channel Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Range	No Filter		87.5/87.5		dB
	With A-Weighted Filter		90/90		dB
Signal-to-Noise Ratio	No Filter		85.5/85.5		dB
	With A-Weighted Filter		88.5/88.5		dB
THD+N	Peak THD+N (@-2dBFS)		-82/-82		dB
Group Delay			26		fs
Crosstalk			TBD		dB
Power Consumption			7.6		mW
Power Supply Rejection Ratio	1kHz, 300mVrms		55		dB

Note:

1. “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits.

5. Store and Reflow

AP8048C is a moisture sensitive component. The moisture sensitivity classification is **Class 3**.

It's important that the parts are handled under precaution and a proper manner.

The handling, baking and out-of-pack storage conditions of the moisture sensitive components are described in IPC/JEDC S-STD-033A.

The Technologies recommends utilizing the standard precautions listed below.

1. Calculated shelf life in Sealed Bag: 12 months at <40℃ and <90% relative humidity(RH)
2. Peak Package Body Temperature: 250℃
3. After bag is opened, devices that will be subjected to reflow solder of other high temperature process must be:
   a. Mounted within 168 hours of factory condition ≤30℃ / 60% RH
   b. Stored at <10% RH if not used
4. Devices require baking, before mounting if:
   a. Humidity indicator card is >10% when read at 23±5℃ immediately after moisture barrier bag is opened
   b. Items 3a or 3b is not met
5. If baking is required, please refer to J-STD-033 standard for low temperature (40℃) baking requirement in Tape/Reel form.

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