聯陽半導體
ITE Tech. Inc.

IT68051

Dual-port MHL2.2/HDMI2.0b Receiver with 3D Support

Preliminary Specification V0.9.1

ITE TECH. INC.

To find out more about ITE, visit our World Wide Web at:
http://www.ite.com.tw

Or e-mail itesupport@ite.com.tw for more product information/services

Revision History

Section	Revision	Page No.
-	-	

CONTENTS

FIGURES

TABLES

1. Features

- **Dual port HDMI2.0b Receiver**
- **Support 2 HDMI1.4/HDMI2.0b (18Gb/s) input ports (port-0, port-1)**
- **Support HDMI1.4, HDMI2.0b/MHL2.2 dual mode on input port-0**
- **Compliant with MHL2.2, HDMI1.4b, HDMI 2.0, HDCP1.4, HDCP 2.2 and DVI 1.0 specifications**
- **Supporting link speeds of up to 6.0Gbps (link clock rate of 600MHz) for 4K2K@60hz or 1920x1200@120hz with deep color solution, and up to 1080p@60hz on MHL packed pixel mode**
- **Supporting all the primary 3D formats which are compliant with the HDMI 1.4b 3D specification**
  - Supporting 3D video up to 1080P@50/59.95/60/120Hz, 1080P@23.98/24/29.97/30Hz, 1080i@50/59.94/60/Hz, 720P@23.98/24/29.97/30Hz, 720P@50/59.94/60Hz
  - Supporting formats: Framing Packing, Side-by-Side (half), Top-and-Bottom
  - Support 3D frame packing convert to frame sequence mode
- **Support HDMI2.0b 3D feature**
  - Frame packing mode up to 4Kx2K@23.98/24/30Hz and 1080P@59.94/60Hz
  - Top and Bottom up to 4Kx2K@59.94/60Hz
  - Side-by-Side (Half) up to 4Kx2K@59.94/60Hz
  - Side-by-Side (Full) up to 1080P@59.94/60Hz
  - Support 3D frame packing convert to frame sequence mode
- **Digital audio output interface supporting**
  - up to six I2S interface supporting maximum 12-channel 3D audio, with sample rates of 32~192 kHz and sample sizes of 16~24 bits
  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
  - Support for high-bit-rate (HBR) audio such as DTS-HD and Dolby TrueHD through the four I2S interface or the S/PDIF interface, with frame rates as high as 1536kHz
  - Support maximum 8-channel 3D DSD audio through dedicated inputs
  - Compatible with IEC 60958 and IEC 61937
  - Support Multi-Stream and One Bit Multi-Stream audio packets
  - automatic audio error detection for programmable soft mute, preventing annoying harsh output sound due to audio error or hot-unplug
- **Support 4Kx2K@60/50Hz 9Gb/s YCbCr 4:2:0 convert to 4Kx2K@60/50Hz 18Gb/s YCbCr4:4:4**
  - Support YCbCr 4:2:0 to RGB 4:4:4 or YCbCr 4:4:4 or YCbCr 4:2:2 conversion
- **Support 4Kx2K@60/50Hz down scaling to 1080P@60/50Hz**
  - Support Video format timing VIC(Video Identification ID Code) 96/106, scaling down to VIC 31/75 (3840x2160@50HZ scaling down to 1920x1080@50Hz)
  - Support video format timing VIC(Video Identification ID Code) 97/107, scaling down to VIC 16/76 (3840x2160@60HZ scaling down to 1920x1080@60Hz)
  - Support Video format timing VIC(Video Identification ID Code) 101, scaling down to 2048x1080@50hz
  - Support Video format timing VIC(Video Identification ID Code) 102, scaling down to 2048x1080@60hz

- **Support split single one 18Gb/s 4Kx2K@50/60Hz HDMI2.0b stream to two 9Gb/s 2Kx2K@50/60Hz**
  - Support Even/Odd Pixel split mode
  - Support Left/Right Frame split mode
- **Support HDR packet InfoFrame decode and save the related static metadata in registers table**
- **Support Single-channel TTL output with 36 bits data (12bit deep color) upto 4Kx2K@30Hz resolution with DDR mode**
- **Support Dual-channel TTL output with each channel 30 bits data(10bit deep color), total is 60bits**
  - On DDR mode, the Max. clock rate is upto 150Mhz, the Data rate is upto 300Mhz.
  - The Max. resolution is upto 4Kx2K@60Hz with 8bpp. Or 1920x1200@120 with 10bpp

2. General Description

The IT68051 is a dual-port HDMI2.0b receiver which supports 6.0Gbps/channel capability and up to 18Gb/s bandwidth for each port. The port-0 also can operate in both HDMI2.0b and MHL2.2 dual mode, it is fully compatible with MHL2.2, HDMI 1.4b/HDMI2.0b, HDCP 1.4/HDCP2.2 and also backward compatible to DVI 1.0 specifications. The IT68051 with its Deep Color capability (up to 36-bit) ensures robust reception of high-quality uncompressed video content, along with state-of-the-art uncompressed and compressed digital audio content such as DTS-HD and Dolby TrueHD in digital televisions and projectors. The IT68051 also supports all the primary 3D formats which are compliant with the HDMI 2.0 3D specification.

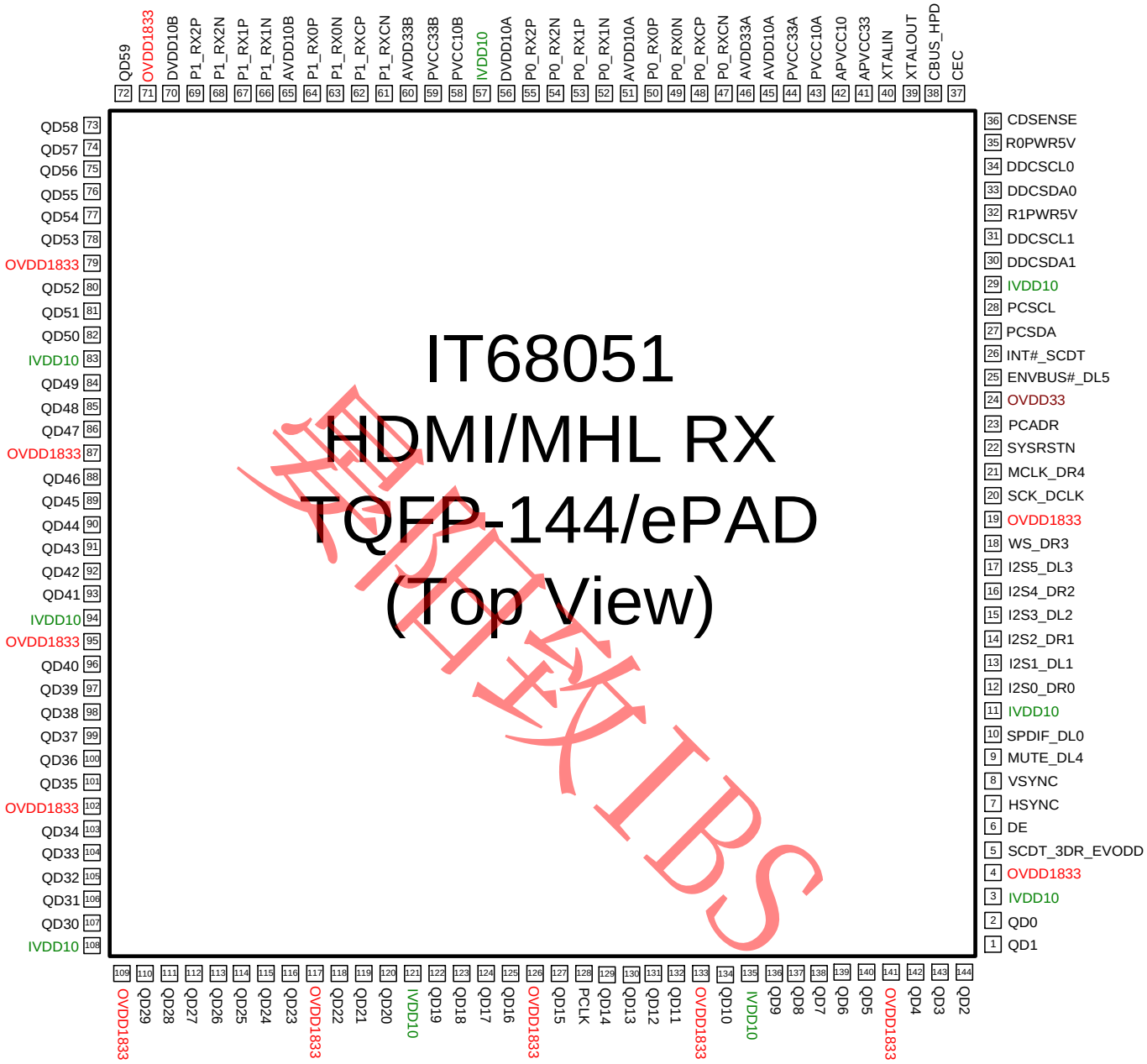
Aside from the various video output formats supported, the IT68051 also receives and provides up to 12 channels of I^2S digital audio outputs, with sampling rate up to 192kHz and sample size up to 24 bits, facilitating direct connection to industry-standard low-cost audio DACs. Also, an S/PDIF output is provided to support up to compressed audio of 192kHz frame rate. Super Audio Compact Disc (SACD) is supported at up to 8 channels and 88.2kHz through DSD (Direct Stream Digital ports) ports.

The High-Bit Rate (HBR) audio is also provided by the IT68051 in two interfaces: with the four I^2S output ports or the S/PDIF output port. With both interfaces the highest possible HBR frame rate is supported at up to 1536kHz.

IT68051 supports 4Kx2K@60/50Hz down scaling to 1080P@60/50Hz. It supports 60 bits LVTTL interface to transmit the various video content to next stage video processor. Via the output interface, IT68051 can support 4K2K@60 UHD video resolution out.
IT68051 also supports video split mode which split single one 18Gb/s 4Kx2K@50/60Hz HDMI2.0b stream to two 9Gb/s 2Kx2K@50/60Hz stream through output interface.

Each IT68051 comes preprogrammed with an unique HDCP key, in compliance with the HDCP standard so as to provide secure transmission of high-definition content. Users of the IT68051 need not purchase any HDCP keys or ROMs.

3. Pin Configuration



4. Pin Description

Table 4-1. Digital Video Output Pins

Pin Name	Direction	Description	Type	Pin No.
QD[59:0]	Output	***Digital Video Output Pins. Channel swap and MSB-LSB reversal are supported through register setting***	LVTTL	1-2, 72-78, 80-82, 84-86, 88-93, 96-101,103-107, 110-116, 118-120, 122-125, 127, 129-132, 134, 136-140, 142-144
PCLK	Output	***Output data clock. The backend controller should use the rising edge of PCLK to strobe QD[59:0]***	LVTTL	128
DE	Output	***Data enable***	LVTTL	6
HSYNC	Output	***Horizontal sync. signal***	LVTTL	7
VSYNC	Output	***Vertical sync. signal***	LVTTL	8
SCDT_3DR_EVODD	Output	***Indication for active MHL/HDMI signal is stable at input port, doubles as 3D R/L signal or Even/Odd Signal***	LVTTL	5

Table 4-2. Digital Audio Input Pins

Pin Name	Direction	Description	Type	Pin No.
XTALIN	Input	***Crystal clock input (for Audio PLL)***	LVTTL	40
XTALOUT	Output	***Crystal clock output (for Audio PLL)***	LVTTL	39
MCLK	Output	***Audio master clock***	LVTTL	21
SCK_DCLK	Output	***I2S serial clock output, doubles as DSD clock***	LVTTL	20
WS_DR3	Output	***I2S word select output, doubles as DSD Serial Right CH3 data output***	LVTTL	18
I2S0_DR0	Output	***I2S serial data output, doubles as DSD Serial Right CH0 data output***	LVTTL	12
I2S1_DL1	Output	***I2S serial data output, doubles as DSD Serial Left CH1 data output***	LVTTL	13
I2S2_DR1	Output	***I2S serial data output, doubles as DSD Serial Right CH1 data output***	LVTTL	14
I2S3_DL2	Output	***I2S serial data output, doubles as DSD Serial Left CH2 data output***	LVTTL	15
I2S4_DR2	Output	***I2S serial data output, doubles as DSD Serial Right CH2 data output***	LVTTL	16
I2S5_DL3	Output	***I2S serial data output, doubles as DSD Serial Left CH3 data output***	LVTTL	17
SPDIF_DL0	Output	***S/PDIF audio output, doubles as DSD Serial Left CH0 data output***	LVTTL	10
MUTE	Output	***Mute output***	LVTTL	9

Table 4-3. Programming Pins

Pin Name	Direction	Description	Type	Pin No.
INT#_SCDT	Output	***Interrupt output. Default active-low (5V-tolerant), doubles as Indication for active MHL/HDMI signal is stable at input port***	LVTTL	26
SYSRSTN	Input	***Hardware reset pin. Active LOW***	Schmitt	22
DDCSCL0	I/O	***DDC I2C Clock for HDMI Port 0 (5V-tolerant)***	Schmitt 5V-TOL	34

DDCSDA0	I/O	***DDC I2C Data for HDMI Port 0 (5V-tolerant)***	Schmitt 5V-TOL	33
R0PWR5V	Input	***TMDS transmitter detection for Port 0(5V-tolerant)***	LVTTL 5V-TOL	35
DDCSCL1	I/O	***DDC I2C Clock for HDMI Port 1 (5V-tolerant)***	Schmitt 5V-TOL	31
DDCSDA1	I/O	***DDC I2C Data for HDMI Port 1 (5V-tolerant)***	Schmitt 5V-TOL	30
R1PWR5V	Input	***TMDS transmitter detection for Port 1(5V-tolerant)***	LVTTL	32
PCSCL	Input	***Serial Programming Clock for chip programming (5V-tolerant)***	Schmitt 5V-TOL	28
PCSDA	I/O	***Serial Programming Data for chip programming (5V-tolerant)***	Schmitt 5V-TOL	27
PCADR	Input	***Serial Programming device address select. Device address is 0x90 when PCADR is pulled low, 0x92 otherwise***	LVTTL	23
CEC	I/O	***CEC function I/O (5V-tolerant)***	LVTTL 5V-TOL	37
CDSENSE	Input	***This pin is used to detect MHL connection (5V-tolerant)***	LVTTL 5V-TOL	36
CBUS/HPD	I/O	***In MHL mode this pin is the Control Bus signal. The CBUS signal is 1.8V. In HDMI mode this pin serves as the HPD out signal***	LVTTL	38
ENVBUS#	Output	***Power supply control output in MHL mode (5V-tolerant)***	LVTTL 5V-TOL	25

Table 4-4. HDMI Analog Front-End Interface Pins

Pin Name	Direction	Description	Type	Pin No.
P0_RX2P	Analog	***HDMI Channel 2 positive input for HDMI Port 0***	TMDS	55
P0_RX2N	Analog	***HDMI Channel 2 negative input for HDMI Port 0***	TMDS	54
P0_RX1P	Analog	***HDMI Channel 1 positive input for HDMI Port 0***	TMDS	53
P0_RX1N	Analog	***HDMI Channel 1 negative input for HDMI Port 0***	TMDS	52
P0_RX0P	Analog	***HDMI Channel 0 positive input for MHL/HDMI Port 0***	TMDS	50
P0_RX0N	Analog	***HDMI Channel 0 negative input for MHL/HDMI Port 0***	TMDS	49
P0_RXCP	Analog	***HDMI Clock Channel positive input for HDMI Port 0***	TMDS	48
P0_RXCN	Analog	***HDMI Clock Channel negative input for HDMI Port 0***	TMDS	47
P1_RX2P	Analog	***HDMI Channel 2 positive input for HDMI Port 1***	TMDS	69
P1_RX2N	Analog	***HDMI Channel 2 negative input for HDMI Port 1***	TMDS	68
P1_RX1P	Analog	***HDMI Channel 1 positive input for HDMI Port 1***	TMDS	67
P1_RX1N	Analog	***HDMI Channel 1 negative input for HDMI Port 1***	TMDS	66
P1_RX0P	Analog	***HDMI Channel 0 positive input for HDMI Port 1***	TMDS	64
P1_RX0N	Analog	***HDMI Channel 0 negative input for HDMI Port 1***	TMDS	63
P1_RXCP	Analog	***HDMI Clock Channel positive input for HDMI Port 1***	TMDS	62
P1_RXCN	Analog	***HDMI Clock Channel negative input for HDMI Port 1***	TMDS	61

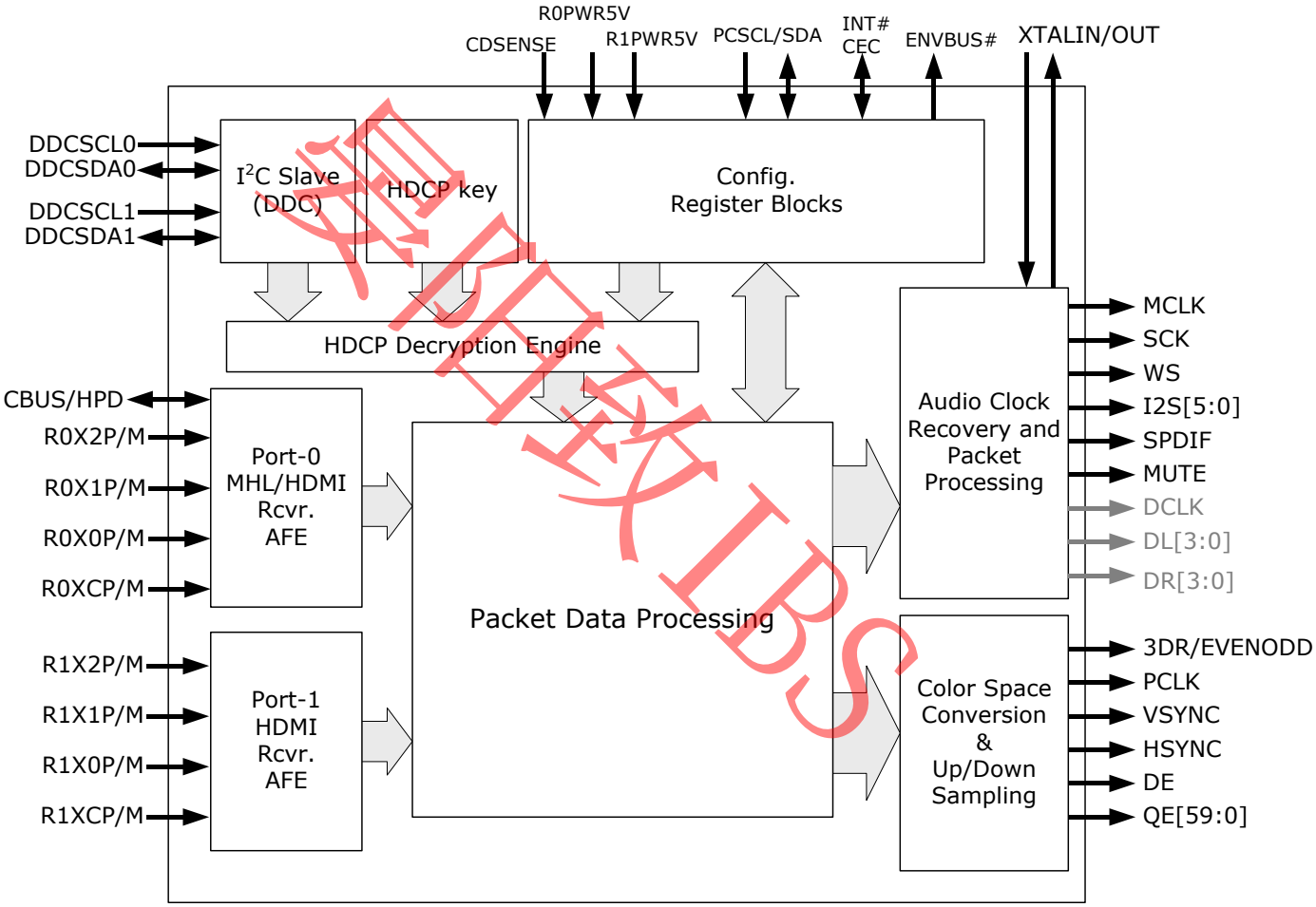
Table 4-5. Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD10	***Digital logic power (1.0V)***	Power	3, 11, 29, 57, 83, 94, 108, 121, 135
OVDD1833	***I/O Pin power (3.3V or 1.8V)***	Power	4, 19, 71, 79, 87, 95, 102, 109, 117, 126, 133, 141
OVDD33	***3/5V I/O Pin power (3.3V)***	Power	24
APVCC33	***MHL/HDMI PLL and analog frontend power (3.3V)***	Power	41
APVCC10	***MHL/HDMI PLL and analog frontend power (1.0V)***	Power	42
PVCC10A	***Port 0 MHL/HDMI receiver PLL power (1.0V)***	Power	43
PVCC33A	***Port 0 MHL/HDMI receiver PLL power (3.3V)***	Power	44
AVDD10A	***Port 0 MHL/HDMI AFE analog power (1.0V)***	Power	45, 51
AVDD33A	***Port 0 MHL/HDMI AFE analog power (3.3V)***	Power	46
DVDD10A	***Port 0 MHL/HDMI AFE digital power (1.0V)***	Power	56
PVCC10B	***Port 1 HDMI receiver PLL power (1.0V)***	Power	58
PVCC33B	***Port 1 HDMI receiver PLL power (3.3V)***	Power	59
AVDD10B	***Port 1 HDMI AFE analog power (1.0V)***	Power	65
AVDD33B	***Port 1 HDMI AFE analog power (3.3V)***	Power	60
DVDD10B	***Port 1 HDMI AFE digital power (1.0V)***	Power	70

5. Functional Description

The IT68051 provides complete solutions for HDMI v2.0b Sink systems, supporting reception and processing of Deep Color video and state-of-the-art digital audio such as DTS-HD and Dolby TrueHD. The IT68051 with its two HDMI input ports supports color depths of 10 bits and 12 bits up to 4Kx2K@30Hz. And with its MH/HDMI dual mode port-0 support MHL2.2 signal input up to 1080p60hz. Advanced processing algorithms are employed to optimize the performance of video processing such as color space conversion and up/down sampling. The following picture is the functional block diagram of the IT68051, which describes clearly the data flow. Note that only one the two inputs can be activated at a time.
The integrated TMDS receiver analog frontend macros are capable of receiving and decoding MHL/HDMI data at up to 6.0Gbps (with a TMDS clock of 600MHz). Adaptive equalization is employed to support long cables.

Figure 5-1. Functional block diagram of IT68051

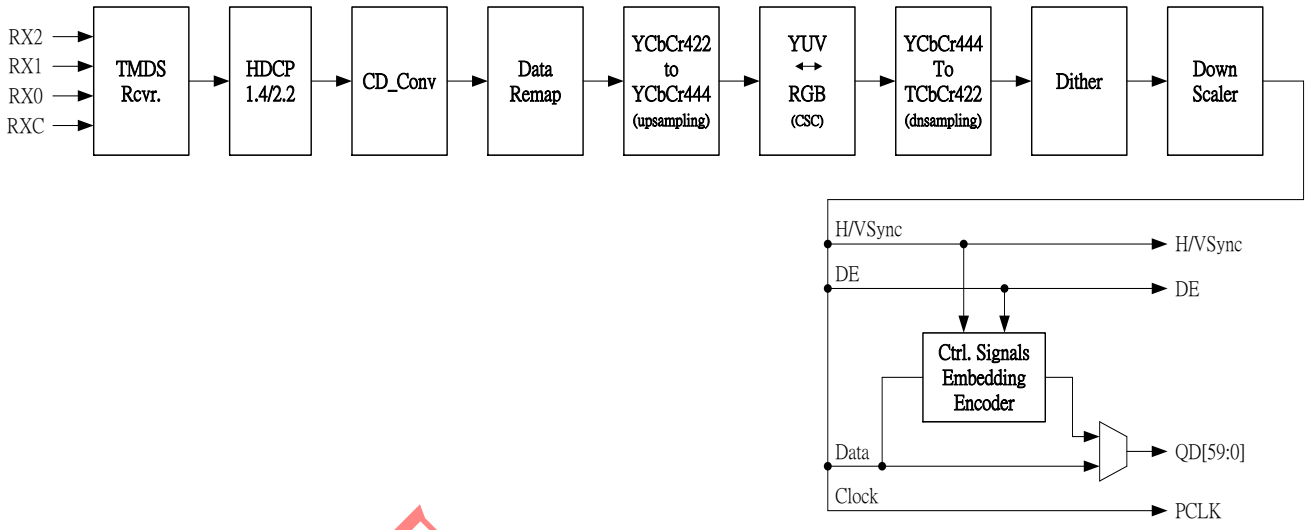


5.1 Video Data Processing Flow

Figure 5-2 depicts the video data processing flow. For the purpose of retaining maximum flexibility, most of the block enablings and path bypassings are controlled through register programming. Please refer to IT68051 Programming Guide for detailed and precise descriptions.

As can be seen from Figure 5-2, the received and recovered HDMI raw data is first HDCP-decrypted. The extracted video data then go through various processing blocks, as described in the following paragraphs, before outputting the proper video format to the backend video controller.

Figure 5-2. Video data processing flow of the IT68051



The video processing including YCbCr up/down-sampling, color-space conversion and dithering. Depending on the selected input and output video formats, different processing blocks are either enabled or bypassed via register control. For the sake of flexibility, this is all done in software register programming. Therefore, extra care should be taken in keeping the selected output format and the corresponding video processing block selection. Please refer to the IT68051 Programming Guide for suggested register setting.

Designated as QD[59:0], the output video data could take on bus width of 24 bits to 36bits in single pixel mode and 24 bits to 30 bits in dual pixel mode, depending on the formats and color depths. The output interface could be configured through register setting to provide various data formats as listed in Table 5-1 in order to cater to different preferences of different backend controllers.

Major video processing in the IT68051 are carried out in 14 bits per channel in order to minimize rounding errors and other computational residuals that occur during processing. General description of video processing blocks is as follows:

HDCP engine (HDCP1.4/2.2)
The HDCP engine include both HDCP1.4 and HDCP2.2 engine. The HDCP engine decrypts in incoming data. Preprogrammed HDCP keys are embedded in the IT68051. Users need not worry about the purchasing and management of the HDCP keys as ITE Tech. will take care of them.

CD_Conv (color-depth conversion)
CD_Conv module can extract correct pixel data from TMDS channel when operation in deep color mode. It also extract correct video control signal form TMDS channel when operation in deep color mode, include H/VSync and DE.

Data Remap
In cases where input HDMI video data are in YCbCr4:2:0 format and output is selected ad 4:2:2 or 4:4:4, this block can convert input format YCbCr420 to YCbCr422. It also can convert 3D LR image to different TTL pair. left half image will output to TTL pair 0 (QD0-29) and right half image will output to TTL pair 1 (QD30-QD59).

Up-sampling (YCbCr422 to YCbCr444)
In cases where input HDMI video data are in YCbCr 4:2:2 format and output is selected as 4:4:4, this block is enabled to do the upsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during upsampling.

Bi-directional Color Space Conversion (YCbCr <-> RGB)
Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer

full compatibility between various Source and Sink combination, this block offers bi-directional RGB <-> YCbCr color space conversion (CSC). To provide maximum flexibility, the matrix coefficients of the CSC engine in the IT68051 are fully programmable. Users could elect to employ their preferred conversion formula. When CSC module is enabled and output color space is RGB, the output video will be full range (RGB: 0-255). When CSC module is enabled and output color space is YUV, the output video can be limit range (Y: 16-235, UV: 16-240) or full range (YUV: 0-255). When CSC module has been power down, the output video range will dependent on input video range.

Down-sampling (YCbCr444 to YCbCr422)
In cases where input HDMI video data are in YCbCr 4:4:4 format and output is selected as YCbCr 4:2:2, this block is enabled to do the downsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during downsampling.

Dithering (Dithering 12-to-10 or 12-to-8)
For outputing to the 10-bits / 8-bits-per-channel formats, decimation might be required depending on the exact input formats. This block performs the necessary dithering for decimation to prevent visible artifacts from appearing.

DownScaler
DownScaler can convert 4Kx2K input video to 1080P video.

5.2 Supported Input Video Formats

Table 5-1 lists the output video formats supported by the IT68051. The listed Output Pixel Clock Frequency in MHz is the actual clock frequency at the output pin PCLK, regardless of the color depth. According to the HDMI Specification v2.0b, the input TMDS clock frequency could be 1.25 times or 1.5 times that of the output PCLK frequency, depending on the color depth:
For 24-bit inputs, TMDS Clock frequency = 1 x PCLK frequency
For 30-bit inputs, TMDS Clock frequency = 1.25 x PCLK frequency
For 36-bit inputs, TMDS Clock frequency = 1.5 x PCLK frequency
The IT68051 also provides automatic video mode detection. The system controller can elect to check out respective status registers to get the information.

Table 5-1 Output video formats supported by the IT68051

					Output Pixel Clock Frequency (MHz)				
Color Space	**Video Format**	**Bus Width**	**H/Vsync**	**Clocking**	**480P**	**720P**	**1080P**	**4Kx2K@30Hz**	**4Kx2K@60Hz**
RGB	4:4:4	24/30/36	Separate	1X	27	74.25	148.5		
		12/15/18	Seperate	Dual-edged	27	74.25	148.5		
		48/60	Separate	1X	13.5	37.13	74.25	148.5	
		24/30/36	Separate	0.5X, Dual-edged	13.5	37.13	74.25	148.5	
		48/60	Separate	0.5X, Dual-edged	6.75	18.57	37.13	74.25	148.5
YCbCr	4:4:4	24/30/36	Separate	1X	27	74.25	148.5		
		12/15/18	Seperate	Dual-edged	27	74.25	148.5		
		48/60	Separate	1X	13.5	37.13	74.25	148.5	
		24/30/36	Separate	0.5X, Dual-edged	13.5	37.13	74.25	148.5	
		48/60	Separate	0.5X, Dual-edged	6.75	18.57	37.13	74.25	148.5
	4:2:2	16/20/24	Separate	1X	27	74.25	148.5		
			Separate	0.5X, Dual-edged	13.5	37.13	74.25	148.5	

			Embedded	1X	27	74.25	148.5		
			Embedded	0.5X, Dual-edged	13.5	37.13	74.25	148.5	
		32/40	Separate	1X	13.5	37.13	74.25	148.5	
			Separate	0.5X, Dual-edged	6.75	18.57	37.13	74.25	148.5
			Embedded	1X	13.5	37.13	74.25	148.5	
			Embedded	0.5X, Dual-edged	6.75	18.57	37.13	74.25	148.5
	BTA1004	16/20/24	Embedded	1X	27	74.25	148.5		
			Embedded	0.5X, Dual-edged	13.5	37.125	74.25		
		32/40	Embedded	1X	13.5	37.13	74.25	148.5	
			Embedded	0.5X, Dual-edged	6.75	18.57	37.13	74.25	148.5

Notes:

- Table cells that are left blanks are those format combinations that are not supported by the IT68051.
- Output channel number is defined by the way the three color components (either R, G & B or Y, Cb & Cr) are arranged. Refer to Video Data Bus Mappings for better understanding.
- Embedded sync signals are defined by CCIR-656 standard, using SAV/EAV sequences of FF, 00, 00, XY.
- The lowest TMDS clock frequency specified by the HDMI standard is 25MHz for 640X480@60Hz.

5.3 Supported 3D Formats

The IT68051 supports all the HDMI 2.0b 3D mandatory formats including
4Kx2K@50Hz --Top-and-Bottom
4Kx2K@59.94/60Hz --Top-and-Bottom
4Kx2K@29.97/30Hz --Framing Packing, Top-and-Bottom
4Kx2K @23.98/24Hz --Framing Packing, Side-by-Side (Half), Top-and-Bottom
1920x1080i@50Hz –Frame Packing, Side-by-Side (Half)
1920x1080i@59.94/60Hz –Frame Packing, Side-by-Side (Half)
1280x 720P@50Hz --Framing Packing, Side-by-Side (Half), Top-and-Bottom
1280x 720P@59.94/60Hz --Framing Packing, Side-by-Side (Half), Top-and-Bottom

5.4 Audio Data Capture and Processing

The audio processing block in the MHL/HDMI Sink is crucial to the system performance since human hearing is susceptive to audio imperfection. The IT68051 prides itself in outstanding audio recovery performances. In addition, the audio clock recovery PLL uses an external crystal reference so as to provide stable and reliable audio clocks for all audio output formats.
The IT68051 supports all audio formats and interfaces specified by the HDMI Specification v2.0b through I2S, S/PDIF and optional one-bit audio outputs. The one-bit audio outputs take on the pins used by I2S outputs, so only one between the two could be activated at a time.

I^2S

Six I2S outputs are provided to support 12-channel uncompressed 3D audio data at up to 192kHz sample rate. A coherent multiple (master) clock MCLK is generated at pin 21 to facilitate proper functions of mainstream backend audio DAC ICs. The supported multiplied factor and sample frequency as well as the resultant MCLK frequencies are summarized in Table 5-2.

Table 5-2 Output MCLK frequencies (MHz) supported by IT68051

Multiple of audio sample frequency	Audio sample frequency								
	32kHz	44.1kHz	48kHz	64kHz	88.2kHz	96kHz	128kHz	176.4kHz	192kHz
128	4.096	5.645	6.144	8.192	11.290	12.288	16.384	22.579	24.576
256	8.192	11.290	12.288	16.384	22.579	24.576	32.768	45.158	49.152
384	12.288	16.934	18.432	24.576	33.869	36.864	49.152	67.738	73.728
512	16.384	22.579	24.576	32.768	45.158	49.152	65.536	90.317	98.304
640	20.480	28.224	30.720	40.960	56.448	61.440	81.920	112.896	122.880
768	24.576	33.869	36.864	49.152	67.738	73.728	98.304	135.475	147.456
896	28.672	39.514	43.008	57.344	79.027	86.016	114.688	N.A.	N.A.
1024	32.768	45.158	49.152	65.536	90.317	98.304	131.072	N.A.	N.A.

Notes:

- The MCLK frequencies in parenthesis are MCLK frequencies over 150MHz. These frequencies are implemented in the IT68051 and could be output through register setting as well. However, the I/O circuit of the MCLK pin does not guarantee to be operating at such a high frequency under normal operation conditions. In addition, few audio backend ICs such as DACs support such high MCLK frequencies. Therefore, using the MCLKs in parenthesis is strongly discouraged.

S/PDIF

The S/PDIF output provides 2-channel uncompressed PCM data (IEC 60958) or compressed multi-channel data (IEC 61937) at up to 192kHz. By default the clock of S/PDIF is carried within the data stream itself via coding. The IT68051 also supplies coherent MCLK in cases of S/PDIF output to help ease the implementation with certain audio processing ICs.

One-Bit Audio (DSD/SACD)

Direct stream digital (DSD) audio is an one-bit audio format which is prescribed by Super Audio CD (SACD) to provide superiore audio hearing experiences. Based on the register setting of the system controller, the IT68051 outputs DSD audio optionally through existing I2S output pins. A total of 8 data outputs are provided for right channels and left channels. Refer to Pin Description on Table 4-2 for detailed port-to-pin mapping.

High-Bit-Rate Audio (HBR)

High-Bit-Rate Audio is also new to the HDMI standard. It is called upon by high-end audio system such as DTS-HD and Dolby TrueHD. No specific interface is defined by the HBR standard. The IT68051 supports HBR audio in two ways. One is to employ the four I2S outputs simultaneously, where the original streaming HBR audio is broken into four parallel data streams. The other is to use the S/PDIF output port. The data rate in the later case is as high as 196.608Mbps. A coherent MCLK is generated by the IT68051 for the backend audio processors.

Smart Audio Error Detection

Some previous HDMI Sink products were reported to generate unbearably harsh sounds during hot-plug/unplug as well as unspecified audio error. IT68051 prides itself for detecting all kinds of audio error and soft-mutes the audio accordingly, therefore preventing unpleasant noise from outputting.

5.5 Interrupt Generation

To provide automatic format setting, hot plug/unplug handling and error handling, the system micro-controller should monitor the interrupt signal output at Pin 26 (INT#). The IT68051 generates an interrupt signal whenever events involving the following signals or situations occur:

1. A status change of incoming 5V power signals at pin 35 or pin 32 (corresponding to plug/unplug)
2. A status change of CDSENSE at pin 36
3. Stable video is acquired (SCDT at pin 5 is asserted)
4. Events of audio errors and/or audio mute

5. Events of ECC errors
6. Video mode change

Without software intervention the hardware of the IT68051 should be able to output some sort of displayable video data in HDMI mode. However, this video could be in the wrong format or color space. Also, hardware alone is not sufficient in handling the exception events listed above. The micro-controller must monitor the INT# signal carefully and poll the corresponding registers for optimum operation.

6. Configuration and Function Control

The IT68051 comes with three serial programming ports: one for interfacing with micro-controller, the other two allowing access by HDMI Sources through the DDC channels of the Port 0/Port 1 HDMI link or received CBUS to DDC transactions of the Port 0 MHL link.

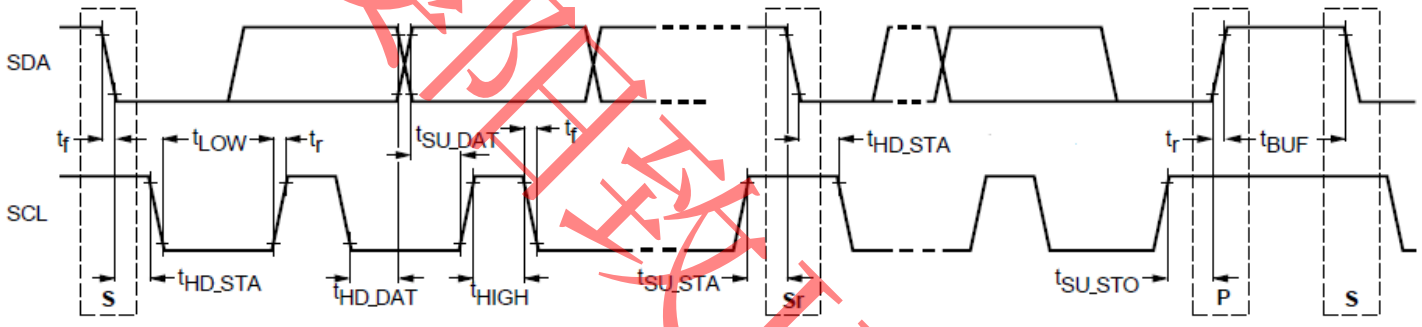
The serial programming interface for interfacing the micro-controller is a slave interface, comprising PCSCL (Pin 28) and PCSDA (Pin 27). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 23). If PCADR is pulled high by the user, the device address is **0x92**. If pulled low, **0x90**.

Since the IT68051 provides one MHL/HDMI input port and one HDMI only input port, two DDC I2C interface are present at DDCSCL0(Pin 34)& DDCSDA0(Pin 33) and DDCSCL1(Pin 31)& DDCSDA1(Pin 30). With the interfaces, the IT68051 responds to the access of HDMI Sources via the DDC channels for both ports or translate the CBUS protocol to DDC protocol for Port 0. HDMI Sources use the interfaces to perform HDCP authentication with the IT68051.

All serial programming interfaces conform to standard I^2C transactions and operate at up to 400kHz.

Characteristics of the PCSDA (PIN27) and PCSCL(PIN28) for F/S-mode I^2C-bus

Figure 6-1 Definition of timing for F/S devices on the I2C-bus



Symbol	Parameter	Standard mode		Fast Mode		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	0	100	0	400	kHz
t_{HD_STA}	Hold time for (repeated) START condition	4.0	-	0.6	-	us
t_{LOW}	LOW period of the SCL clock	4.7	-	1.3	-	us
t_{HIGH}	HIGH period of the SCL clock	4.0	-	0.6	-	us
t_{SU_STA}	Set-up time for a repeated START condition	4.7	-	0.6	-	us
t_{HD_DAT}	Data hold time	0	3.45	0	0.9	us
t_{SU_DAT}	Data set-up time	250	-	100	-	ns
t_r	Rise time of both SDA and SCL signals	-	1000	$20+0.1C_b$ (1)	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	$20+0.1C_b$ (1)	300	ns
t_{SU_STO}	Set-up time for STOP condition	4.0	-	0.6	-	us
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	us
C_b	Capacitive load for each bus line	-	400	-	200	pF
V_{nL}	Noise Margin at the LOW level	0.1*OVDD	-	0.1*OVDD	-	V
V_{nH}	Noise Margin at the HIGH level	0.1*OVDD	-	0.1*OVDD	-	V

Notes:

- Cb = total capacitance of one bus line in pF.

7. Electrical Specifications

7.1 Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
APVCC33	HDMI analog frontend power	-0.3		4.0	V
PVCC33A	Port 0 MHL/HDMI receiver PLL power	-0.3		4.0	V
AVDD33A	Port 0 MHL/HDMI AFE analog power	-0.3		4.0	V
PVCC33B	Port 1 HDMI receiver PLL power	-0.3		4.0	V
AVDD33B	Port 1HDMI AFE analog power	-0.3		4.0	V
OVDD33	I/O pins supply voltage for 3.3/5V I/O	-0.3		4.0	V
OVDD1833	I/O pins supply voltage for 3.3V/1.8V IO	-0.3		4.0	V
APVCC10	HDMI analog frontend power	-0.3		1.2	V
PVCC10A	Port 0 MHL/HDMI receiver PLL power	-0.3		1.2	V
AVDD10A	Port 0 MHL/HDMI AFE analog power	-0.3		1.2	V
DVDD10A	Port 0 digital frontend power	-0.3		1.2	V
PVCC10B	Port 1 HDMI receiver PLL power	-0.3		1.2	V
AVDD10B	Port 1 HDMI AFE analog power	-0.3		1.2	V
DVDD10B	Port 1 digital frontend power	-0.3		1.2	V
IVDD10	Core logic supply voltage	-0.3		1.2	V
VI(non 3/5V)	Input voltage for non 3/5V IO	-0.3		OVDD+0.3	V
VI(3/5V)	Input voltage 3/5V IO	-0.3		5.3	V
Vo	Output Voltage	-0.3		OVDD+0.3	V
TJ	Junction Temperature			125	℃
TSTG	Storage Temperature	-65		150	℃
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:

- Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.

7.2 Functional Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVCC33	HDMI analog frontend power	3.0	3.3	3.6	V
PVCC33A	Port 0 MHL/HDMI receiver PLL power	3.0	3.3	3.6	V
AVDD33A	Port 0 MHL/HDMI AFE analog power	3.0	3.3	3.6	V
PVCC33B	Port 1 HDMI receiver PLL power	3.0	3.3	3.6	V
AVDD33B	Port 1HDMI AFE analog power	3.0	3.3	3.6	V
OVDD33	I/O pins supply voltage for 3.3/5V I/O	3.0	3.3	3.6	V
OVDD1833	I/O pins supply voltage for 3.3V/1.8V IO	3.0	3.3	3.6	V
APVCC10	HDMI analog frontend power	0.95	1.0	1.1	V
PVCC10A	Port 0 MHL/HDMI receiver PLL power	0.95	1.0	1.1	V
AVDD10A	Port 0 MHL/HDMI AFE analog power	0.95	1.0	1.1	V

DVDD10A	Port 0 digital frontend power	0.95	1.0	1.1	V
PVCC10B	Port 1 HDMI receiver PLL power	0.95	1.0	1.1	V
AVDD10B	Port 1 HDMI AFE analog power	0.95	1.0	1.1	V
DVDD10B	Port 1 digital frontend power	0.95	1.0	1.1	V
IVDD10	Core logic supply voltage	0.95	1.0	1.1	V
$V_{CCNOISE}$	Supply noise			25	mV_{PP}
T_A	Ambient temperature			70	℃
Θ_{ja}	Junction to ambient thermal resistance		TBD		℃/W

Notes:

- AVCC33, PVCC33A(B), AVDD33A(B), APVCC10, PVCC10A(B), AVDD10A(B) and DVDD10A(B) should be regulated.
- AVCC33 supplies the termination voltage. Therefore the range is specified by the HDMI Standard.

7.3 DC Electrical Specification

Under functional operation conditions for OVDD1833=OVDD33=3.3V

1.8V~3.3V IO (OVDD1833)							
Symbol	**Parameter**	**Pin Type**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	Input high voltage	LVTTL		2.2		OVDD1833	V
V_{IL}	Input high voltage	LVTTL		GND		0.8	V
V_T	Switching threshold	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage	Schmitt			1.6	2.0	V
5V-Tolerant IO (OVDD33)							
Symbol	**Parameter**	**Pin Type**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{IH}	Input high voltage	LVTTL		2.5		5.5	V
V_{IL}	Input high voltage	LVTTL		GND		0.8	V
V_T	Switching threshold	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage	Schmitt			1.6	2.0	V

Symbol	**Parameter**	**Pin Type**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
V_{OL}	Ouput low voltage	LVTTL	I_{OL} = 2.5~10mA			0.4	V
V_{OH}	Output high voltage	LVTTL	I_{OH} = -2.5~-10mA	2.4			V
I_{IN}	Input leakage current	all	V_{IN} = 3.6V or 0		± 2		μA
I_{OZ}	Tri-state output leakage current	all	V_{IN} = 3.6V or 0		± 5		μA
I_{OL}	Serial programming output sink current	Schmitt	V_{OUT} = 0.2V	2.5		10	mA
V_{diff}	TMDS input differential swing	TMDS		150		1200	mV

Notes:

- Guaranteed by I/O design.
- The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O

design under the condition of driving the output pin with 0.2V. In a real I2C environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I2C Standard. When set at maximum current, the serial programming output ports of the IT68051 are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I2C VIL. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT68051 Programming Guide for proper register setting.

- Limits defined by HDMI 2.0b standard

7.4 Audio AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{S_I2S}	I^2S sample rate	Up to 12 channels	32		192	KHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		1536	KHz
F_{XTAL}	External audio crystal frequency	± 300ppm accuracy	24	27	28.5	MHz

Notes:

- The IT68051 is designed to work in default with a 27MHz crystal for audio functions. Crystals of other frequencies within the designated functional range mandate certain register programming for proper functioning.

7.5 Video AC Timing Specification

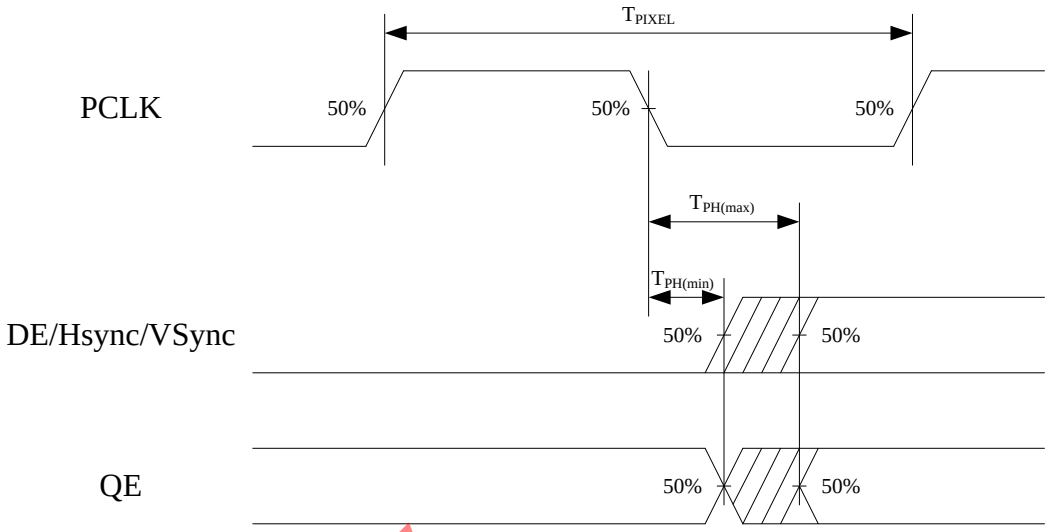
Under functional operation conditions

Symbol	Parameter	Conditions	Min	Tye	Max	Unit
T_{PIXEL}	PCLK pixel clock period	Single-edged clocking	6.17		40	ns
F_{PIXEL}	PCLK pixel clock frequency		25		162	MHz
T_{CDE}	PCLK dual-edged clock period	Dual-edged clocking	6.66		40	ns
F_{CDE}	PCLK dual-edged clock frequency		25		150	MHz
T_{PDUTY}	PCLK clock duty cycle		40%		60%	
$T_{PHsingle}$	PCLK falling edge to Transition time	single-pixel mode	0.84		2.70	ns
T_{PHdual}	PCLK falling/rising edge to Transition time	dual-pixel mode	1.16		2.74	ns

Notes:

- F_{PIXEL} is the inverse of T_{PIXEL}. Operating frequency range is given here while the actual video clock frequency should comply with all video timing standards. Refer to Table 5-1 for supported video timings and corresponding pixel frequencies.
- All setup time and hold time specifications are with respect to the latching edge of PCLK selected by the user through register programming.
- The PCLK falling edge to transition time could be got when Vclk_inv (reg[0x1C4]bit[7]='1') is enabled. If user intends to delay 0.5Tpixel for TTL data output, please disable Vclk_inv bit (reg[0x1C4]bit[7]='0'). And then TPH will increase 0.5Tpixel.

Figure 7-1 PCLK falling edge to transition time under single-data-rate mode



7.6 Operation Supply Current Specification

Normal Operation Mode

	Typical			Maximum		
Video Format	**Total 1.0V (mA)**	**Total 3.3V (mA)**	**Total Power (mW)**	**Total 1.0V (mA)**	**Total 3.3V (mA)**	**Total Power (mW)**
VIC=102, 8ch 192k, HDCP2.2	451.9	257.33	1301.05	469.85	454.47	1969.6
VIC=100, 8ch 192k, HDCP2.2	269.9	189	893.56	279.54	292.99	1246.41
VIC=100, 8ch 192k, HDCP1.4	242.3	189	865.85	252.57	292.97	1219.37
VIC=16, 8ch 192k, HDCP1.4	189.3	168.2	744.45	214.91	199.45	873.1
VIC=4, 8ch 192k, HDCP1.4	103.6	118.5	494.58	105.63	139.85	567.14
VIC=2, 2ch 192k, HDCP1.4	71.2	105.3	418.65	72.4	113.41	446.65

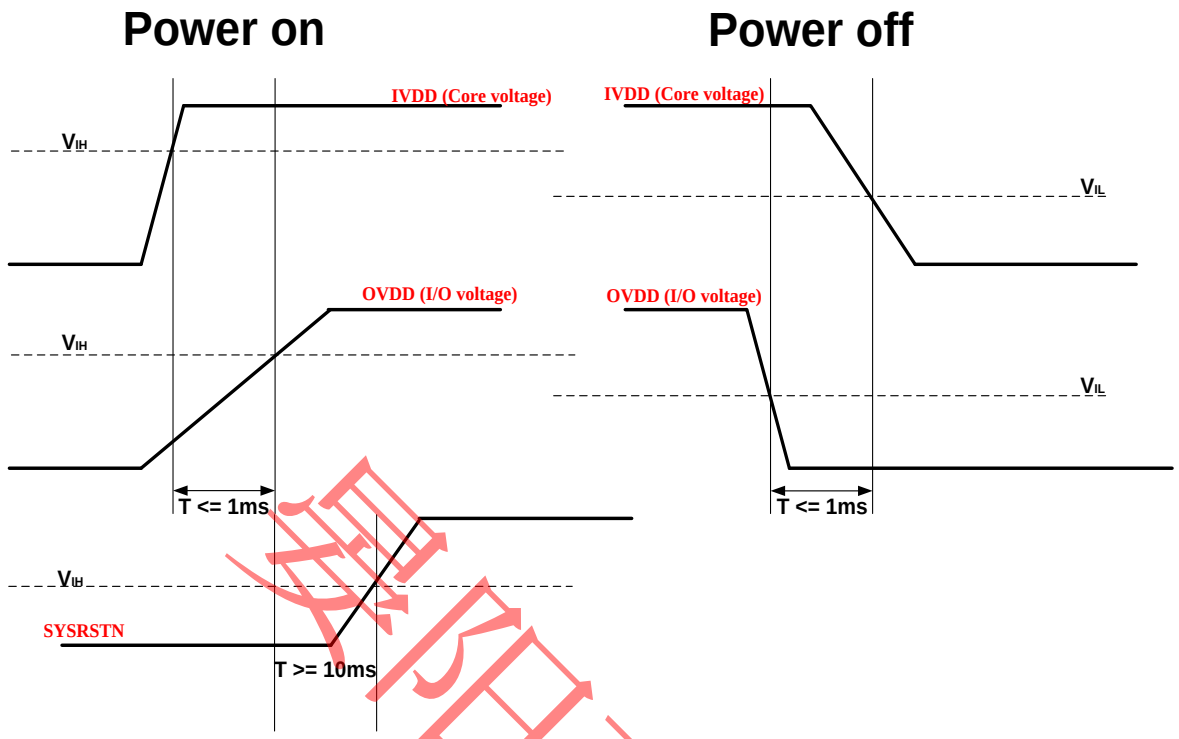
Notes:

- Typical measured by color bar pattern, Maximum measured by freq sweep pattern
- VIC=102, 8ch 192k, HDCP2.2: 4Kx2K@60Hz, using dual pixel mode, Audio = I2S 8ch 192K, with HDCP2.2
- VIC=100, 8ch 192k, HDCP2.2: 4Kx2K@30Hz, using single pixel mode, Audio = I2S 8ch 192K, with HDCP2.2
- VIC=100, 8ch 192k, HDCP1.4: 4Kx2K@30Hz, using single pixel mode, Audio = I2S 8ch 192K, with HDCP1.4
- VIC=16, 8ch 192k, HDCP1.4: 1080P@60Hz, using single pixel mode, Audio = I2S 8ch 192K, with HDCP1.4
- VIC=4, 8ch 192k, HDCP1.4: 720P@60Hz, using single pixel mode, Audio = I2S 8ch 192K, with HDCP1.4
- VIC=2, 2ch 192k, HDCP1.4: 480P@60Hz, using single pixel mode, Audio = I2S 2ch 192K, with HDCP1.4

Standby Mode

	Total 1.0V (mA)	**Total 3.3V (mA)**	**Total Power (mW)**
Standby Mode	5.416	0.154	5.93

7.7 Power and System Reset Sequence



When power on, please keep IVDD go VIH before OVDD go VIH (IVDD must supply earlier than or equal to OVDD). And please keep the time interval between IVDD and OVDD shorter than 1ms when power on or power off.

8. Video Output Configurations and Support Modes

Table 8-1 Output video format supported by IT68051

Color Space	Video Format	Bus Width	H/Vsync	Clocking
RGB	4:4:4	24/30/36	Seperate	1X
		24/30/36	Seperate	0.5X, Dual-edged
		12/15/18	Seperate	1X, Dual-edged
		48/60	Seperate	0.5X, Dual-pixel
		48/60	Seperate	0.25X, Dual-pixel and Dual-edged
YCbCr	4:4:4	24/30/36	Seperate	1X
		24/30/36	Seperate	0.5X, Dual-edged
		12/15/18	Seperate	1X, Dual-edged
		48/60	Seperate	0.5X, Dual-pixel
		48/60	Seperate	0.25X, Dual-pixel and Dual-edged
	4:2:2	16/20/24	Seperate	1X
			Seperate	0.5X, Dual-edged
			Embedded	1X
			Embedded	0.5X, Dual-edged
		32/40	Seperate	0.5X, Dual-pixel
			Seperate	0.25X, Dual-pixel and Dual-edged
			Embedded	0.5X, Dual-pixel
			Embedded	0.25X, Dual-pixel and Dual-edged
	BTA1004	16/20/24	Embedded	1X
			Embedded	0.5X, Dual-edged
		32/40	Embedded	0.5X, Dual-pixel
			Embedded	0.25X, Dual-pixel and Dual-edged

8.1 Single Pixel Mode

There are three output IO modes when IT68051 operated in single pixel mode. QE[11:0] = Pixel B, QE[23:12] = Pixel G, QE[35:24] = Pixel R. The mapping between QEx and QDx as Table 8-2.

Table 8-2 IO mapping for single pixel mode

	Mode 0	Mode 1	Mode2
QE0	QD0	QD30	QD24
QE1	QD1	QD31	QD25
QE2	QD2	QD0	QD30
QE3	QD3	QD1	QD31
QE4	QD4	QD2	QD32
QE5	QD5	QD3	QD33
QE6	QD6	QD4	QD34
QE7	QD7	QD5	QD35
QE8	QD8	QD6	QD36
QE9	QD9	QD7	QD37
QE10	QD10	QD8	QD38
QE11	QD11	QD9	QD39
QE12	QD12	QD32	QD26
QE13	QD13	QD33	QD27
QE14	QD14	QD10	QD40
QE15	QD15	QD11	QD41
QE16	QD16	QD12	QD42
QE17	QD17	QD13	QD43
QE18	QD18	QD14	QD44
QE19	QD19	QD15	QD45
QE20	QD20	QD16	QD46
QE21	QD21	QD17	QD47
QE22	QD22	QD18	QD48
QE23	QD23	QD19	QD49
QE24	QD24	QD34	QD28
QE25	QD25	QD35	QD29
QE26	QD26	QD20	QD50
QE27	QD27	QD21	QD51
QE28	QD28	QD22	QD52
QE29	QD29	QD23	QD53
QE30	QD30	QD24	QD54
QE31	QD31	QD25	QD55
QE32	QD32	QD26	QD56
QE33	QD33	QD27	QD57
QE34	QD34	QD28	QD58
QE35	QD35	QD29	QD59

8.1.1 RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs

Table 8-3 RGB & YUV 4:4:4 data mapping

	RGB			YCbCr		
Pin Name	36-bit	30-bit	24-bit	36-bit	30-bit	24-bit
QE0	B0	NC	NC	Cb0	NC	NC
QE1	B1	NC	NC	Cb1	NC	NC
QE2	B2	B0	NC	Cb2	Cb0	NC
QE3	B3	B1	NC	Cb3	Cb1	NC
QE4	B4	B2	B0	Cb4	Cb2	Cb0
QE5	B5	B3	B1	Cb5	Cb3	Cb1
QE6	B6	B4	B2	Cb6	Cb4	Cb2
QE7	B7	B5	B3	Cb7	Cb5	Cb3
QE8	B8	B6	B4	Cb8	Cb6	Cb4
QE9	B9	B7	B5	Cb9	Cb7	Cb5
QE10	B10	B8	B6	Cb10	Cb8	Cb6
QE11	B11	B9	B7	Cb11	Cb9	Cb7
QE12	G0	NC	NC	Y0	NC	NC
QE13	G1	NC	NC	Y1	NC	NC
QE14	G2	G0	NC	Y2	Y0	NC
QE15	G3	G1	NC	Y3	Y1	NC
QE16	G4	G2	G0	Y4	Y2	Y0
QE17	G5	G3	G1	Y5	Y3	Y1
QE18	G6	G4	G2	Y6	Y4	Y2
QE19	G7	G5	G3	Y7	Y5	Y3
QE20	G8	G6	G4	Y8	Y6	Y4
QE21	G9	G7	G5	Y9	Y7	Y5
QE22	G10	G8	G6	Y10	Y8	Y6
QE23	G11	G9	G7	Y11	Y9	Y7
QE24	R0	NC	NC	Cr0	NC	NC
QE25	R1	NC	NC	Cr1	NC	NC
QE26	R2	R0	NC	Cr2	Cr0	NC
QE27	R3	R1	NC	Cr3	Cr1	NC
QE28	R4	R2	R0	Cr4	Cr2	Cr0
QE29	R5	R3	R1	Cr5	Cr3	Cr1
QE30	R6	R4	R2	Cr6	Cr4	Cr2
QE31	R7	R5	R3	Cr7	Cr5	Cr3
QE32	R8	R6	R4	Cr8	Cr6	Cr4
QE33	R9	R7	R5	Cr9	Cr7	Cr5
QE34	R10	R8	R6	Cr10	Cr8	Cr6
QE35	R11	R9	R7	Cr11	Cr9	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

These are the simpliest formats, with a complete definition of every pixel in each clock period. Timing examples of 36-bit and 30-bit RGB 4:4:4 is depicted in Figure 8-1 and Figure 8-2 respectively.

Figure 8-1 36-bit RGB 4:4:4 timing diagram

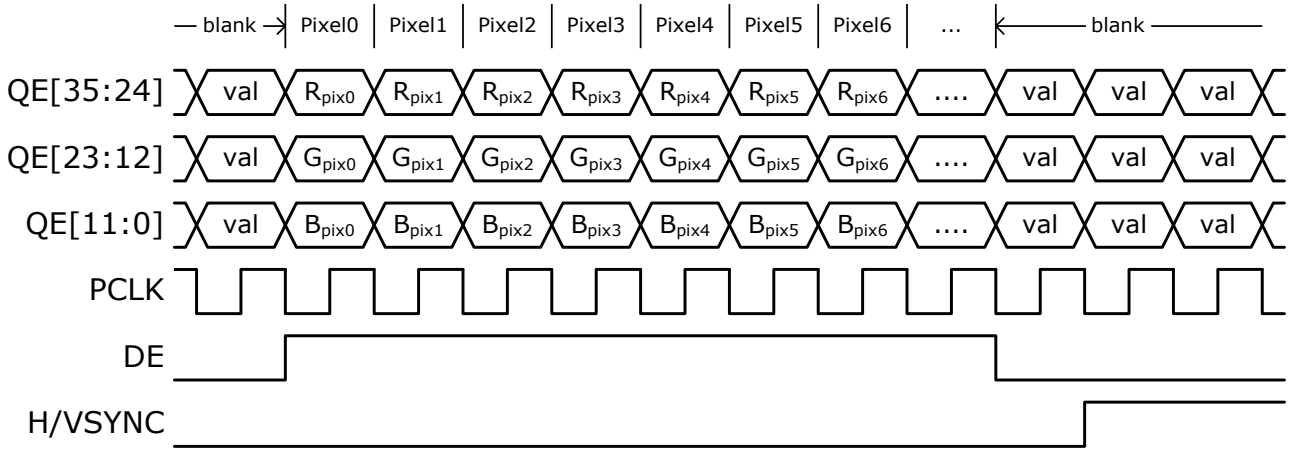
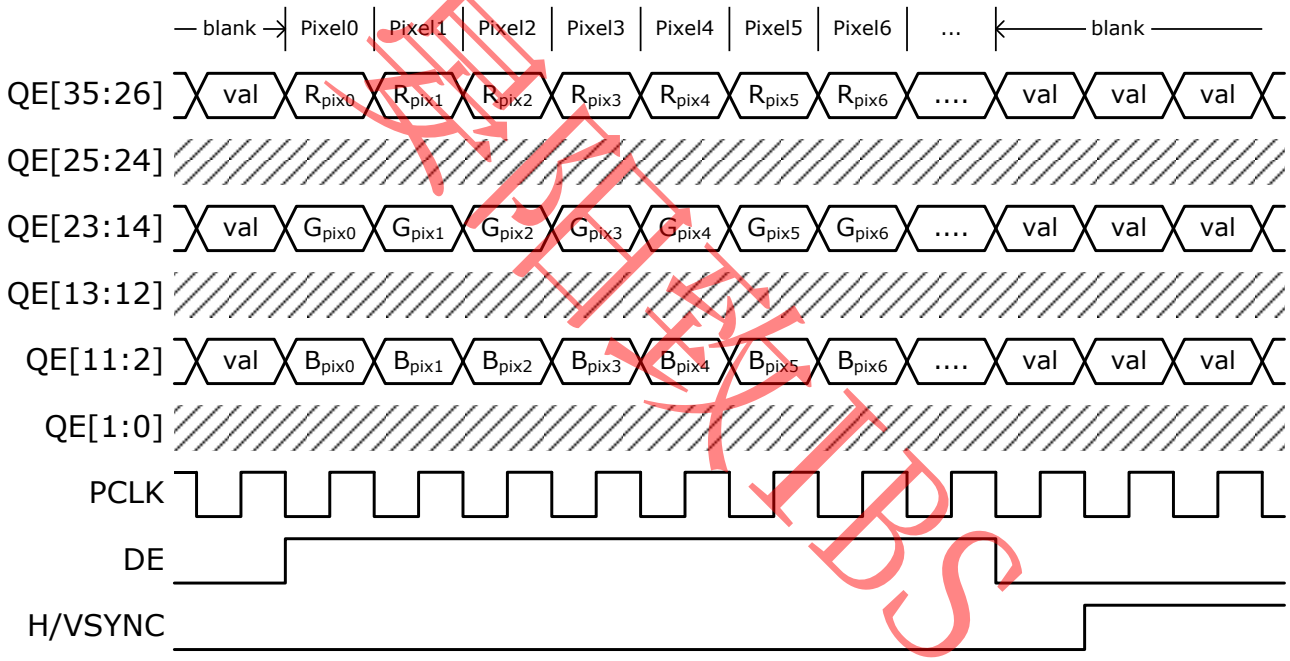


Figure 8-2 30-bit RGB 4:4:4 timing diagram



8.1.2 RGB 4:4:4 and YCbCr 4:4:4 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

Figure 8-3 36-bit RGB 4:4:4 dual-edges triggered with 0.5X PCLK

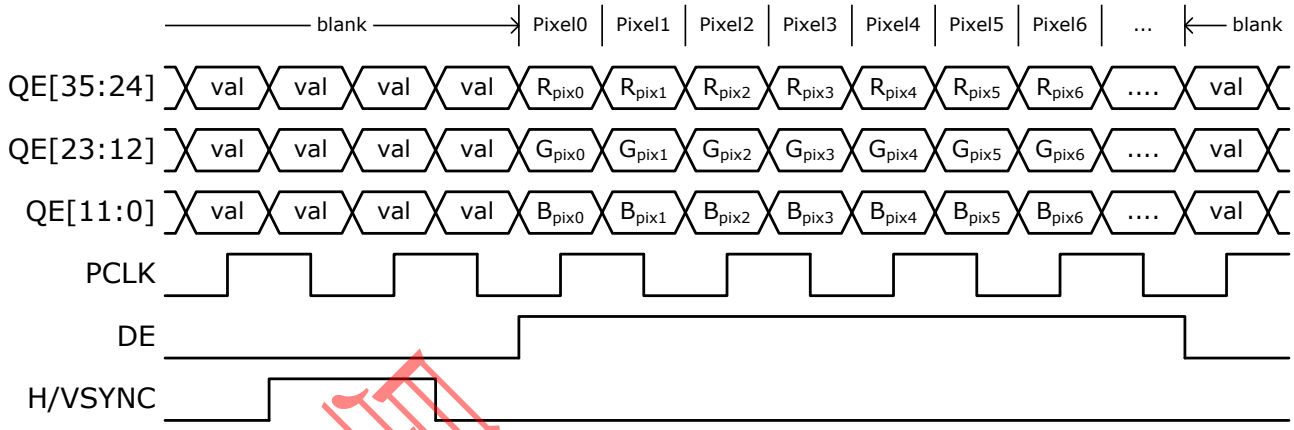
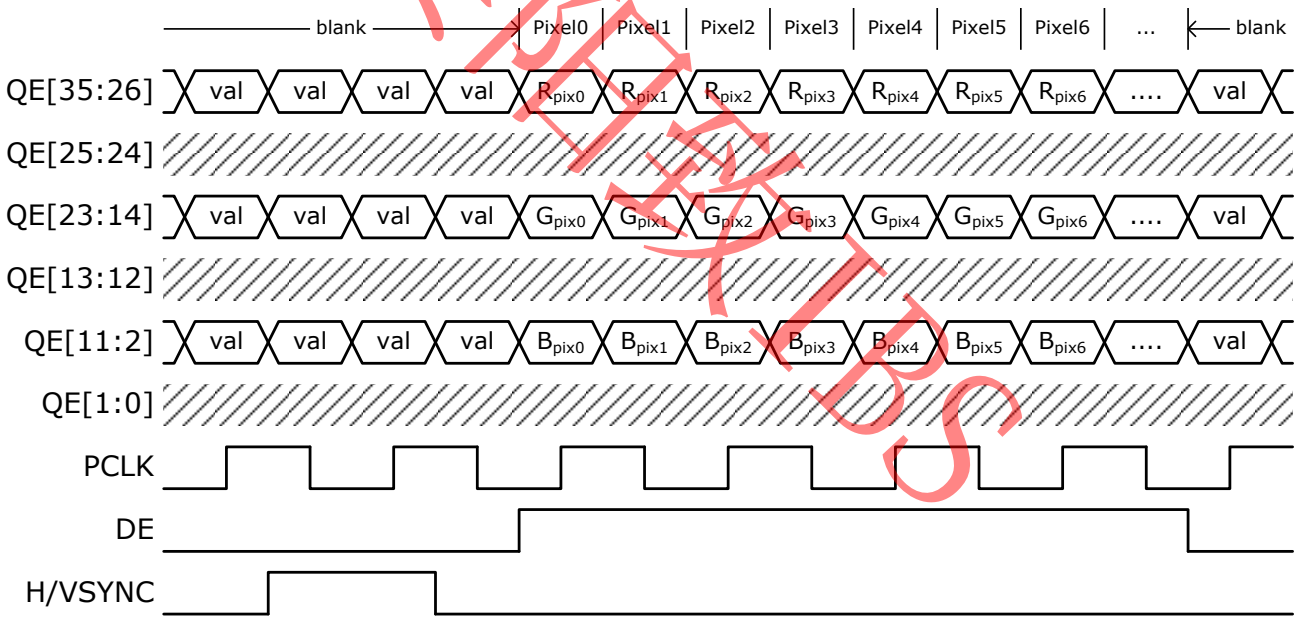


Figure 8-4 30-bit RGB 4:4:4 dual-edges triggered with 0.5X PCLK



8.1.3 12/15/18-bit RGB 4:4:4 and YCbCr 4:4:4 Using Dual-Edge Triggering

Table 8-4 Mappings of 12/15/18-bit 4:4:4 dual-edge triggered

	RGB/YCbCr					
	18-bit		15-bit		12-bit	
Pin Name	1st edge	2nd edge	1st edge	2nd edge	1st edge	2nd edge
QE0	B0/Cb0	G6/Y6	NC	NC	NC	NC
QE1	B1/Cb1	G7/Y7	NC	NC	NC	NC
QE2	B2/Cb2	G8/Y8	NC	NC	NC	NC
QE3	B3/Cb3	G9/Y9	B0/Cb0	G5/Y5	NC	NC
QE4	B4/Cb4	G10/Y10	B1/Cb1	G6/Y6	NC	NC
QE5	B5/Cb5	G11/Y11	B2/Cb2	G7/Y7	NC	NC
QE6	B6/Cb6	R0/Cr0	B3/Cb3	G8/Y8	B0/Cb0	G4/Y4
QE7	B7/Cb7	R1/Cr1	B4/Cb4	G9/Y9	B1/Cb1	G5/Y5
QE8	B8/Cb8	R2/Cr2	B5/Cb5	R0/Cr0	B2/Cb2	G6/Y6
QE9	B9/Cb9	R3/Cr3	B6/Cb6	R1/Cr1	B3/Cb3	G7/Y7
QE10	B10/Cb10	R4/Cr4	B7/Cb7	R2/Cr2	B4/Cb4	R0/Cr0
QE11	B11/Cb11	R5/Cr5	B8/Cb8	R3/Cr3	B5/Cb5	R1/Cr1
QE12	G0/Y0	R6/Cr6	B9/Cb9	R4/Cr4	B6/Cb6	R2/Cr2
QE13	G1/Y1	R7/Cr7	G0/Y0	R5/Cr5	B7/Cb7	R3/Cr3
QE14	G2/Y2	R8/Cr8	G1/Y1	R6/Cr6	G0/Y0	R4/Cr4
QE15	G3/Y3	R9/Cr9	G2/Y2	R7/Cr7	G1/Y1	R5/Cr5
QE16	G4/Y4	R10/Cr10	G3/Y3	R8/Cr8	G2/Y2	R6/Cr6
QE17	G5/Y5	R11/Cr11	G4/Y4	R9/Cr9	G3/Y3	R7/Cr7
QE18	NC	NC	NC	NC	NC	NC
QE19	NC	NC	NC	NC	NC	NC
QE20	NC	NC	NC	NC	NC	NC
QE21	NC	NC	NC	NC	NC	NC
QE22	NC	NC	NC	NC	NC	NC
QE23	NC	NC	NC	NC	NC	NC
QE24	NC	NC	NC	NC	NC	NC
QE25	NC	NC	NC	NC	NC	NC
QE26	NC	NC	NC	NC	NC	NC
QE27	NC	NC	NC	NC	NC	NC
QE28	NC	NC	NC	NC	NC	NC
QE29	NC	NC	NC	NC	NC	NC
QE30	NC	NC	NC	NC	NC	NC
QE31	NC	NC	NC	NC	NC	NC
QE32	NC	NC	NC	NC	NC	NC
QE33	NC	NC	NC	NC	NC	NC
QE34	NC	NC	NC	NC	NC	NC
QE35	NC	NC	NC	NC	NC	NC
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

In this double-edge triggering mode, PCLK frequency remains at the nominal pixel clock rate. The halved data pins, however, run at a data rate double that of the nominal pixel clock rate. Each set of data are clocked out by the rising edge and the falling edge alternatively. Overall one complete pixel is output within one PCLK period. Figure 8-5 and Figure 8-6 give examples of 18-bit and 12-bit RGB 4:4:4 Dual-Edge Triggered output respectively.

Figure 8-5 18-bit RGB 4:4:4 dual-edge triggered

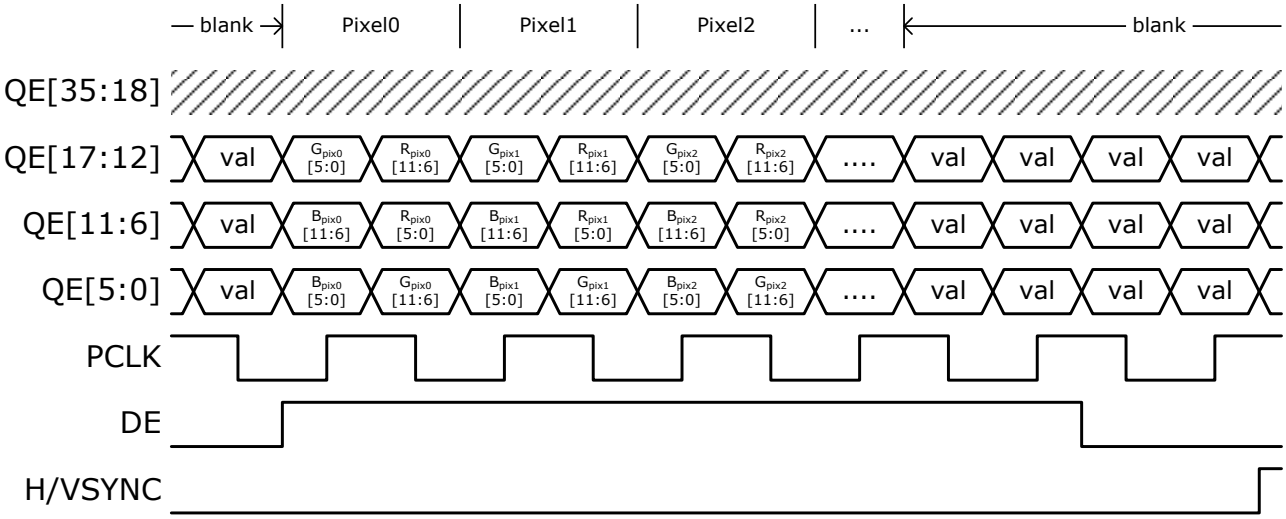
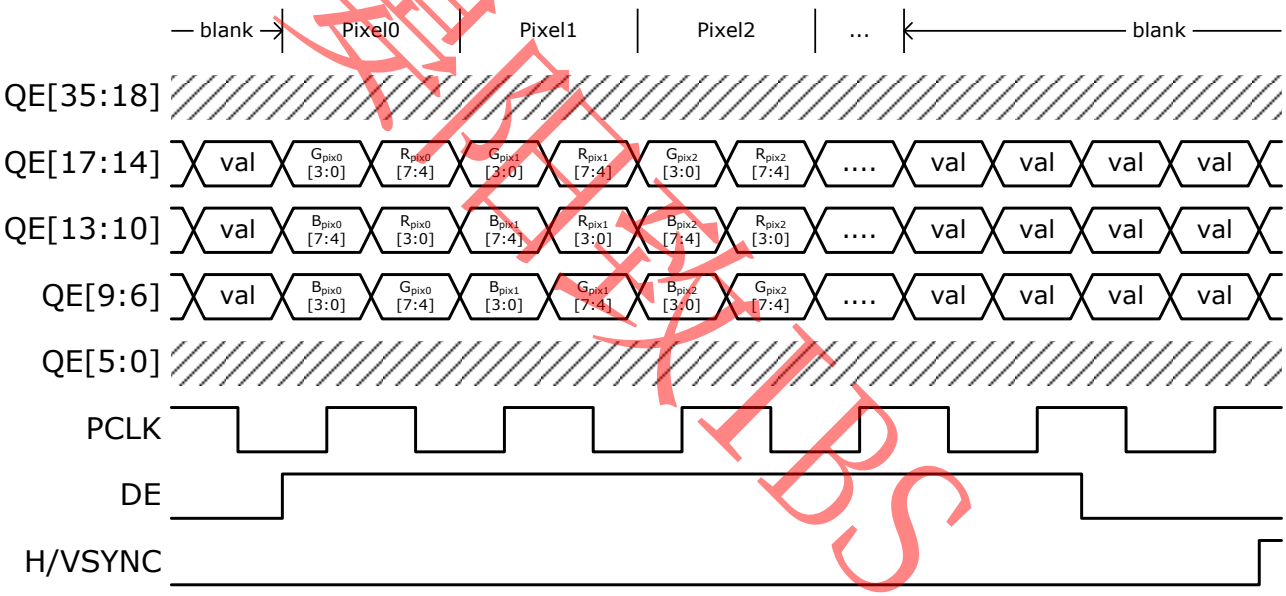


Figure 8-6 12-bit RGB 4:4:4 dual-edge triggered



8.1.4 YCbCr 4:2:2 with Separate Syncs

Table 8-5 Mappings of YCbCr 4:2:2 with separate syncs

	24-bit		20-bit		16-bit	
Pin Name	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1	Pixel#2N	Pixel#2N+1
QE0	NC	NC	NC	NC	NC	NC
QE1	NC	NC	NC	NC	NC	NC
QE2	NC	NC	NC	NC	NC	NC
QE3	NC	NC	NC	NC	NC	NC
QE4	NC	NC	NC	NC	NC	NC
QE5	NC	NC	NC	NC	NC	NC
QE6	NC	NC	NC	NC	NC	NC
QE7	NC	NC	NC	NC	NC	NC
QE8	NC	NC	NC	NC	NC	NC
QE9	NC	NC	NC	NC	NC	NC
QE10	NC	NC	NC	NC	NC	NC
QE11	NC	NC	NC	NC	NC	NC
QE12	Y0	Y0	NC	NC	NC	NC
QE13	Y1	Y1	NC	NC	NC	NC
QE14	Y2	Y2	Y0	Y0	NC	NC
QE15	Y3	Y3	Y1	Y1	NC	NC
QE16	Y4	Y4	Y2	Y2	Y0	Y0
QE17	Y5	Y5	Y3	Y3	Y1	Y1
QE18	Y6	Y6	Y4	Y4	Y2	Y2
QE19	Y7	Y7	Y5	Y5	Y3	Y3
QE20	Y8	Y8	Y6	Y6	Y4	Y4
QE21	Y9	Y9	Y7	Y7	Y5	Y5
QE22	Y10	Y10	Y8	Y8	Y6	Y6
QE23	Y11	Y11	Y9	Y9	Y7	Y7
QE24	Cb0	Cr0	NC	NC	NC	NC
QE25	Cb1	Cr1	NC	NC	NC	NC
QE26	Cb2	Cr2	Cb0	Cr0	NC	NC
QE27	Cb3	Cr3	Cb1	Cr1	NC	NC
QE28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
QE29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
QE30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
QE31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
QE32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
QE33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
QE34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
QE35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE

YCbCr 4:2:2 format does not have one complete pixel for every clock period. Luminace channel (Y) is given for every pixel, while the two chroma channels are given alternatively on every other clock period. The average bit amount of Y is twice that of Cb or Cr. Depending on the bus width, each component could take on different lengths. The DE period should contain an even number of clock periods. Figure 8-7 gives a timing example of 24-bit YCbCr 4:2:2 and Figure 8-8 gives a timing example of 16-bit YCbCr 4:2:2..

Figure 8-7 24-bit YCbCr 4:2:2 with separate syncs

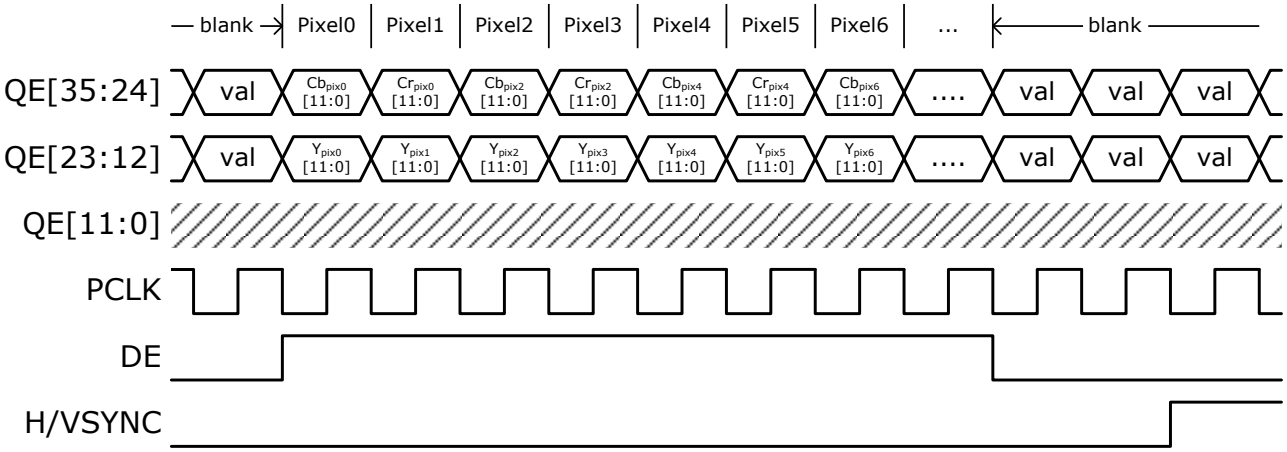
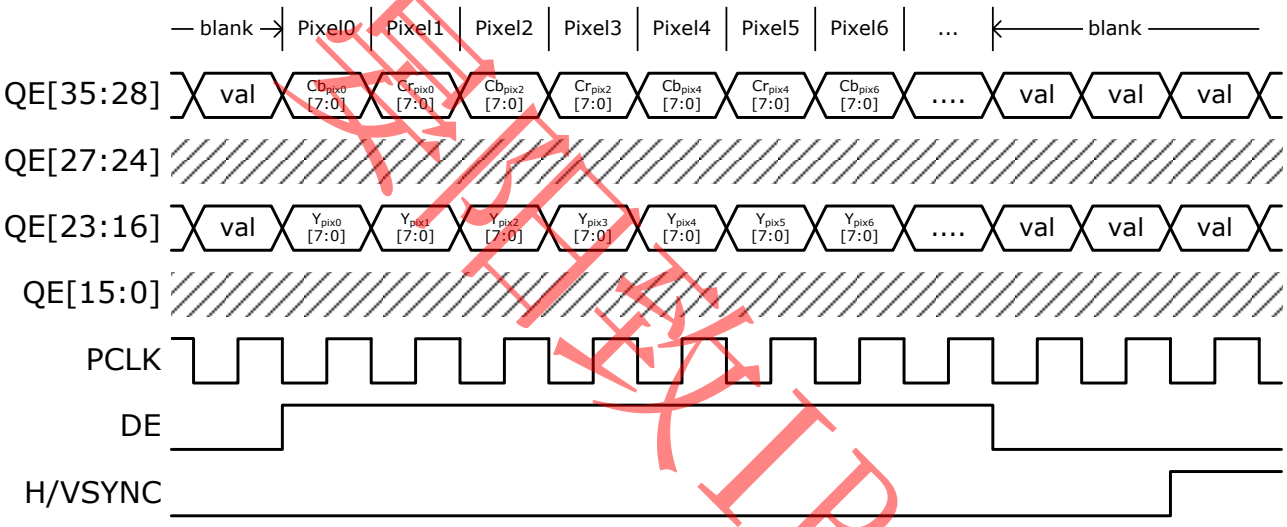


Figure 8-8 16-bit YCbCr 4:2:2 with separate syncs



8.1.5 YCbCr 4:2:2 with Separate Syncs Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of YCbCr 4:2:2 with Separate Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

Figure 8-9 24-bit YCbCr 4:2:2 with separate syncs dual-edges triggered with 0.5X PCLK

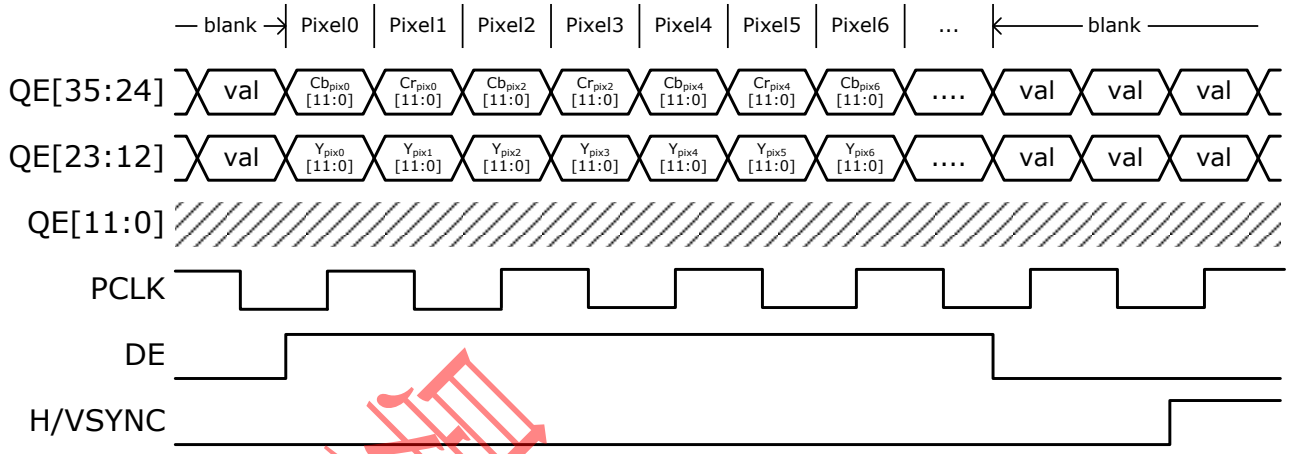
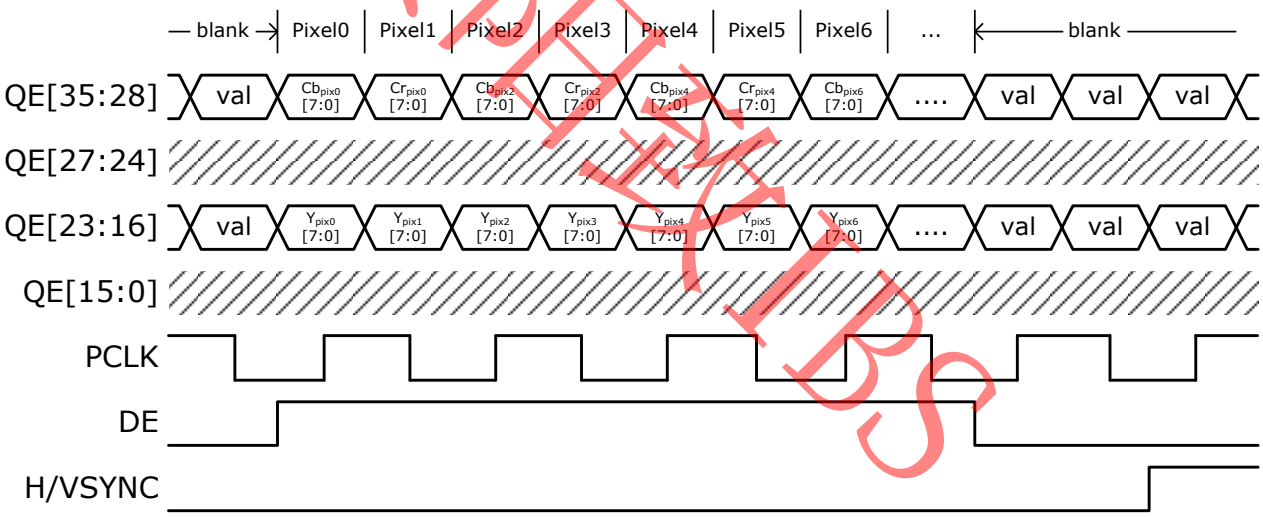


Figure 8-10 16-bit YCbCr 4:2:2 with separate syncs dual-edges triggered with 0.5X PCLK



8.1.6 YCbCr 4:2:2 with Embedded Syncs

Table 8-6 Mappings of YCbCr 4:2:2 with embedded syncs

	24-bit		20-bit		16-bit	
Pin Name	**Pixel#2N**	**Pixel#2N+1**	**Pixel#2N**	**Pixel#2N+1**	**Pixel#2N**	**Pixel#2N+1**
QE0	NC	NC	NC	NC	NC	NC
QE1	NC	NC	NC	NC	NC	NC
QE2	NC	NC	NC	NC	NC	NC
QE3	NC	NC	NC	NC	NC	NC
QE4	NC	NC	NC	NC	NC	NC
QE5	NC	NC	NC	NC	NC	NC
QE6	NC	NC	NC	NC	NC	NC
QE7	NC	NC	NC	NC	NC	NC
QE8	NC	NC	NC	NC	NC	NC
QE9	NC	NC	NC	NC	NC	NC
QE10	NC	NC	NC	NC	NC	NC
QE11	NC	NC	NC	NC	NC	NC
QE12	Y0	Y0	NC	NC	NC	NC
QE13	Y1	Y1	NC	NC	NC	NC
QE14	Y2	Y2	Y0	Y0	NC	NC
QE15	Y3	Y3	Y1	Y1	NC	NC
QE16	Y4	Y4	Y2	Y2	Y0	Y0
QE17	Y5	Y5	Y3	Y3	Y1	Y1
QE18	Y6	Y6	Y4	Y4	Y2	Y2
QE19	Y7	Y7	Y5	Y5	Y3	Y3
QE20	Y8	Y8	Y6	Y6	Y4	Y4
QE21	Y9	Y9	Y7	Y7	Y5	Y5
QE22	Y10	Y10	Y8	Y8	Y6	Y6
QE23	Y11	Y11	Y9	Y9	Y7	Y7
QE24	Cb0	Cr0	NC	NC	NC	NC
QE25	Cb1	Cr1	NC	NC	NC	NC
QE26	Cb2	Cr2	Cb0	Cr0	NC	NC
QE27	Cb3	Cr3	Cb1	Cr1	NC	NC
QE28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
QE29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
QE30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
QE31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
QE32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
QE33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
QE34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
QE35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	embedded	embedded	embedded	embedded	embedded	embedded
VSYNC	embedded	embedded	embedded	embedded	embedded	embedded
DE	embedded	embedded	embedded	embedded	embedded	embedded

Similar to YCbCr 4:2:2 with Separate Sync. The only difference is that the syncs are now non-explicit, i.e. embedded. Bus width could be 16-bit, 20-bit or 24-bit. Figure 8-11 gives a timing example of 24-bit YCbCr 4:2:2 and Figure 8-12 gives that of 16-bit. Note that while "embedded syncs" implies that neither DE nor H/VSYNC are required, the IT68051 optionally output these signals via proper register setting to ease the design for some backend processors.

Figure 8-11 24-bit YCbCr 4:2:2 with embedded syncs

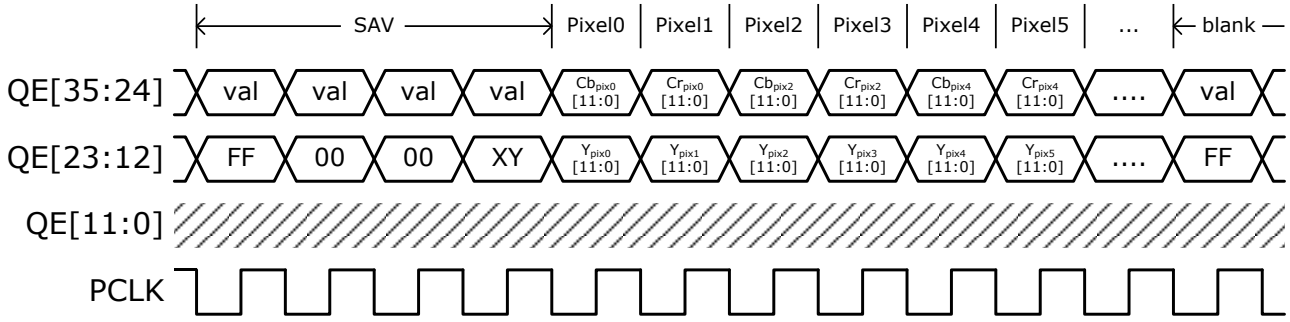
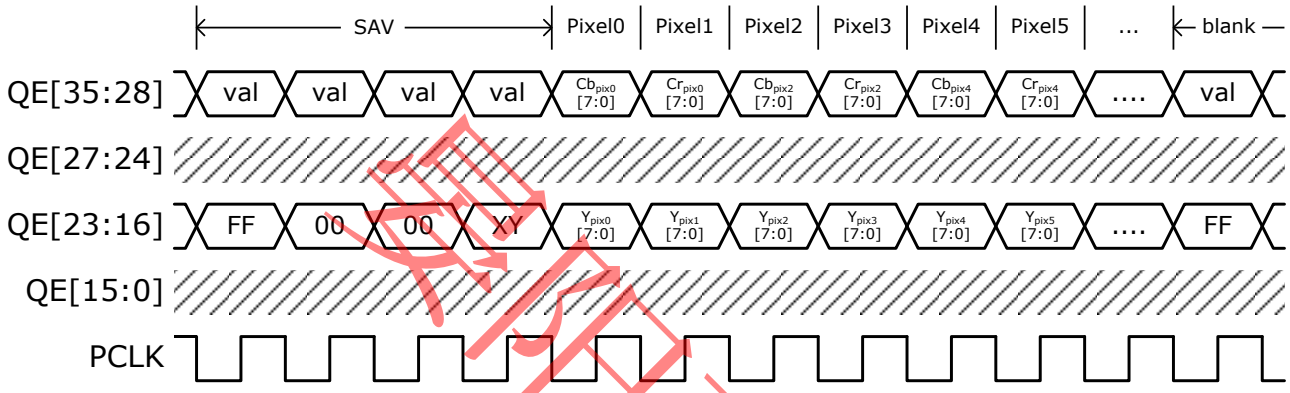


Figure 8-12 16-bit YCbCr 4:2:2 with embedded syncs



8.1.7 YCbCr 4:2:2 with Embedded Syncs Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of YCbCr 4:2:2 with Embedded Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

Figure 8-13 24-bit YCbCr 4:2:2 with embedded syncs dual-edges triggered with 0.5X PCLK

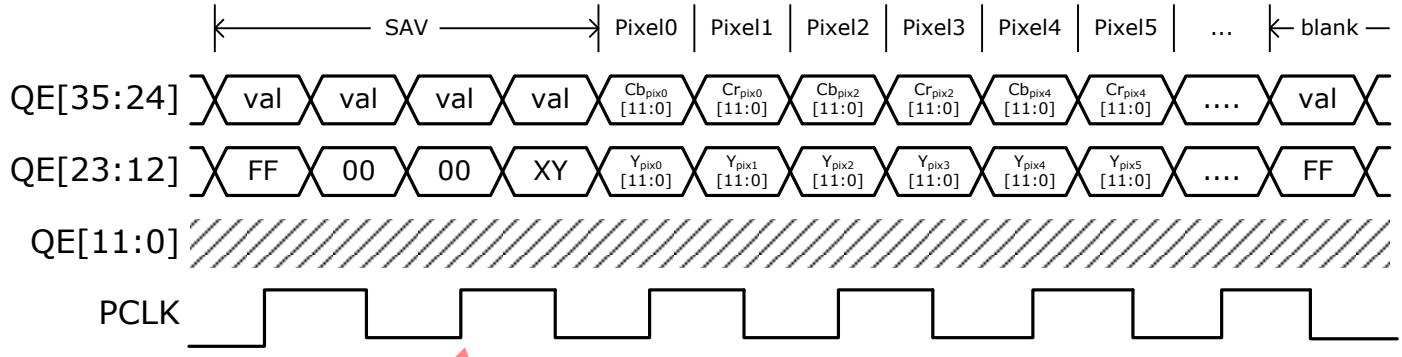
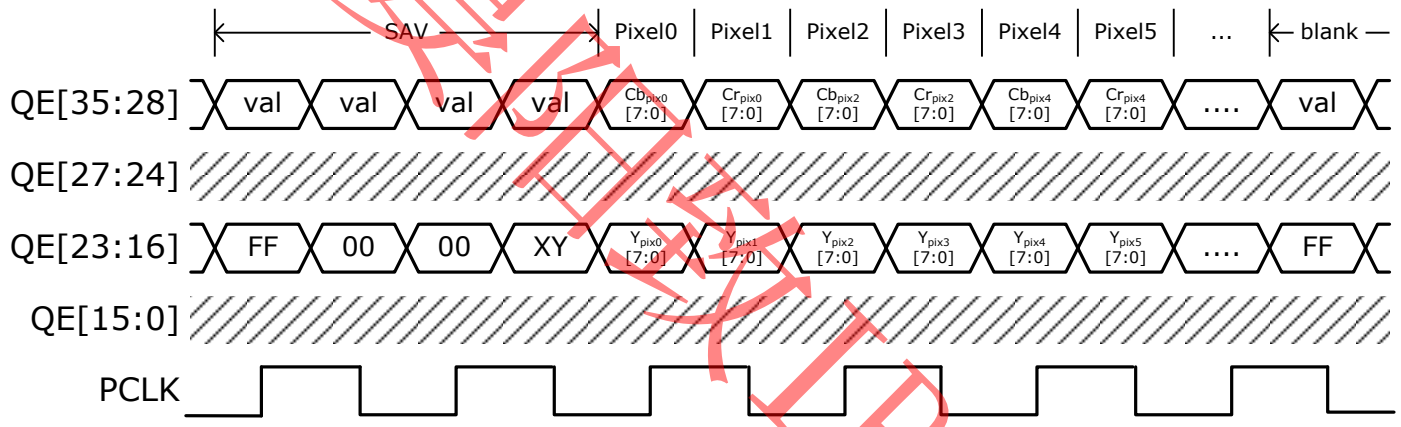


Figure 8-14 16-bit YCbCr 4:2:2 with embedded syncs dual-edges triggered with 0.5X PCLK



8.1.8 BTA1004

Table 8-7 Mappings of BTA1004

	24-bit		20-bit		16-bit	
Pin Name	**Pixel#2N**	**Pixel#2N+1**	**Pixel#2N**	**Pixel#2N+1**	**Pixel#2N**	**Pixel#2N+1**
QE0	NC	NC	NC	NC	NC	NC
QE1	NC	NC	NC	NC	NC	NC
QE2	NC	NC	NC	NC	NC	NC
QE3	NC	NC	NC	NC	NC	NC
QE4	NC	NC	NC	NC	NC	NC
QE5	NC	NC	NC	NC	NC	NC
QE6	NC	NC	NC	NC	NC	NC
QE7	NC	NC	NC	NC	NC	NC
QE8	NC	NC	NC	NC	NC	NC
QE9	NC	NC	NC	NC	NC	NC
QE10	NC	NC	NC	NC	NC	NC
QE11	NC	NC	NC	NC	NC	NC
QE12	Y0	Y0	NC	NC	NC	NC
QE13	Y1	Y1	NC	NC	NC	NC
QE14	Y2	Y2	Y0	Y0	NC	NC
QE15	Y3	Y3	Y1	Y1	NC	NC
QE16	Y4	Y4	Y2	Y2	Y0	Y0
QE17	Y5	Y5	Y3	Y3	Y1	Y1
QE18	Y6	Y6	Y4	Y4	Y2	Y2
QE19	Y7	Y7	Y5	Y5	Y3	Y3
QE20	Y8	Y8	Y6	Y6	Y4	Y4
QE21	Y9	Y9	Y7	Y7	Y5	Y5
QE22	Y10	Y10	Y8	Y8	Y6	Y6
QE23	Y11	Y11	Y9	Y9	Y7	Y7
QE24	Cb0	Cr0	NC	NC	NC	NC
QE25	Cb1	Cr1	NC	NC	NC	NC
QE26	Cb2	Cr2	Cb0	Cr0	NC	NC
QE27	Cb3	Cr3	Cb1	Cr1	NC	NC
QE28	Cb4	Cr4	Cb2	Cr2	Cb0	Cr0
QE29	Cb5	Cr5	Cb3	Cr3	Cb1	Cr1
QE30	Cb6	Cr6	Cb4	Cr4	Cb2	Cr2
QE31	Cb7	Cr7	Cb5	Cr5	Cb3	Cr3
QE32	Cb8	Cr8	Cb6	Cr6	Cb4	Cr4
QE33	Cb9	Cr9	Cb7	Cr7	Cb5	Cr5
QE34	Cb10	Cr10	Cb8	Cr8	Cb6	Cr6
QE35	Cb11	Cr11	Cb9	Cr9	Cb7	Cr7
HSYNC	embedded	embedded	embedded	embedded	embedded	embedded
VSYNC	embedded	embedded	embedded	embedded	embedded	embedded
DE	embedded	embedded	embedded	embedded	embedded	embedded

BTA1004 data mapping format is the same as YCbCr422 with embedded syncs. The only difference is the mapping of SAV.

Figure 8-15 24-bit BTA1004

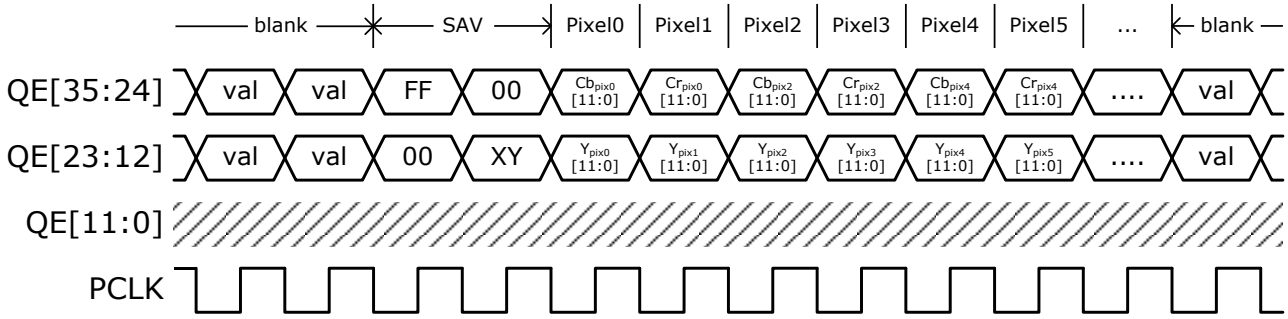
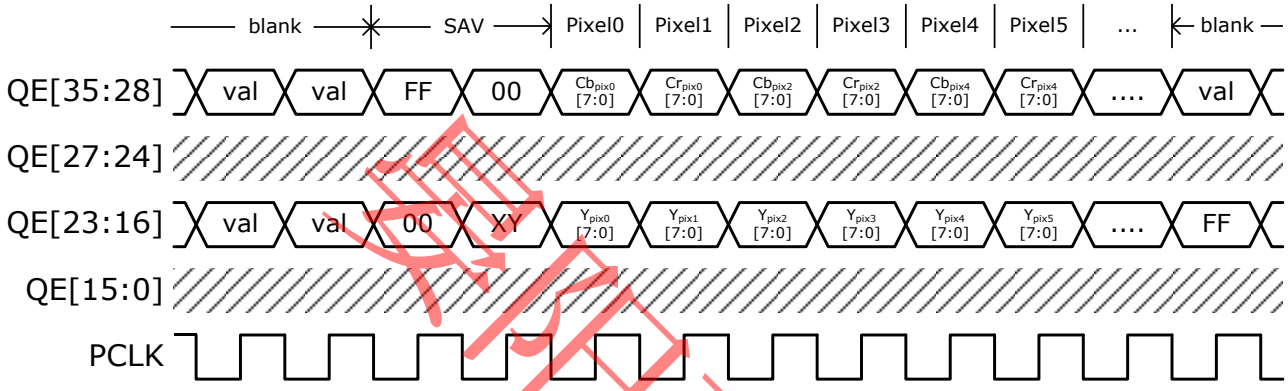


Figure 8-16 16-bit BTA1004



8.1.9 BTA1004 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of BTA1004. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

Figure 8-17 24-bit BTA1004 dual-edges triggered with 0.5X PCLK

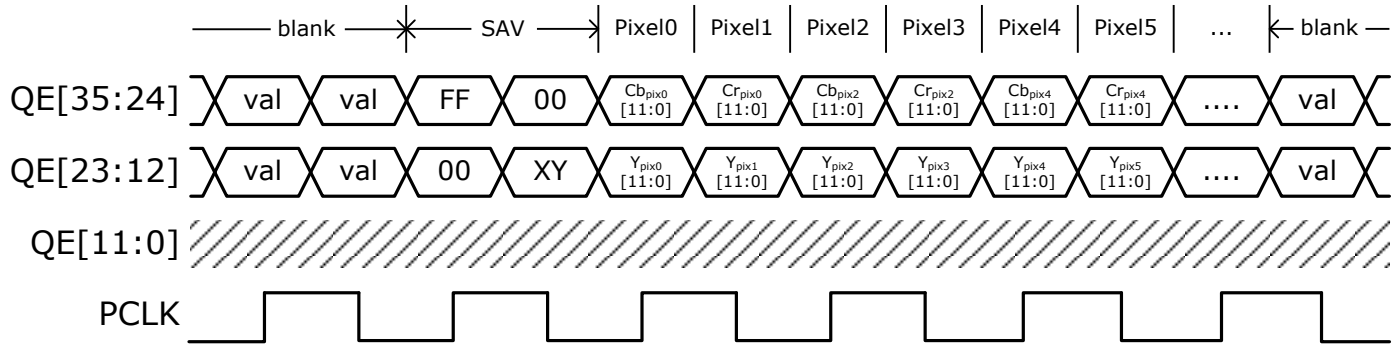
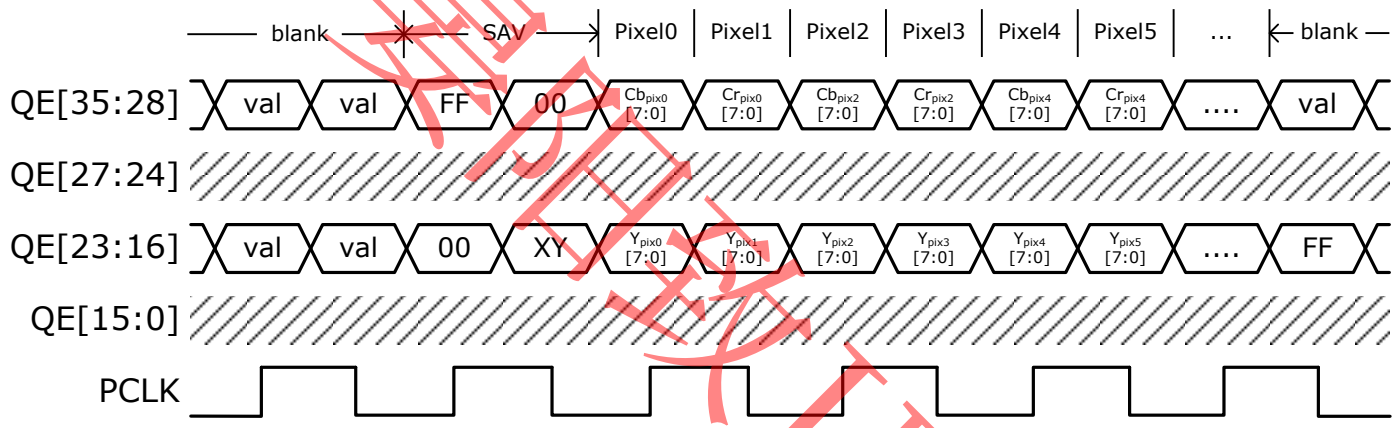


Figure 8-18 16-bit BTA1004 dual-edges triggered with 0.5X PCLK



8.2 Dual Pixel Mode

There are only one IO mode when IT68051 operated in dual pixel mode. Defined QE[9:0] = PixelA_B, QE[19:10] = PixelA_G, QE[29:20] = PixelA_R, QE[39:30] = PixelB_B, QE[49:40] = PixelB_G, QE[59:50] = PixelB_R. The mapping between QEx and QDx as Table 8-8.

Table 8-8 IO mappings for dual pixel mode

PIXEL A	QE0	QD0
	QE1	QD1
	QE2	QD2
	QE3	QD3
	QE4	QD4
	QE5	QD5
	QE6	QD6
	QE7	QD7
	QE8	QD8
	QE9	QD9
	QE10	QD10
	QE11	QD11
	QE12	QD12
	QE13	QD13
	QE14	QD14
	QE15	QD15
	QE16	QD16
	QE17	QD17
	QE18	QD18
	QE19	QD19
	QE20	QD20
	QE21	QD21
	QE22	QD22
	QE23	QD23
	QE24	QD24
	QE25	QD25
	QE26	QD26
	QE27	QD27
	QE28	QD28
	QE29	QD29
	HSYNC	HSYNC
	VSYNC	VSYNC
	DE	DE

PIXEL B	QE30	QD30
	QE31	QD31
	QE32	QD32
	QE33	QD33
	QE34	QD34
	QE35	QD35
	QE36	QD36
	QE37	QD37
	QE38	QD38
	QE39	QD39
	QE40	QD40
	QE41	QD41
	QE42	QD42
	QE43	QD43
	QE44	QD44
	QE45	QD45
	QE46	QD46
	QE47	QD47
	QE48	QD48
	QE49	QD49
	QE50	QD50
	QE51	QD51
	QE52	QD52
	QE53	QD53
	QE54	QD54
	QE55	QD55
	QE56	QD56
	QE57	QD57
	QE58	QD58
	QE59	QD59
	HSYNC	HSYNC
	VSYNC	VSYNC
	DE	DE

8.2.1 RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs

Table 8-9 RGB & YCbCr 4:4:4 Mappings

	RGB444		YCbCr444			RGB444		YCbCr444	
Pin Name	30-bit	24-bit	30-bit	24-bit	Pin Name	30-bit	24-bit	30-bit	24-bit
QE0	A_B0	NC	A_Cb0	NC	QE30	B_B0	NC	B_Cb0	NC
QE1	A_B1	NC	A_Cb1	NC	QE31	B_B1	NC	B_Cb1	NC
QE2	A_B2	A_B0	A_Cb2	A_Cb0	QE32	B_B2	B_B0	B_Cb2	B_Cb0
QE3	A_B3	A_B1	A_Cb3	A_Cb1	QE33	B_B3	B_B1	B_Cb3	B_Cb1
QE4	A_B4	A_B2	A_Cb4	A_Cb2	QE34	B_B4	B_B2	B_Cb4	B_Cb2
QE5	A_B5	A_B3	A_Cb5	A_Cb3	QE35	B_B5	B_B3	B_Cb5	B_Cb3
QE6	A_B6	A_B4	A_Cb6	A_Cb4	QE36	B_B6	B_B4	B_Cb6	B_Cb4
QE7	A_B7	A_B5	A_Cb7	A_Cb5	QE37	B_B7	B_B5	B_Cb7	B_Cb5
QE8	A_B8	A_B6	A_Cb8	A_Cb6	QE38	B_B8	B_B6	B_Cb8	B_Cb6
QE9	A_B9	A_B7	A_Cb9	A_Cb7	QE39	B_B9	B_B7	B_Cb9	B_Cb7
QE10	A_G0	NC	A_Y0	NC	QE40	B_G0	NC	B_Y0	NC
QE11	A_G1	NC	A_Y1	NC	QE41	B_G1	NC	B_Y1	NC
QE12	A_G2	A_G0	A_Y2	A_Y0	QE42	B_G2	B_G0	B_Y2	B_Y0
QE13	A_G3	A_G1	A_Y3	A_Y1	QE43	B_G3	B_G1	B_Y3	B_Y1
QE14	A_G4	A_G2	A_Y4	A_Y2	QE44	B_G4	B_G2	B_Y4	B_Y2
QE15	A_G5	A_G3	A_Y5	A_Y3	QE45	B_G5	B_G3	B_Y5	B_Y3
QE16	A_G6	A_G4	A_Y6	A_Y4	QE46	B_G6	B_G4	B_Y6	B_Y4
QE17	A_G7	A_G5	A_Y7	A_Y5	QE47	B_G7	B_G5	B_Y7	B_Y5
QE18	A_G8	A_G6	A_Y8	A_Y6	QE48	B_G8	B_G6	B_Y8	B_Y6
QE19	A_G9	A_G7	A_Y9	A_Y7	QE49	B_G9	B_G7	B_Y9	B_Y7
QE20	A_R0	NC	A_Cr0	NC	QE50	B_R0	NC	B_Cr0	NC
QE21	A_R1	NC	A_Cr1	NC	QE51	B_R1	NC	B_Cr1	NC
QE22	A_R2	A_R0	A_Cr2	A_Cr0	QE52	B_R2	B_R0	B_Cr2	B_Cr0
QE23	A_R3	A_R1	A_Cr3	A_Cr1	QE53	B_R3	B_R1	B_Cr3	B_Cr1
QE24	A_R4	A_R2	A_Cr4	A_Cr2	QE54	B_R4	B_R2	B_Cr4	B_Cr2
QE25	A_R5	A_R3	A_Cr5	A_Cr3	QE55	B_R5	B_R3	B_Cr5	B_Cr3
QE26	A_R6	A_R4	A_Cr6	A_Cr4	QE56	B_R6	B_R4	B_Cr6	B_Cr4
QE27	A_R7	A_R5	A_Cr7	A_Cr5	QE57	B_R7	B_R5	B_Cr7	B_Cr5
QE28	A_R8	A_R6	A_Cr8	A_Cr6	QE58	B_R8	B_R6	B_Cr8	B_Cr6
QE29	A_R9	A_R7	A_Cr9	A_Cr7	QE59	B_R9	B_R7	B_Cr9	B_Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE	DE	DE	DE	DE

The output video clock (PCLK) will be halved in frequency. There are two pixels will be latched in PCLK rising edge.

Figure 8-19 30-bit RGB 4:4:4 Timing Diagram for Dual Pixel Mode

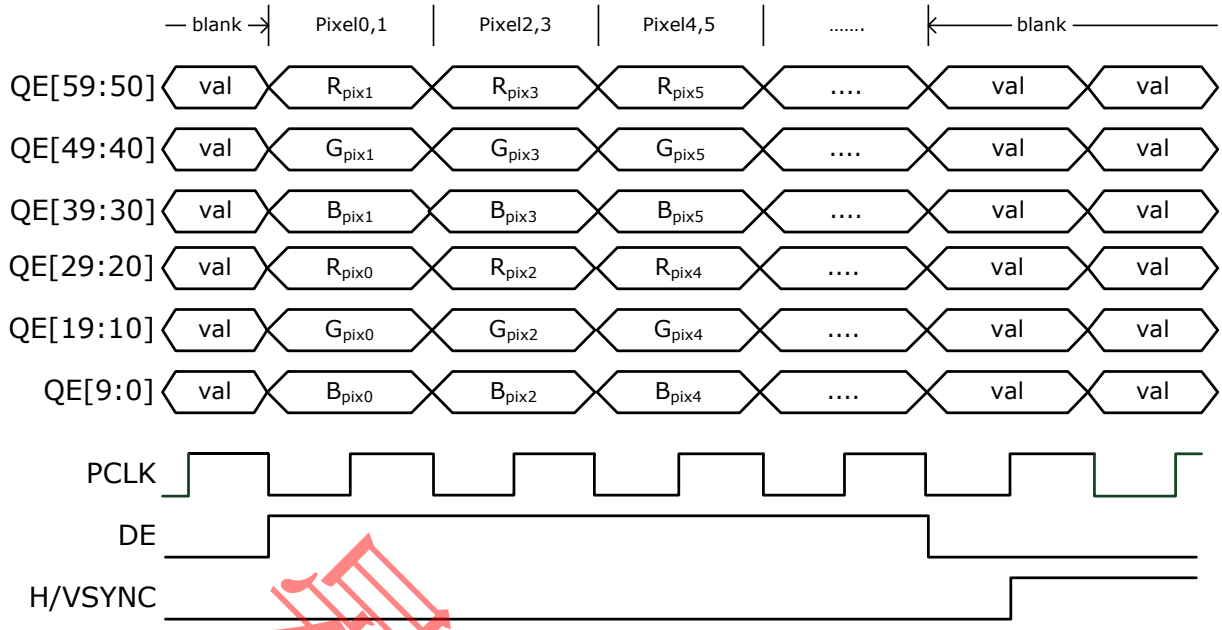
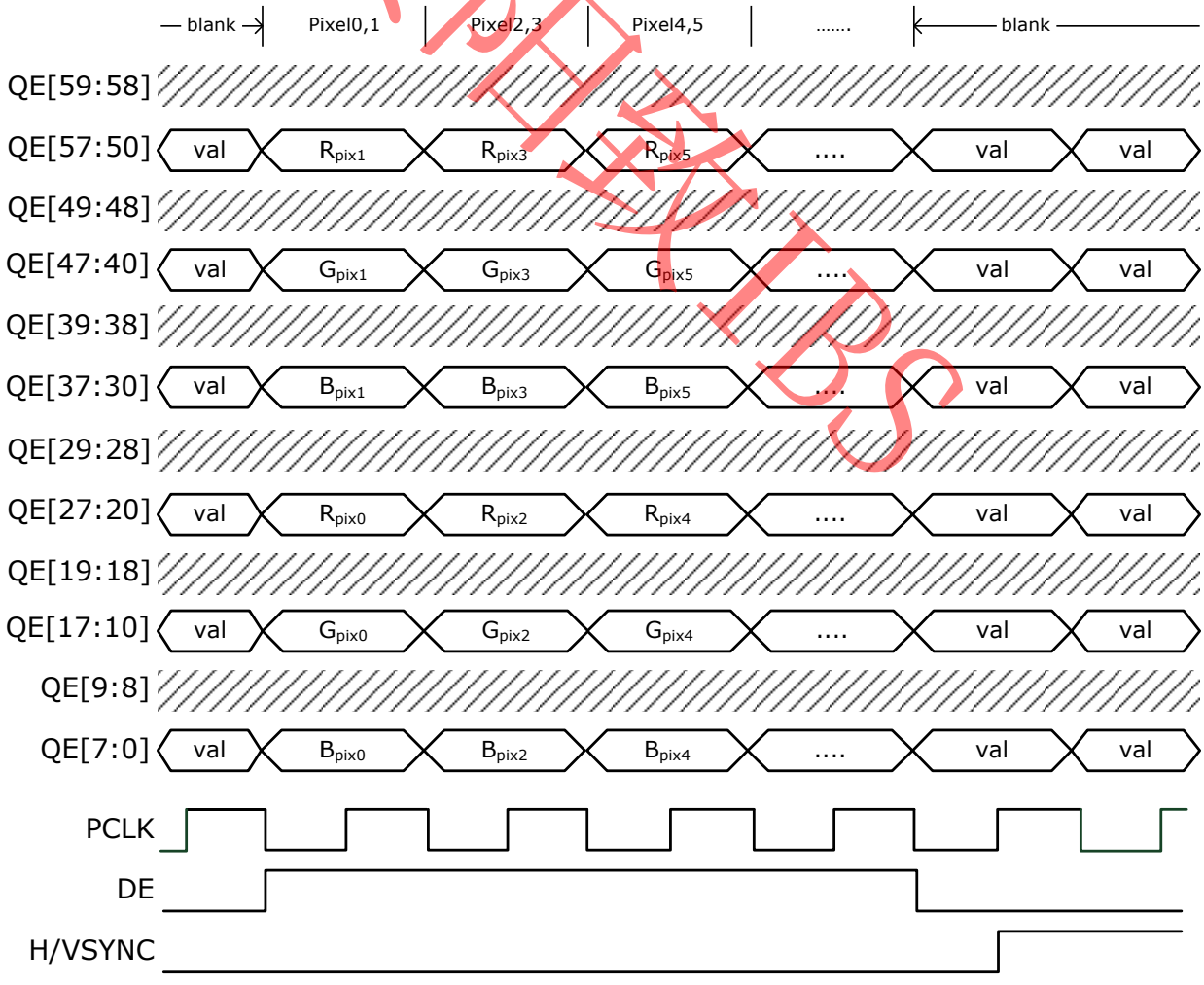


Figure 8-20 24-bit RGB 4:4:4 Timing Diagram for Dual Pixel Mode



8.2.2 RGB 4:4:4 and YCbCr 4:4:4 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.25X PCLK.

Figure 8-21 30-bit RGB 4:4:4 timing diagram for dual pixel dual edge mode

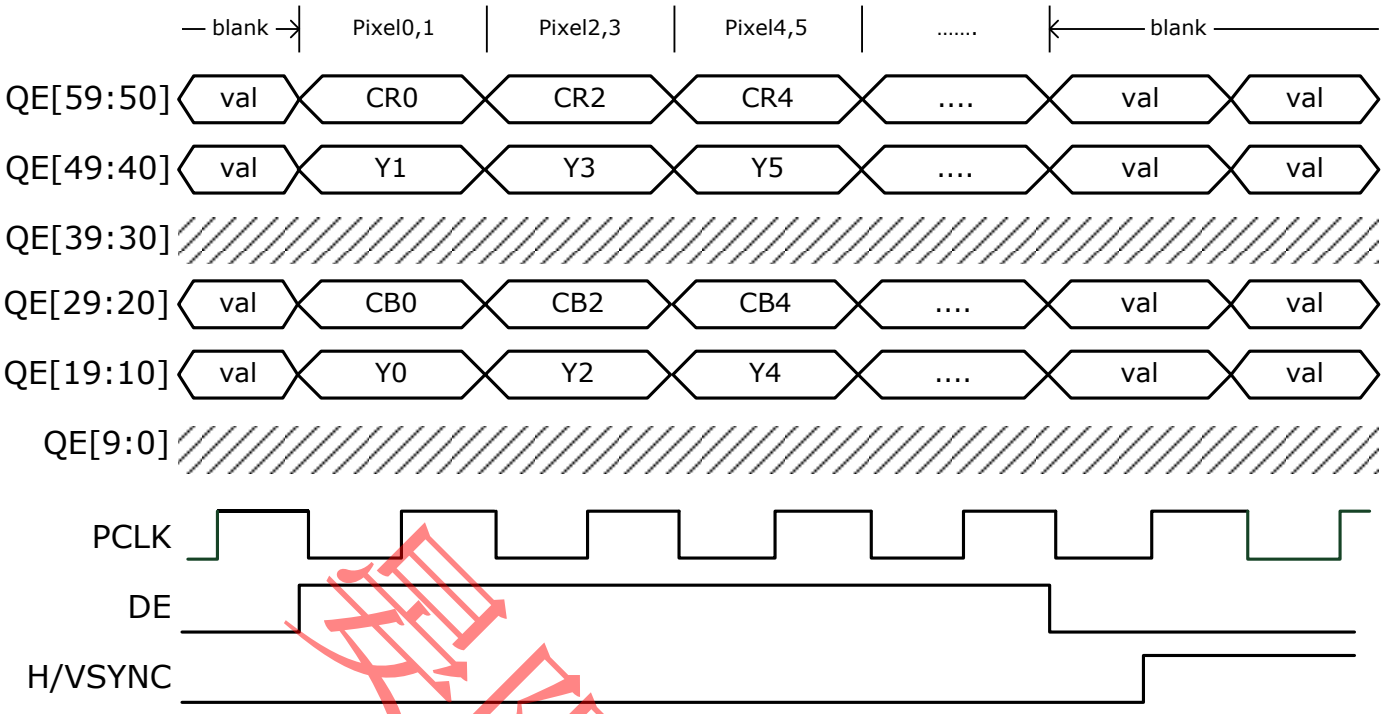
8.2.3 YCbCr 4:2:2 with Separate Syncs

Table 8-10 YCbCr 4:2:2 mappings

	YCbCr444			YCbCr444	
Pin Name	**30-bit**	**24-bit**	**Pin Name**	**30-bit**	**24-bit**
QE0	NC	NC	QE30	NC	NC
QE1	NC	NC	QE31	NC	NC
QE2	NC	NC	QE32	NC	NC
QE3	NC	NC	QE33	NC	NC
QE4	NC	NC	QE34	NC	NC
QE5	NC	NC	QE35	NC	NC
QE6	NC	NC	QE36	NC	NC
QE7	NC	NC	QE37	NC	NC
QE8	NC	NC	QE38	NC	NC
QE9	NC	NC	QE39	NC	NC
QE10	A_Y0	NC	QE40	B_Y0	NC
QE11	A_Y1	NC	QE41	B_Y1	NC
QE12	A_Y2	A_Y0	QE42	B_Y2	B_Y0
QE13	A_Y3	A_Y1	QE43	B_Y3	B_Y1
QE14	A_Y4	A_Y2	QE44	B_Y4	B_Y2
QE15	A_Y5	A_Y3	QE45	B_Y5	B_Y3
QE16	A_Y6	A_Y4	QE46	B_Y6	B_Y4
QE17	A_Y7	A_Y5	QE47	B_Y7	B_Y5
QE18	A_Y8	A_Y6	QE48	B_Y8	B_Y6
QE19	A_Y9	A_Y7	QE49	B_Y9	B_Y7
QE20	A_Cr0	NC	QE50	B_Cr0	NC
QE21	A_Cr1	NC	QE51	B_Cr1	NC
QE22	A_Cr2	A_Cr0	QE52	B_Cr2	B_Cr0
QE23	A_Cr3	A_Cr1	QE53	B_Cr3	B_Cr1
QE24	A_Cr4	A_Cr2	QE54	B_Cr4	B_Cr2
QE25	A_Cr5	A_Cr3	QE55	B_Cr5	B_Cr3
QE26	A_Cr6	A_Cr4	QE56	B_Cr6	B_Cr4
QE27	A_Cr7	A_Cr5	QE57	B_Cr7	B_Cr5
QE28	A_Cr8	A_Cr6	QE58	B_Cr8	B_Cr6
QE29	A_Cr9	A_Cr7	QE59	B_Cr9	B_Cr7
HSYNC	HSYNC	HSYNC	HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC	VSYNC	VSYNC	VSYNC
DE	DE	DE	DE	DE	DE

The output video clock (PCLK) will be halved in frequency. There are two pixels will be latched in PCLK rising edge.

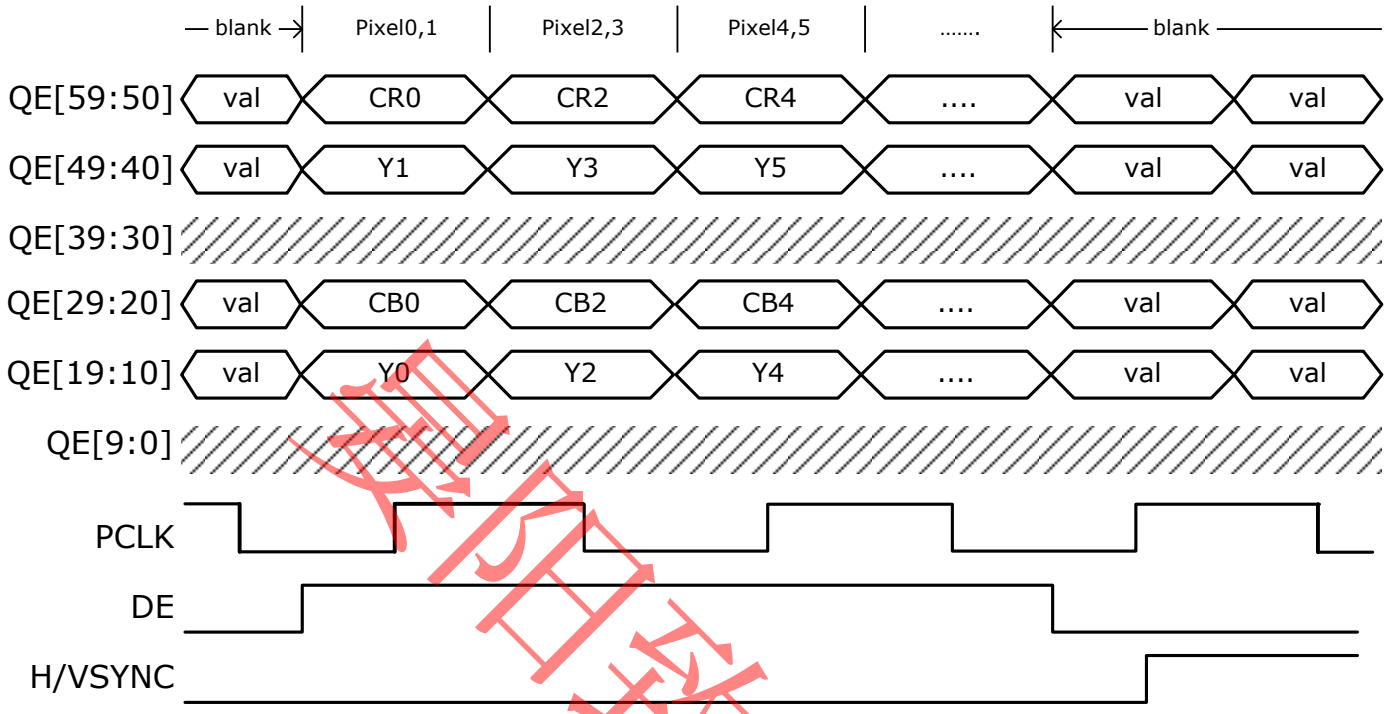
Figure 8-22 20-bit YCbCr 4:2:2 Timing Diagram for Dual Pixel Mode



8.2.4 YCbCr 4:2:2 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of YCbCr 4:2:2 with Separate Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.25X PCLK.

Figure 8-23 20-bit YCbCr 4:2:2 Timing Diagram for Dual Pixel Dual Edge Mode



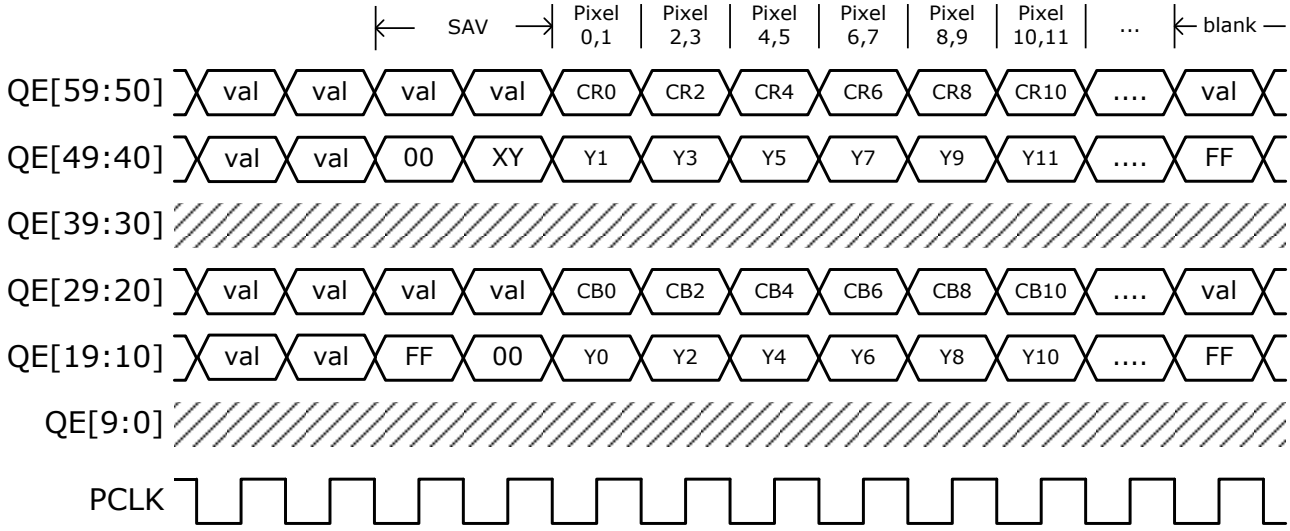
8.2.5 YCbCr 4:2:2 with Embedded Syncs

Table 8-11 YCbCr 4:2:2 Mappings with embedded syncs

	YCbCr444			YCbCr444	
Pin Name	**30-bit**	**24-bit**	**Pin Name**	**30-bit**	**24-bit**
QE0	NC	NC	QE30	NC	NC
QE1	NC	NC	QE31	NC	NC
QE2	NC	NC	QE32	NC	NC
QE3	NC	NC	QE33	NC	NC
QE4	NC	NC	QE34	NC	NC
QE5	NC	NC	QE35	NC	NC
QE6	NC	NC	QE36	NC	NC
QE7	NC	NC	QE37	NC	NC
QE8	NC	NC	QE38	NC	NC
QE9	NC	NC	QE39	NC	NC
QE10	A_Y0	NC	QE40	B_Y0	NC
QE11	A_Y1	NC	QE41	B_Y1	NC
QE12	A_Y2	A_Y0	QE42	B_Y2	B_Y0
QE13	A_Y3	A_Y1	QE43	B_Y3	B_Y1
QE14	A_Y4	A_Y2	QE44	B_Y4	B_Y2
QE15	A_Y5	A_Y3	QE45	B_Y5	B_Y3
QE16	A_Y6	A_Y4	QE46	B_Y6	B_Y4
QE17	A_Y7	A_Y5	QE47	B_Y7	B_Y5
QE18	A_Y8	A_Y6	QE48	B_Y8	B_Y6
QE19	A_Y9	A_Y7	QE49	B_Y9	B_Y7
QE20	A_Cr0	NC	QE50	B_Cr0	NC
QE21	A_Cr1	NC	QE51	B_Cr1	NC
QE22	A_Cr2	A_Cr0	QE52	B_Cr2	B_Cr0
QE23	A_Cr3	A_Cr1	QE53	B_Cr3	B_Cr1
QE24	A_Cr4	A_Cr2	QE54	B_Cr4	B_Cr2
QE25	A_Cr5	A_Cr3	QE55	B_Cr5	B_Cr3
QE26	A_Cr6	A_Cr4	QE56	B_Cr6	B_Cr4
QE27	A_Cr7	A_Cr5	QE57	B_Cr7	B_Cr5
QE28	A_Cr8	A_Cr6	QE58	B_Cr8	B_Cr6
QE29	A_Cr9	A_Cr7	QE59	B_Cr9	B_Cr7
HSYNC	embedded	embedded	embedded	embedded	embedded
VSYNC	embedded	embedded	embedded	embedded	embedded
DE	embedded	embedded	embedded	embedded	embedded

The output video clock (PCLK) will be halved in frequency. There are two pixels will be latched in PCLK rising edge.

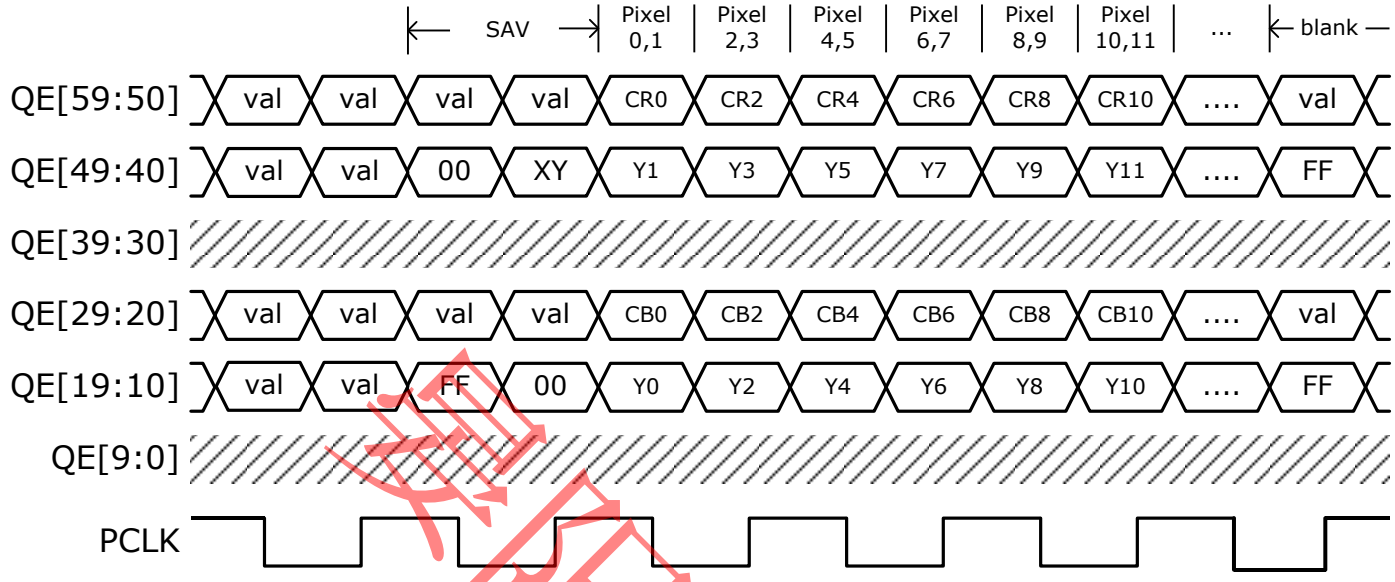
Figure 8-24 20-bit YCbCr 4:2:2 timing diagram for dual pixel mode with embedded sync



8.2.6 YCbCr 4:2:2 with Embed Sync Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of YCbCr 4:2:2 with Embedded Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.25X PCLK.

Figure 8-25 20-bit YCbCr 4:2:2 timing diagram for dual pixel dual edge mode with embedded sync



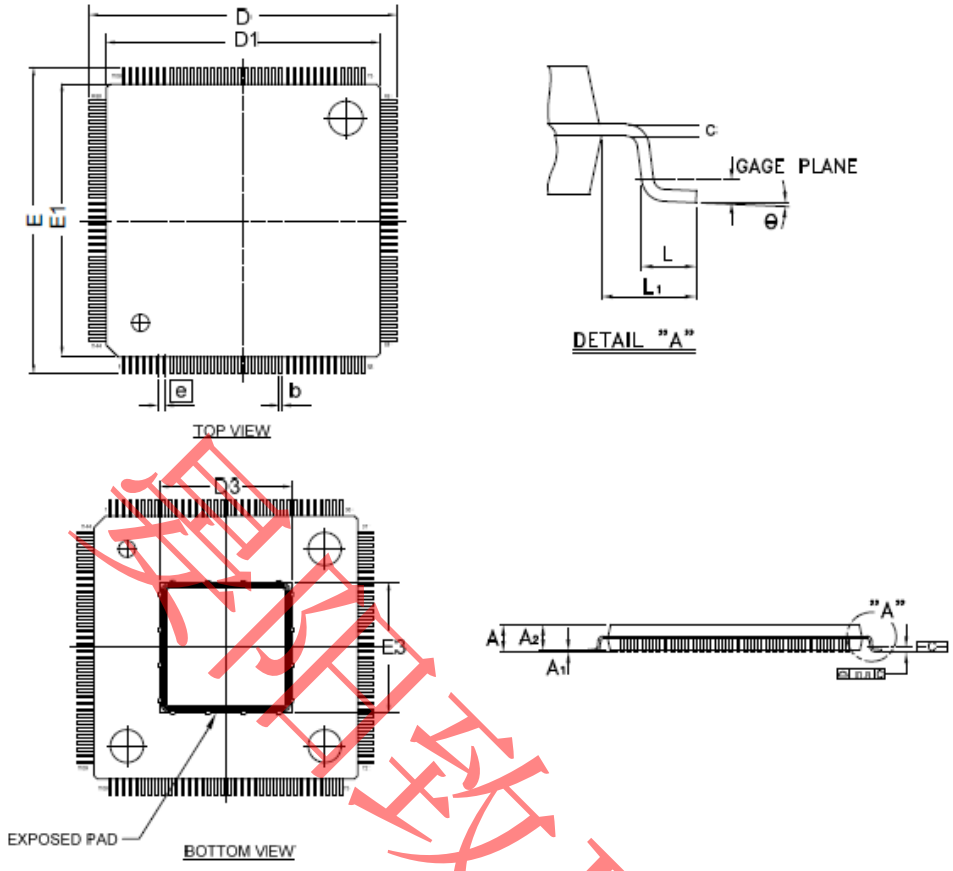
9. System Design Consideration

As a high-performance receiver/transmitter, ITE's RX/TX is capable of receiving/transmitting those signals that are attenuated and degraded by the HDMI/MHL cables. These signals are usually very small in amplitudes in addition to the distortion that the cable inflicts on them. The analog front-end of ITE's RX/TX is designed to combat environment noises as well as interference to some degree. However, to get the optimum performance, the system designers should follow the guideline when designing the application circuits and PCB layout.

Please refer the "IT68051 HW Design Guidelines" document for detail description.

10. Package Information

Figure 10-1 144-pin TQFP with Epad Package Dimensions



Symbol	Dimensions in inches			Dimensions in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	-	-	0.047	-	-	1.20
A1	0.002	-	0.006	0.05	-	0.15
A2	0.037	0.039	0.041	0.95	1.00	1.05
b	0.005	0.006	0.009	0.13	0.16	0.23
c	0.004	-	0.008	0.09	-	0.20
D/E	0.709 BSC			18.00 BSC		
D_1/E_1	0.630 BSC			16.00 BSC		
D_3/E_3	0.315 BSC			8.00 BSC		
e	0.016 BSC			0.40 BSC		
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	0.039 REF.			1.0 REF.		
θ	0°	-	7°	0°	-	7°

Notes:

1. Dimensions D_1 and E_1 do not include mold protrusion. But mold mismatch is included.
2. Dimensions b does not include dambar protrusion.
3. Controlling dimension: millimeter

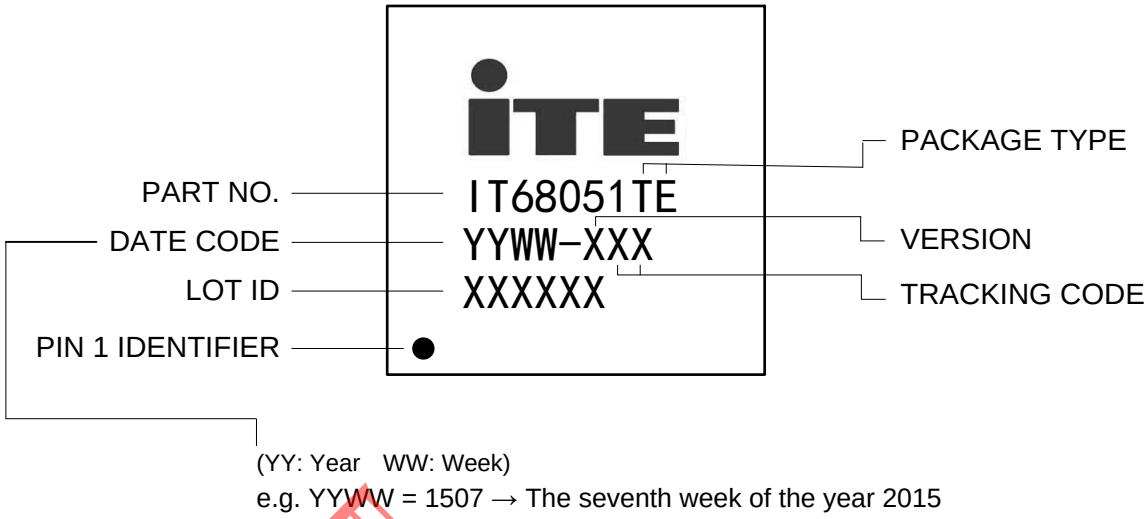
DI-E(315*315MIL)-TQFP144(16*16)v0

11. Ordering Information

Part No.	Package
IT68051TE	TQFP 144

All green components provided are in compliance with RoHS, and Halogen-Free.

12. Top Marking Information



(YY: Year WW: Week)

e.g. YYWW = 1507 → The seventh week of the year 2015

ITE TECH. INC. TERMS AND CONDITIONS OF SALE (Rev: 2013)

0. PARTIES

ITE Tech. Inc. ("Seller") is a company headquartered in Taiwan, Republic of China, and incorporated under laws of Republic of China, Buyer is a company or an entity, purchasing product from ITE Tech. Inc.

1. ACCEPTANCE OF TERMS

BUYER ACCEPTS THESE TERMS (i) BY WRITTEN ACCEPTANCE (BY PURCHASE ORDER OR OTHERWISE), OR (ii) BY FAILURE TO RETURN GOODS DESCRIBED ON THE FACE OF THE PACKING LIST WITHIN FIVE DAYS OF THEIR DELIVERY.

2. DELIVERY

(a) Otherwise specified in the order agreed by Seller, delivery will be made Free Carrier (Incoterms), Seller's warehouse, Science-Based Industrial Park, Hsinchu, Taiwan.
(b) Title to the goods and the entire risk will pass to Buyer upon delivery to carrier.
(c) Shipments are subject to availability. Seller shall make every reasonable effort to meet the date(s) quoted or acknowledged; and if Seller makes such effort, Seller will not be liable for any delays.

3. TERMS OF PAYMENT

(a) Terms are as stated on Seller's quotation, or if none are stated, net thirty (30) days. Accounts past due will incur a monthly charge at the rate of one percent (1%) per month (or, if less, the maximum allowed by applicable law) to cover servicing costs.
(b) Seller reserves the right to change credit terms at any time in its sole discretion.

4. LIMITED WARRANTY

(a) Seller warrants that the goods sold will be free from defects in material and workmanship and comply with Seller's applicable published specifications for a period of ninety (90) days from the date of Seller's delivery. Within the warranty period and by obtaining a return number from Seller, Buyer may request replacement or repair for defective goods.
(b) Goods or parts which have been subject to abuse (including without limitation repeated or extended exposure to conditions at or near the limits of applicable absolute ratings) misuse, accident, alteration, neglect, or unauthorized repair or improper application are not covered by any warranty. No warranty is made with respect to custom products or goods produced to Buyer's specifications (unless specifically stated in a writing signed by Seller).
(c) No warranty is made with respect to goods used in devices intended for use in applications where failure to perform when properly used can reasonably be expected to result in significant injury (including, without limitation, navigation, aviation or nuclear equipment, or for surgical implant or to support or sustain life) and Buyer agrees to indemnify, defend, and hold harmless Seller from all claims, damages and liabilities arising out of any such uses.
(d) This Paragraph 4 is the only warranty by Seller with respect to goods and may not be modified or amended except in writing signed by an authorized officer of Seller.
(e) Buyer acknowledges and agrees that it is not relying on any applications, diagrams or circuits contained in any literature, and by its conditions Buyer will test all parts and applications under extended field and laboratory conditions. Notwithstanding any cross-reference or any statements of compatibility, functionality, interchangeability, and the like, the goods may differ from similar goods from other vendors in performance, function or operation, and in areas not contained in the written specifications, or as to ranges and conditions outside such specifications; and Buyer agrees that there are no warranties and that Seller is not responsible for such things.
(f) EXCEPT AS PROVIDED ABOVE, SELLER MAKES NO WARRANTIES OR CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY; AND SELLER EXPRESSLY EXCLUDES AND DISCLAIMS ANY WARRANTY OR CONDITION OF MERCHANTABILITY OR FITNESS FOR PARTICULAR PURPOSE OR APPLICATION.

5. LIMITATION OF LIABILITY

(a) Seller will not be liable for any loss, damage or penalty resulting from causes beyond its reasonable control, including but not limited to delay by others, force majeure, acts of God, or labor conditions. In any such event, the date(s) for Seller's performance will be deemed extended for a period equal to any delay resulting.
(b) THE LIABILITY OF SELLER ARISING OUT OF THE CONTRACT OR ANY GOODS SOLD WILL BE LIMITED TO REFUND OF THE PURCHASE PRICE OR REPLACEMENT OF PURCHASED GOODS (RETURNED TO SELLER FREIGHT PRE-PAID) OR, WITH SELLER'S PRIOR WRITTEN CONSENT, REPAIR OF PURCHASED GOODS.
(c) Buyer will not return any goods without first obtaining a customer return order number.
(d) AS A SEPARATE LIMITATION, IN NO EVENT WILL SELLER BE LIABLE FOR COSTS OF SUBSTITUTE GOODS; FOR ANY SPECIAL, CONSEQUENTIAL, INCIDENTAL OR INDIRECT DAMAGES; OR LOSS OF USE, OPPORTUNITY, MARKET POTENTIAL, AND/OR PROFIT ON ANY THEORY (CONTRACT, TORT, FROM THIRD PARTY CLAIMS OR OTHERWISE). THESE LIMITATIONS SHALL APPLY NOTWITHSTANDING ANY FAILURE OF ESSENTIAL PURPOSE OF ANY REMEDY.

(e) No action against Seller, whether for breach, indemnification, contribution or otherwise, shall be commenced more than one year after the cause of action has accrued, or more than one year after either the Buyer, user or other person knew or with reasonable diligence should have known of the matter or of any claim of dissatisfaction or defect involved; and no such claim may be brought unless Seller has first been given commercially reasonable notice, a full written explanation of all pertinent details, and a good faith opportunity to resolve the matter.
(f) BUYER EXPRESSLY AGREES TO THE LIMITATIONS OF THIS PARAGRAPH 5 AND TO THEIR REASONABLENESS.

6. SUBSTITUTIONS AND MODIFICATIONS

Seller may at any time make substitutions for product ordered which do not materially and adversely affect overall performance with the then current specifications in the typical and intended use. Seller reserves the right to halt deliveries and shipments and alter specifications and prices without notice. Buyer shall verify that the literature and information is current before purchasing.

7. CANCELLATION

The purchase contract may not be canceled by Buyer except with written consent by Seller and Buyer's payment of reasonable cancellation charges (including but not be limited to expenses already incurred for labor and material, overhead, commitments made by Seller, and a reasonable profit).

8. INDEMNIFICATION

Seller will, at its own expense, assist Buyer with technical support and information in connection with any claim that any parts as shipped by Seller under the purchase order infringe any valid and enforceable copyright, or trademark, provided however, that Buyer (i) gives immediate written notice to Seller, (ii) permits Seller to participate and to defend if Seller requests to do so, and (iii) gives Seller all needed information, assistance and authority. However, Seller will not be responsible for infringements resulting from anything not entirely manufactured by Seller, or from any combination with products, equipment, or materials not furnished by Seller. Seller will have no liability with respect to intellectual property matters arising out of products made to Buyer's specifications, code, or designs.

Except as expressly stated in this Paragraph 8 or in another writing signed by an authorized officer, Seller makes no representations and/or warranties with respect to intellectual and/or industrial property and/or with respect to claims of infringement. Except as to claims Seller agrees in writing to defend, BUYER WILL INDEMNIFY, DEFEND AND HOLD HARMLESS SELLER FROM ALL CLAIMS, COSTS, LOSSES, AND DAMAGES (INCLUDING ATTORNEYS FEES) AGAINST AND/OR ARISING OUT OF GOODS SOLD AND/OR SHIPPED HEREUNDER.

9. NO CONFIDENTIAL INFORMATION

Seller shall have no obligation to hold any information in confidence except as provided in a separate non-disclosure agreement signed by both parties.

10. ENTIRE AGREEMENT

(a) These terms and conditions are the entire agreement and the only representations and understandings between Seller and Buyer, and no addition, deletion or modification shall be binding on Seller unless expressly agreed to in written and signed by an officer of Seller.
(b) Buyer is not relying upon any warranty or representation except for those specifically stated here.

11. APPLICABLE LAW

The contract and all performance and disputes arising out of or relating to goods involved will be governed by the laws of R.O.C. (Taiwan, Republic of China), without reference to the U.N. Convention on Contracts for the International Sale of Goods or to conflict of laws principles. Buyer agrees at its sole expense to comply with all applicable laws in connection with the purchase, use or sale of the goods provided hereunder and to indemnify Seller from any failure by Buyer to so comply. Without limiting the foregoing, Buyer certifies that no technical data or direct products thereof will be made available or re-exported, directly or indirectly, to any country to which such export or access is prohibited or restricted under R.O.C. laws or U.S. laws or regulations, unless prior authorization is obtained from the appropriate officials and agencies of the government as required under R.O.C. or U.S. laws or regulations.

12. JURISDICTION AND VENUE

The courts located in Hsinchu, Taiwan, Republic of China, will have the sole and exclusive jurisdiction and venue over any dispute arising out of or relating to the contract or any sale of goods hereunder. Buyer hereby consents to the jurisdiction of such courts.

13. ATTORNEYS' FEES

Reasonable attorneys' fees and costs will be awarded to the prevailing party in the event of litigation involving and/or relating to the enforcement or interpretation of the contract and/or any goods sold under it.