SHARP®

Integrated Circuits Group

APPLICATIONS:
- PDA
- Digital Camera

LH28F160S3 16M (2M × 8/1M ×16) Smart 3 Flash Memory

FEATURES

- Smart 3 Technology
  - 2.7 V or 3.3 V V_{CC}
  - 2.7 V or 3.3 V or 5V V_{PP}
- Common Flash Interface (CFI)
  - Universal and upgradable interface
- Scalable Command Set (SCS)
- High speed write performance
  - 32 bytes × 2 plane page buffer
  - 2.7 µs/byte write transfer rate
- High speed read performance
  - 100/130 ns (3.3 V ±0.3 V), 120/150 ns (2.7 V – 3.6 V)
- Enhanced automated suspend options
  - Write suspend to read
  - Block erase suspend to write
  - Block erase suspend to read
- Industry-standard packaging
  - 56-pin TSOP
  - 56-pin TSOP (Reverse bend)
  - 56-pin SSOP
  - 64-pin SDIP
- Chip size packaging
  - 64-ball CSP
- SRAM-compatible write interface
- User-configurable × 8 or × 16 operation
- High-density symmetrically-blocked architecture
  - Thirty-two 64K erasable blocks
- Enhanced data protection features
  - Absolute protection with V_{PP} = GND
  - Flexible block locking
  - Erase/write lockout during power transitions
- Extended cycling capability
  - 100,000 block erase cycles
  - 3.2 million block erase cycles/chip
- Low power management
  - Deep power-down mode
  - Automatic power savings mode decreases I_{CC} in static mode
- Automated write and erase
  - Command user interface
  - Status register
- ETOX™ V nonvolatile flash technology
- Not designed or rated as radiation hardened.

DESCRIPTION

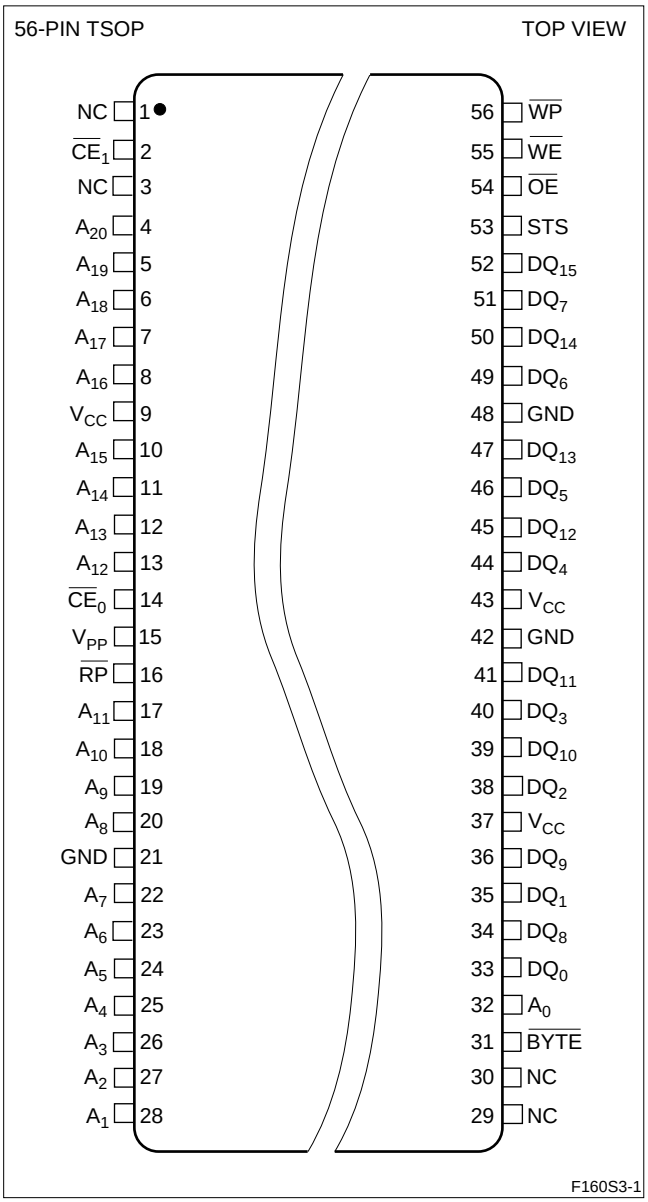
SHARP's LH28F160S3 Flash memory with Smart 3 technology is a high-density, low-cost, nonvolatile, read/write storage solution for a wide range of applications. Its symmetrically-blocked architecture, flexible voltage and extended cycling provide for highly flexible component suitable for resident flash arrays, SIMMs and memory cards. Its enhanced suspend capabilities provide for an ideal solution for code and data storage applications. For secure code storage applications, such as networking, where code is either directly executed out of flash or downloaded to DRAM, the LH28F160S3 offers three levels of protection: absolute protection with V_{PP} at GND, selective hardware block locking, or flexible software block locking. These alternatives give designers ultimate control of their code security needs.

The LH28F160S3 conforms to the flash Scalable Command Set (SCS) and the Common Flash Interface (CFI) specification which enable universal and upgradable interface, enable the highest system/device data transfer rates and minimize device and system-level implementation costs.

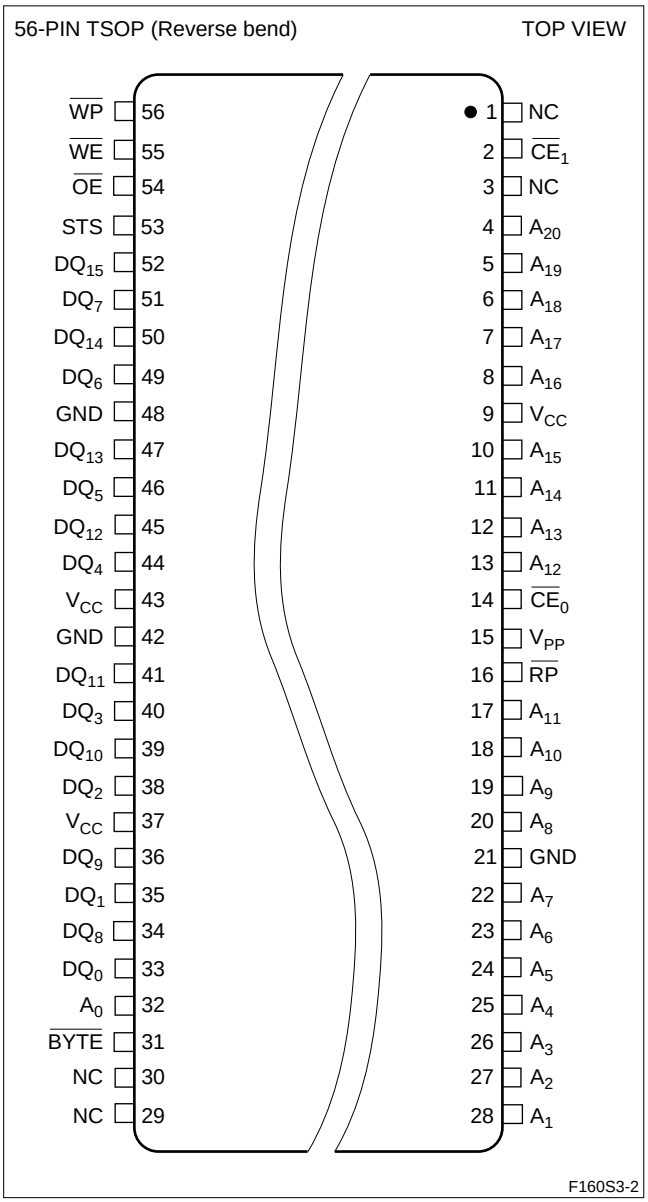
The LH28F160S3 is manufactured on SHARP's 0.4 µm ETOX™ V process technology. It comes in industry-standard package: the 56-pin TSOP, 56-pin SSOP, 64-pin SDIP or Chip size package: the 64-ball CSP, ideal for board constrained applications.

This Product Information is from LH28F160S3 Preliminary Product Preview, Rev. 1.3

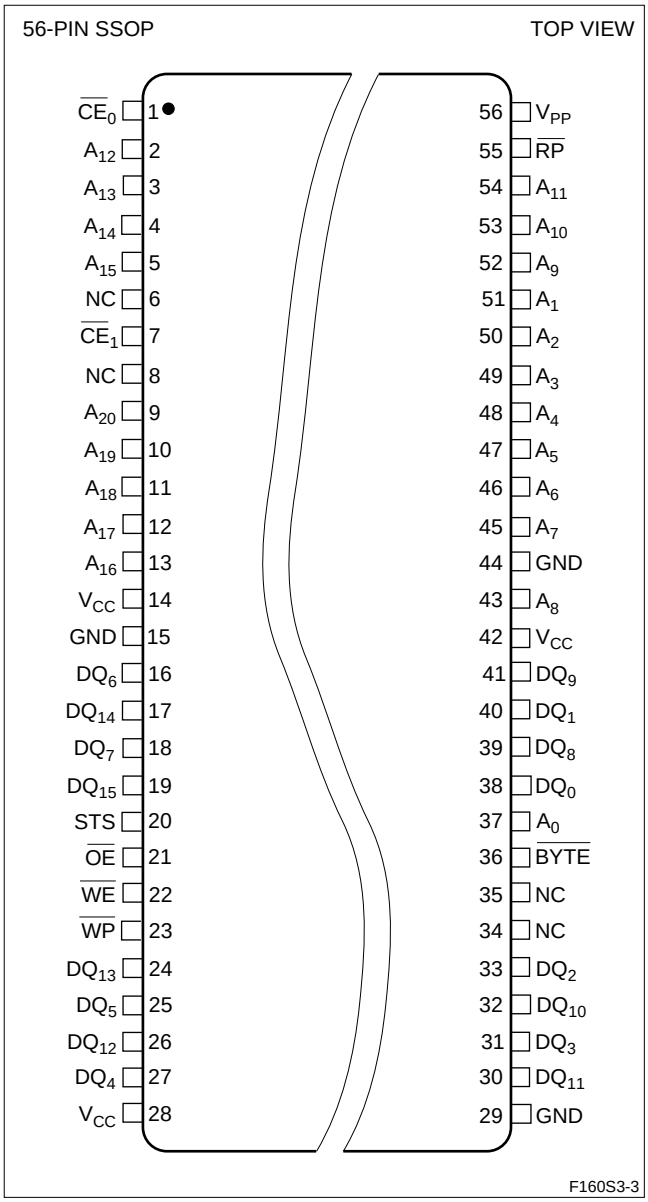
56-PIN TSOP PINOUT



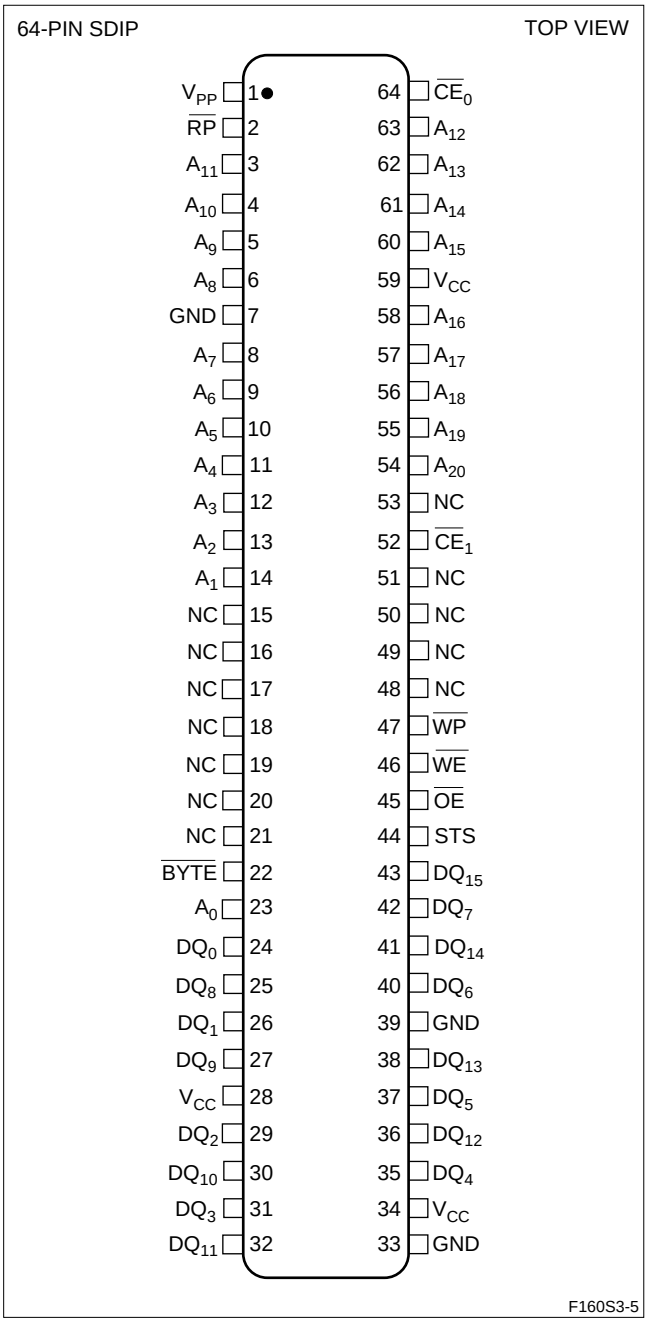
56-PIN TSOP REVERSE BEND PINOUT



56-PIN SSOP PINOUT

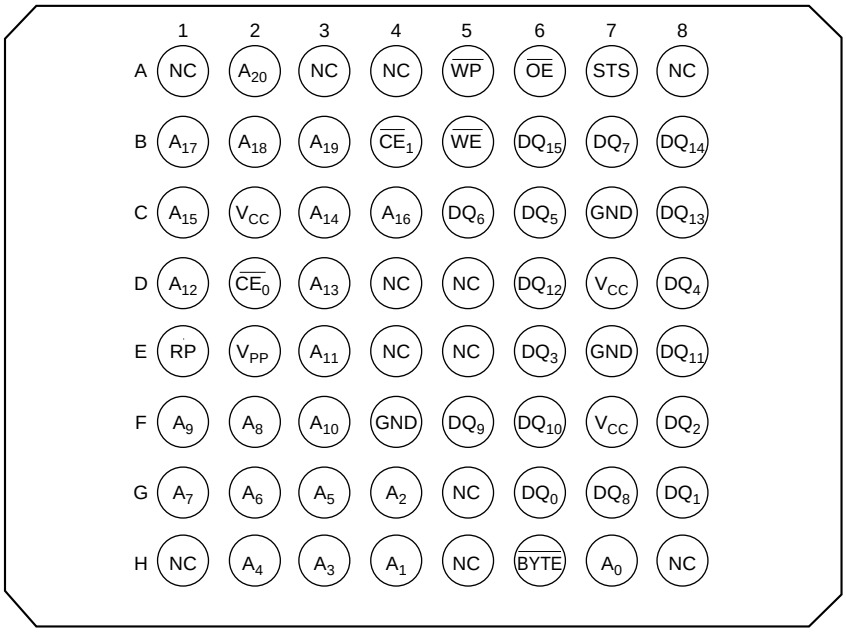


64-PIN SDIP PINOUT



64-BALL CSP PINOUT

64-BALL CSP TOP VIEW



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