February 1985

OBJECTIVE SPECIFICATIONS

Octal Buffers and Line Drivers with 3-State Outputs

Features

- **Function, pin-out, speed and drive compatibility with 54/74LS logic family**
- **Low power consumption characteristic of CMOS**
- **3-State outputs with high drive current (I_{OL} = 24 mA @ V_{OL} = 0.5V) for direct bus interface**
- **Inputs and outputs interface directly with TTL, NMOS and CMOS devices**
- **Wide operating voltage range: 4.5V to 5.5V**
- **Characterized for operation over industrial and military temperature ranges:**
  74HCTLS: −40°C to +85°C
  54HCTLS: −55°C to +125°C

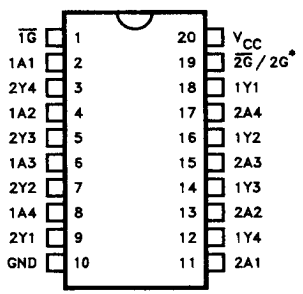
Description

These high-speed octal buffers and line drivers are designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The designer has the choice of combinations of inverting/non-inverting outputs and symmetrical/complementary input controls (both active-low, or one active-low, the other active-high).

Fabricated using Zytrex's proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Configuration



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*$\overline{2G}$ for '240 and '244
2G for '241

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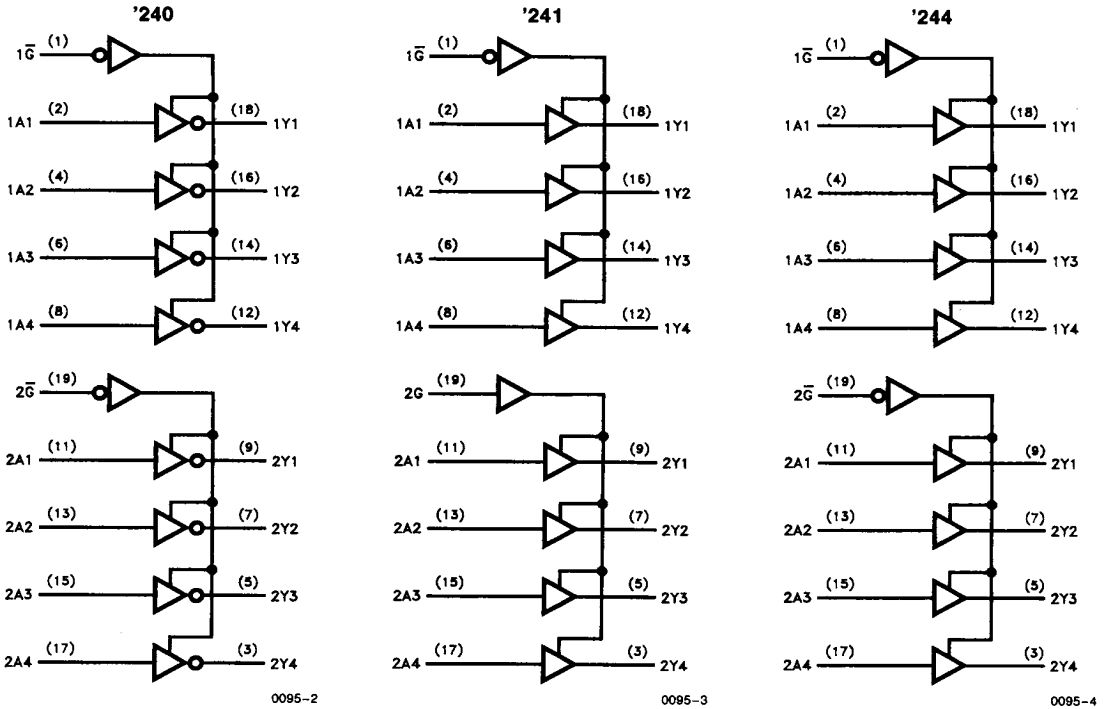
Logic Diagrams



Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} ..... −0.5V to 7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) ..... ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) ..... ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) ..... ±70 mA
Continuous Current Through
V_{CC} or GND pins ..... ±250 mA
Storage Temperature Range, T_{STG} .. −65°C to +150°C
Power Dissipation Per Package, P_D† ..... 500 mW

*Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12 mW/°C from 65°C to 85°C
Ceramic Package (J): −12 mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} ..... 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} ..... 0V to V_{CC}
Operating Temperature
Range ZX74HCTLS: −40°C to +85°C
ZX54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f ..... Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics (V_{CC} = 5V ± 10% Unless Otherwise Specified)

Symbol	Parameter	Test Conditions	T_A = 25°C	74HCTLS T_A = −40°C to +85°C	54HCTLS T_A = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = −20 μA I_O = −6 mA	V_{CC} 4.2	V_{CC} − 0.1 3.98	V_{CC} − 0.1 3.84	V_{CC} − 0.1 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN} = V_{IH} or V_{IL} I_O = 20 μA I_O = 12 mA I_O = 24 mA	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum 3-State Leakage Current	Output Enable = V_{IH} V_{OUT} = V_{CC} or GND		±0.5	±5.0	±10.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80.0	160.0	μA

AC Electrical Characteristics (Input t_r, t_f ≤ 6 ns), HCTLS240/241/244

Symbol	Parameter	Conditions†		T_A = 25°C V_{CC} = 5.0V	74HCTLS T_A = −40°C to +85°C V_{CC} = 5.0V ±10%		54HCTLS T_A = −55°C to +125°C V_{CC} = 5.0V ±10%		Unit
				Typ	Guaranteed Limits				
t_{PLH}	Maximum Propagation Delay, A to Y	C_L = 50 pF C_L = 150 pF		13 19	18 25	22 31	27 38		ns
t_{PHL}		C_L = 50 pF C_L = 150 pF		13 19	18 25	22 31	27 38		ns
t_{PZH}	Maximum Output Enable Time, Enable to Y	R_L = 1 kΩ	C_L = 50 pF C_L = 150 pF	17 23	23 30	29 38	34 45		ns
t_{PZL}			C_L = 50 pF C_L = 150 pF	17 23	23 30	29 38	34 45		ns
t_{PHZ}	Maximum Output Disable Time, Enable to Y	R_L = 1 kΩ C_L = 50 pF		16	21	26	32		ns
t_{PLZ}				16	21	26	32		ns
C_{IN}	Maximum Input Capacitance			5					pF
C_{OUT}	Maximum Output Capacitance	Output Disabled		10					pF
C_{PD}	Power Dissipation Capacitance* (per stage)	Output Disabled Output Enabled		5 30					pF

*C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.
†For AC switching test circuits and timing waveforms see section 2.

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