SanDisk SD Card

OEM Product Manual

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Revision History

Date	Revision	Description
January 2007	2.0	
February 2007	2.1	
June 2007	2.2	Added: -Reliability and Durability Specifications Table for the SD Card to Chapter 2 -Additional capacities and related specs to Tables 3-8 and 3-9 -C Size 6 GB and related specs to Table 3-7 -CID values to Table 3-4 -CSD values to Table 3-6 -TOC with subheadings removed application notes from Appendix D, replaced with links to white paper docs. Consolidated shared specifications in Chapter 2. Switched to out dent format. Rearranged General Description in Chapter 1. Changed hierarchy under Functional Description in Chapter 1. Corrected part number for microSD 6 GB and 8 GB. Made changes to Tables 3-6 and 3-7 according to feedback.
October 2007	2.3	Added microSD Card top view to Chapter 2. Changed sleep current for microSD 6GB/8GB. Other minor edits.
April 2009	2.4	Removed miniSD and microSD (addressed in a separate manual); Sleep current updated; CSD Register updated; DOS Image parameters updated; Ordering information updated
August 2009	2.5	Updated Appendix A SKU information
October 2009	2.6	Updated Class information for SDSDAA-002G and SDSDAB-002G
January 2010	2.7	Updated SDA Version from 2.0 to SDA Version 3.0
August 2010	2.8	Updated speed class for SDSDAA parts
November 2010	2.9	Updated speed class for SDSDAB parts
March 2011	3.0	Updated SDSDAC products - UHSI, 30/30 MB/s Class 10 Added SDSDAB-064G product

Table of Contents

1 Introduction

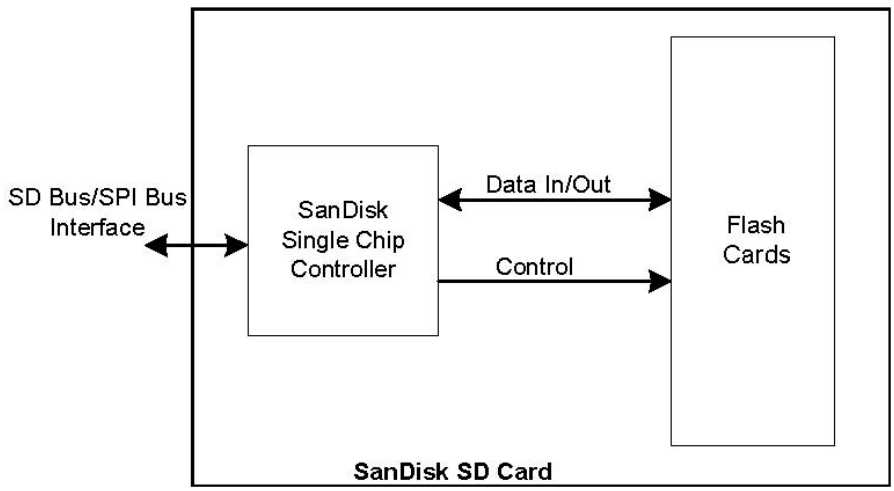
1.1 General Description

The SanDisk SD Card is a flash based removable non-volatile memory device specifically designed to meet the security, capacity, performance and environmental requirements inherent in next generation consumer electronic devices. .

The SanDisk SD Card is based on a 9-pin interface designed to operate in a maximum operating frequency of 100 MHz. The interface for SD Card products allows for easy integration into any design, regardless of which type of microprocessor is used. In addition to the interface, SD Card products offer an alternate communication-protocol based on the SPI standard.

SanDisk SD cards are designed especially for use in mass storage applications. In addition to the mass storage-specific flash memory. SD cards include an on-board intelligent controller which manages interface protocols; security algorithms for content protection; data storage and retrieval, as well as Error Correction Code (ECC) algorithms; defect handling; power management; wear leveling and clock control.

Figure 1-1 SanDisk SD Card Block Diagram



1.2 Features

General features of cards in the SanDisk SD Card include:

- SD-protocol compatible
- Supports SPI Mode
- Targeted for portable and stationary applications for secured (content protected) and unsecured data storage
- Voltage range of 2.7 to 3.6V
- Variable clock rate 0-25 MHz (standard), 0-50 MHz (high performance) . 0-100MHz (Ultra High Speed)
- Up to 50 MB/sec data transfer rate (using four parallel data lines)
- Memory field error correction
- Password protection
- Write-protection using mechanical switch
- Built-in write protection features (permanent and temporary)
- Supports card detection (insertion and removal)
- Application-specific commands

1.3 Scope

This document describes key features and specifications of the SanDisk SD Card as well as the information required to interface this product to a host system. Chapter 2 describes the physical and mechanical properties of cards in the SanDisk SD Card, Chapter 3 contains the pins and register overview, and Chapter 4 gives a general overview of the SD protocol. Information about SPI Protocol can be referenced in Section 7 of the SDA Physical Layer Specification, Version 3.01.

1.4 SD Card Standard

SanDisk SD cards are fully compatible with the SDA Physical Layer Specification, Version 3.01. This specification is available from the SD Card Association (SDA).

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San Ramon, CA 94583
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E-mail: office@sdcard.org
Web site: www.sdcard.org

1.5 Functional Description

The family of SanDisk SD cards contains a high-level, intelligent subsystem as shown in Figure 1-1. This intelligent (microprocessor) subsystem provides many capabilities not found in other types of memory cards. These capabilities include:

- Host independence from details of erasing and programming flash memory
- Sophisticated system for managing defects (analogous to systems found in magnetic disk drives)
- Sophisticated system for error recovery including a powerful ECC
- Power management for low power operation

1.5.1 Technology Independence

The 512-byte sector size of a card in the SanDisk SD Card is the same as that in an IDE magnetic disk drive. To write or read a sector (or multiple sectors), the host software simply

issues a read or write command to the card. The command contains the address and number of sectors to write or read. The host software then waits for the command to complete.

The host software does not get involved in the details of how the flash memory is erased, programmed or read. This is extremely important because flash devices are expected to get increasingly complex in the future. Because SanDisk SD cards use an intelligent on-board controller, host system software will not need to be updated as new flash memory evolves. In other words, systems that support the SD Card today will be able to access future SanDisk cards built with new flash technology without having to update or change host software.

1.5.2 Defect and Error Management

The SanDisk SD Card contains a sophisticated defect and error management system. This system is analogous to the systems found in magnetic disk drives and in many cases offers enhancements. If necessary, SanDisk SD Card will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume any user data space. The SanDisk SD Card soft error rate specification is much better than the magnetic disk drive specification. In the extremely rare case that a read error does occur, SanDisk SD Card has innovative algorithms to recover the data. These defect and error management systems, coupled with the solid state construction, give SanDisk SD Card unparalleled reliability.

1.5.3 Content Protection

A detailed description of the content protection mechanism and related security SD commands can be found in the SD Security Specification from the SDA. All SD security-related commands in the SanDisk SD Card operate in the data transfer mode.

1.5.4 Wear Leveling

Wear leveling is an intrinsic part of the erase pooling functionality of SanDisk SD cards.

1.5.5 Automatic Sleep Mode

A unique feature of SanDisk SD Cards is automatic entrance and exit from sleep mode. Upon completion of an operation, cards enter sleep mode to conserve power if no further commands are received. The host does not have to take any action for this to occur.

When the host is ready to access a card in sleep mode, any command issued to it will cause it to exit sleep, and respond.

1.5.6 Hot Insertion

Support for hot insertion will be required on the host but will be supported through the connector. Connector manufacturers will provide connectors that have power pins long enough to be powered before contact is made with the other pins. This approach is similar to that used in PCMCIA devices to allow for hot insertion.

1.6 SD Card Products in SD Bus Mode

The following sections provide valuable information on SanDisk SD Cards in SD Bus mode.

SanDisk SD Cards are fully compliant with the SDA Physical Layer Specification, Version 3.01. Card Specific Data (CSD) Register structures are compliant with CSD Structure 1.0 and 2.0.

This section covers Negotiating Operating Conditions, Card Acquisition and Identification, Card Status, Memory Array Partitioning, Read/Write Operations, Data Transfer Rate, Data Protection in Flash Cards, Write Protection, Copy Bit, and CSD Register.

Additional practical card detection methods can be found in application notes pertaining to the SDA Physical Layer Specification, Version 3.01.

Figure 1-2 Memory Array Partitioning

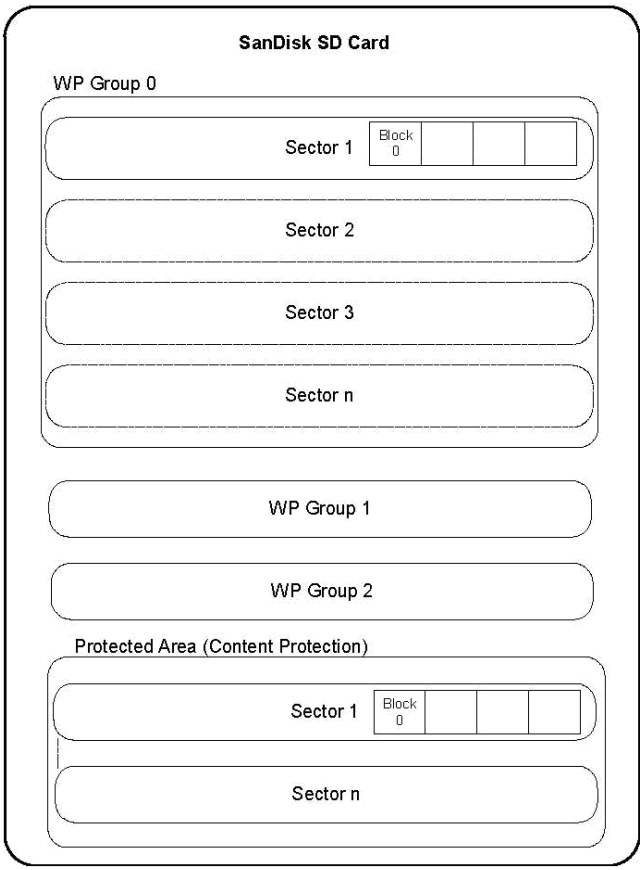


Figure 1-3 illustrates the formatting of a data transfer**.**

Figure 1-3 Data Transfer Formats.

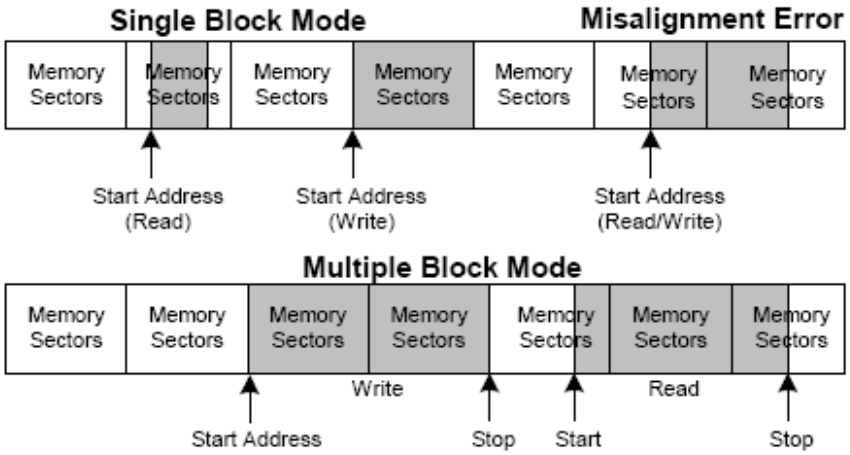


Table 1-1 contains descriptions for each transfer mode.

Table 1-1 Mode Definitions

Mode	Description
Single Block	In this mode the host reads or writes one data block in a pre-specified length. The data block transmission is protected with 16-bit CRC that is generated by the sending unit and checked by the receiving unit. The block length for read operations is limited by the device sector size (512 bytes) but can be as small as a single byte. Misalignment is not allowed. Every data block must be contained in a single physical sector. The block length for write operations must be identical to the sector size and the start address aligned to a sector boundary.
Multiple Block	This mode is similar to the single block mode, except for the host can read/ write multiple data blocks (all have the same length) that are stored or retrieved from contiguous memory addresses starting at the address specified in the command. The operation is terminated with a stop transmission command. Misalignment and block length restrictions apply to multiple blocks and are identical to the single block read/write operations.

1.7 SPI Mode

The SPI Mode is a secondary communication protocol for the SD card. This mode is a subset of the SD Protocol, designed to communicate with an SPI channel, commonly found in Motorola and other vendors' microcontrollers. Detailed information about SPI Mode can be found in Section 7 or the SDA Physical Layer Specification, Version 3.01.

2 Product Specifications

2.1 SD Card

This section provides product specifications for the SanDisk SD Card.

Typical Card Power Requirements

The values stated in Table 2-1 represent the SanDisk SD Card power requirements.

Table 2-1 San Disk SD Card Power Requirements

Mode	Maximum Value
Standard Mode (25 MHz)	
Sleep	350 uA
Read	100 mA
Write	100 mA
Standard Mode – for SDXC card - XPC bit on(25 MHz)	Host selected XPC bit in ACMD41
Sleep	350 uA
Read	150 mA
Write	150 mA
High Performance Mode (50 MHz)	
Sleep	350 uA
Read	200 mA
Write	200 mA
UHS-I SDR50 Mode – (100 MHz)	
Sleep	350 uA
Read	400 mA
Write	400 mA
UHS-I DDR50 Mode – (50 MHz)	
Sleep	350 uA
Read	400 mA
Write	400 mA
UHS-I SDR104 Mode – (208 MHz)	
Sleep	350 uA
Read	800 mA
Write	800 mA

NOTE Current consumption is measured by averaging over one (1) second. Refer to Section 6.6.3 of the SDA Physical Layer Specification, Version 3.01 for more information.

2.1.1 System Performance

This section provides the system performance specifications for the SanDisk SD Card. All performance values in Table 2-2 were measured under the following conditions:

- Voltage range 2.7 to 3.6V

- Temperature -25 ° C to 85 ° C
- Independent of card clock frequency

Table 2-2 System Performance

Timing	Maximum Value
Block Read Access Time	100 ms
Block Write Access Time	250 ms

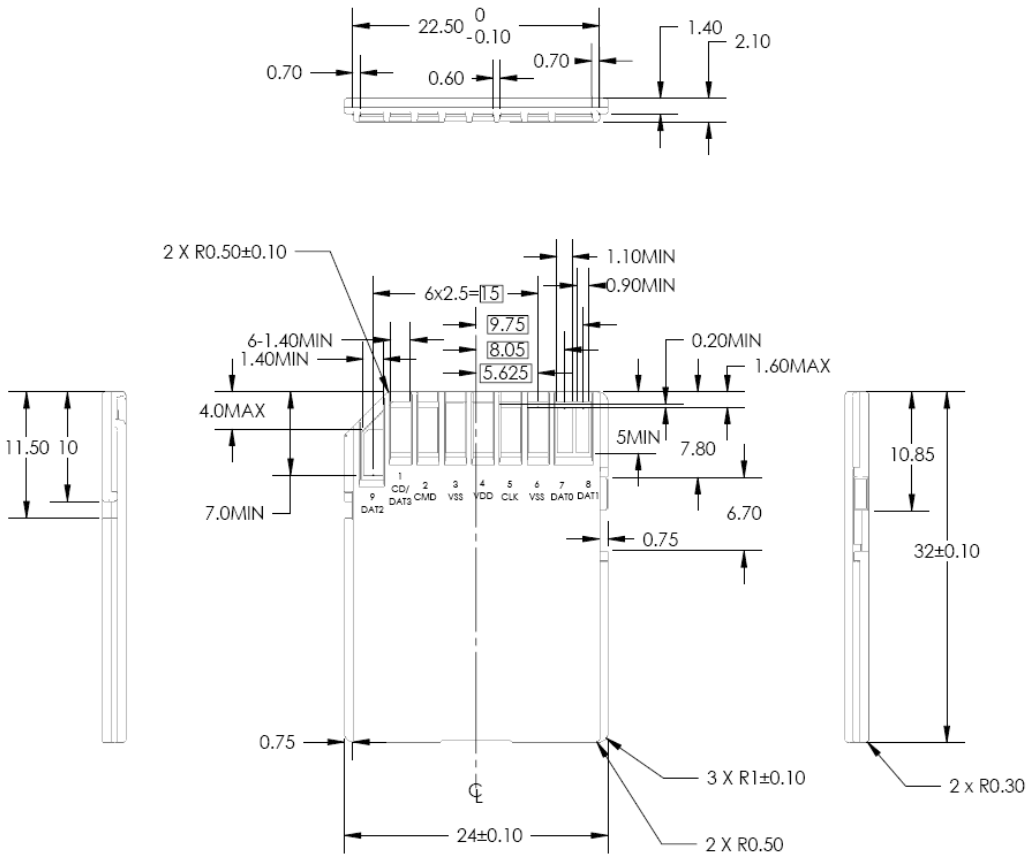
2.1.2 Physical Specifications

Table 2-3 and Figure 2-1 provides the physical dimensions of the SanDisk SD Card.

Table 2-3 SanDisk SD Card Physical Specification Summary

Specification	SanDisk SD Card
Weight	2.5 g maximum
Length	32 mm +/- 0.1 mm
Width	24 mm +/- 0.1 mm
Thickness	2.1 mm +/- 0.15 mm

Figure 2-1 SD Card Dimensions



Notes unless otherwise specified:

All dimensions are in mm
General Tolerance ± 0.15

3 Interface Description

3.1 Pins and Registers

The SanDisk SD Card has exposed contacts on one side. The host uses a dedicated 9-pin connector to connect to SD cards.

In Table 3-1, pin assignments for the SanDisk SD Card are for SD Bus Mode. Table 3-2 contains pin assignments for SPI Mode.

NOTE Pin assignments are provided by the SDA Physical Layer Specification, Version 3.00 and associated addendums. For more details, refer to Section 3.7 of the SDA Physical Layer Specification Layer 3.00.

Table 3-1 SD Bus Mode Pin Assignment

Pin No.	Name	Type[a]	Description
SD Card			
1	CD/DAT3[b]	I/O[c]/PP	Card Detect/Data Line [bit 3]
2	CMD	PP	Command/Response
3	V_{SS1}	S	Supply Voltage Ground
4	V_{DD}	S	Supply Voltage
5	CLK	I	Clock
6	V_{SS2}	S	Supply Voltage Ground
7	DAT0	I/O/PP	Data Line [bit 0]
8	DAT1	I/O/PP	Data Line [bit 1]
9	DAT2	I/O/PP	Data Line [bit 2]

a. Type Key: S=power supply; I= input; O=output using push-pull drivers; PP=I/O using push-pull drivers.

b. The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after the SET_BUS_WIDTH Type Key: S=power supply; I=input; O=output using push-pull drivers; PP=I/O using push-pull drivers.)

c. At power up this line has a 50KOhm pullup enabled in the card. This resistor serves two functions: Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command

The SanDisk SD Card pin assignments in Table 3-2 below are for SPI Mode.

Table 3-2 SPI Mode Pin Assignment

Pin No.	Name	Type	Description
SD Card			
1	CS	I	Chip Select (active low)
2	DataIn	I	Host-to-Card Commands and Data
3	VSS1	S	Supply Voltage Ground
4	VDD	S	Supply Voltage
5	SCLK	I	Clock
6	VSS2	S	Supply Voltage Ground
7	DataOut	O/PP	Card-to-Host Data and Status
8	RSV	—	Reserved
9	RSV	—	Reserved

Each card has a set of information registers. Register descriptions and SDA references are provided in Section 3.7 of the SDA Physical Layer Specification, Version 3.00.

Table 3-3 SD Card Register Overview

Register Abbreviation	Width (in bits)	Register Name
CID	128	Card Identification Number
RCA	16	Relative Card Address
CSD	128	Card Specific Data
SCR	64	SD Configuration Register
OCR	32	Operation Condition Register
SSR	512	SD Status Register
CSR	32	Card Status Register

3.2 Bus Topology

The family of SanDisk SD products supports two communication protocols: SD and SPI. For more details, refer to Section 3.5 of the SDA Physical Layer Specification, Version 3.01. Section 6 of the specification contains a bus circuitry diagram for reference.

3.2.1 SD Bus

For more details, refer to Section 3.5.1 of the SDA Physical Layer Specification, Version 3.01.

3.2.2 SPI Bus

For more details, refer to Section 3.5.2 of the SDA Physical Layer Specification, Version 3.01.

3.3 Hot Insertion and Power Protection

Refer to Section 6.1, 6.2 and 6.3 of the SDA Physical Layer Specification, Version 3.01.

3.4 Electrical Interface

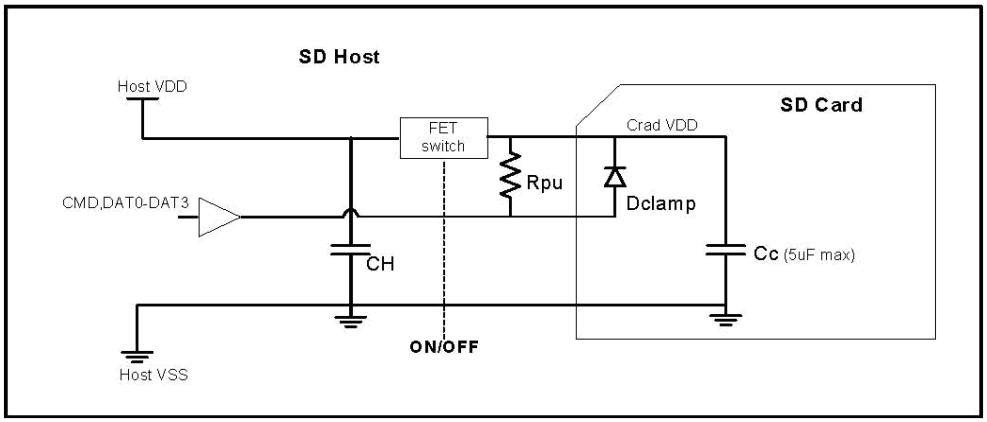
The power scheme of SanDisk SD products is handled locally in each card and in the bus master. Refer to Section 6.4 of the SDA Physical Layer Specification, Version 3.01.

3.4.1 Power Up

Power must be applied to the VDD pin before any I/O pin is set to logic HIGH. In other words, CMD, CLK, and DAT0-3 must be at zero (0) volts when power is applied to the VDD pin. For more information, refer to Section 6.4.1 of the SDA Physical Layer Specification, Version 3.01.

Figure 3-1 provides the recommended power control scheme

Figure 3-1 Recommended Power Control Scheme



The recommended power control scheme for SanDisk SD card is illustrated in Figure 3-1. Most card connectors have a card detect switch that signals the SD host when the card is inserted. After the host is aware of the card insertion, it turns on the FET switch to apply power to card's VDD pin.

Once the card is inserted and all card pins are making contact, there is a delay before the FET switch is turned on.

IMPORTANT: Because there are clamping diodes on the CMD, CLK, and DAT0-3 pins, it is crucial to ensure that CLK, CMD, and DAT0-3 are at zero (0) volts during the delay and before the FET switch is turned on. If any I/O pin, (CMD, CLK, or DAT0-3) goes above zero volts during the delay and before power reaches the card VDD pin, it will forward bias the clamping diodes and can cause the card to go into an unknown state.

It is the host's responsibility to make sure power gets to VDD before CMD, CLK, or DAT0-3 go above zero volts.

3.4.2 Bus Operating Conditions

SPI Mode bus operating conditions are identical to SD Card Bus Mode operating conditions. For details, see Section 6.6 of the SDA Physical Layer Specification, Version 3.01.

3.4.3 Bus Timing (Standard Mode)

See Section 6.7 of the SDA Physical Layer Specification, Version 3.01.

3.5 SD Card Registers

There is a set of eight registers within the card interface. However, the DSR Register is optional and is not used in SanDisk SD Card. For specific information about all registers, refer to Section 5 of the SDA Physical Layer Specification, Version 3.01.

3.5.1 Operation Conditions Register

The Operation Conditions Register (OCR) stores a card's VDD voltage profile. Refer to Section 5.1 of the SDA Physical Layer Specification, Version 3.01 for more information.

3.5.2 Card Identification Register

The Card Identification (CID) Register is 16 bytes long and contains the unique card identification number. It is programmed during card manufacturing and cannot be changed by card hosts. See Table 3-4.

Table 3-4 CID Register Definitions

Name	Type	Width	CID Value	Comments
Manufacturer ID (MID)	Binary	8	0x03	Manufacturer IDs are controlled and assigned by the SD-3C, LLC.
OEM/Application ID (OID)	ASCII	16	SD ASCII Code 0x53, 0x44	Identifies the card OEM and/or the card contents. The OID is controlled and assigned by the SD-3C, LLC.
Product Name (PNM)	ASCII	40	**SD** SD16G SD08G SD04G SD02G SD01G SD512 SD256 SD128 SD064	Five-character ASCII string.
Product Revision (PRV)	BCD	8	Product Revision xx	See Section 5.2 in the SDA Physical Layer Specification, Version 3.00.
Serial Number (PSN)	Binary	32	Product Serial Number	32-bit unsigned integer
Reserved	—	4	—	—
Manufacture Date Code (MDT)	BCD	12	Manufacture date (for example, April 2001=0x014)	Manufacturing date–yym (offset from 2000)
CRC7 Checksum (CRC)	Binary	7	CRC7	Calculated
Not used, always 0	—	1	—	—

3.5.3 Card Specific Data Register

The Card Specific Data (CSD) Register configuration information is required to access card data. The CSD defines the data format, error correction type, maximum data access time, etc. The field structures of the CSD Register vary depending on the physical specifications and card capacity. The CSD_STRUCTURE field in the CSD Register indicates which structure version is used. Table 3-5 shows the version number as it relates to the CSD structure. Refer to Section 5.3.1 of the SDA Physical Layer Specification, Version 3.01 for more information.

Table 3-5 CSD Register Structure

CSD_STRUCTURE	CSD Structure Version	Valid for SD Card Physical Specification Version / Card Capacity
0	CSD Version 1.0	Version 1.01 to 1.10 Version 2.00/Standard Capacity
1	CSD Version 2.0	Version 2.00/High Capacity
2-3	Reserved	—

Table 3-6 provides an overview of the CSD Register. More field-specific information can be found in Section 5.3.2 of the SDA Physical Layer Specification, Version 3.01.

Table 3-6 CSD Register (CSD Version 1.0)

Field	CSD Value	Description
CSD_STRUCTURE	1.0	CSD structure
—	—	Reserved
TAAC	1.5 msec	Data read access-time-1
NSAC	0	Data read access-time-2 in CLK cycles (NSAC*100)
TRANS_SPEED	Standard Mode 25MHz High Performance Mode 50MHz Ultra High Speed Mode 100MHz	Maximum data transfer rate
CCC	All (inc. WP, lock/unlock)	Card command classes
READ_BL_LEN	2G = 0xA Up to 1G = 0x9	Maximum read data block length
READ_BL_PARTIAL	Yes	Partial blocks for read allowed
WRITE_BLK_MISALIGN	No	Write block misalignment
READ_BLK_MISALIGN	No	Read block misalignment
DSR_IMP	No	DSR implemented
—	—	Reserved
C_SIZE 64 MB 128 MB 256 MB 512 MB 1 GB 2 GB	Secured 0xEDF 0xF03 0xF13 0xF1E 0xF22 0xF24	Device Size
VDD_R_CURR_MIN	100 mA	Maximum read current @VDD min
VDD_R_CURR_MAX	80 mA	Maximum read current @VDD max
VDD_W_CURR_MIN	100 mA	Maximum write current @VDD min
VDD_W_CURR_MAX	80 mA	Maximum write current @VDD max
C_SIZE_MULT	2G=2048 1G=1024 512=512 256=256 128=128 64=64	Device size multiplier
ERASE_BLK_EN	Yes	Erase single block enable
SECTOR_SIZE	31 blocks	Erase sector size
WP_GRP_SIZE	127 sectors	Write protect group size
WP_GRP_ENABLE	Yes	Write protect group enable
Reserved	—	Reserved for MMC compatibility
R2W_FACTOR	x16	Write speed factor
WRITE_BL_LEN	0x9	Maximum write data block length
WRITE_BL_PARTIAL	No	Partial blocks for write allowed
—	—	Reserved
FILE_FORMAT_GRP	0	File format group
COPY	Has been copied	Copy flag (OTP)
PERM_WRITE_PROTECT	Not protected	Permanent write protection
TMP_WRITE_PROTECT	Not protected	Temporary write protection
FILE_FORMAT	HD w/partition	File format
Reserved	—	Reserved
CRC	CRC7	CRC
—	—	Not used, always “1”

Refer to Section 5.3.3, Table 5-16 of the SDA Physical Layer Specification, Version 3.00 for more detailed information.

Table 3-7 CSD Register (CSD Version 2.0)

Field	CSD Value	Description
CSD_STRUCTURE	2.0	CSD structure
—	—	Reserved
TAAC	1.5 msec	Data read access-time
NSAC	0	Data read access-time in CLK cycles (NSAC*100)
TRANS_SPEED	Standard Mode 25MHz High Performance Mode 50MHz Ultra High Speed Mode 100MHz	Maximum data transfer rate
CCC	All (inc. WP, lock/unlock)	Card command classes
READ_BL_LEN	9	Maximum read data block length
READ_BL_PARTIAL	Yes	Partial blocks for read allowed
WRITE_BLK_MISALIGN	No	Write block misalignment
READ_BLK_MISALIGN	No	Read block misalignment
DSR_IMP	No	DSR implemented
—	0	Reserved
C_SIZE 4 GB 6 GB 8 GB 12 GB 16 GB 32 GB	Secured 0x1E5C 0x2D8C 0x3CDC 0x5B6C 0x79FC 0xF45C	Device Size
—	0	Reserved
ERASE_BLK_EN	1	Erase single block enable
SECTOR_SIZE	64 blocks	Erase sector size
WP_GRP_SIZE	000000b	Write protect group size
WP_GRP_ENABLE	No	Write protect group enable
Reserved	—	Reserved for MMC compatibility
R2W_FACTOR	x4	Write speed factor
WRITE_BL_LEN		Maximum write data block length
WRITE_BL_PARTIAL	No	Partial blocks for write allowed
—	—	Reserved
FILE_FORMAT_GRP	0	File format group
COPY	Has been copied	Copy flag (OTP)
PERM_WRITE_PROTECT	Not protected	Permanent write protection
TMP_WRITE_PROTECT	Not protected	Temporary write protection
FILE_FORMAT	HD w/partition	File format
Reserved	—	Reserved
CRC	CRC7	CRC
—	—	Not used, always “1”

3.5.4 Card Status Register

The Card Status Register (CSR) transmits the card's status information (which may be stored in a local status register) to the host. The CSR is defined in Section 4.10.1 in the SDA Physical Layer Specification, Version 3.01.

3.5.5 SD Status Register

The SD Status Register (SSR) contains status bits that are related to the SD Card proprietary features and may be used for future applications. The SD Status structure is described in Section 4.10.2 in the SDA Physical Layer Specification, Version 3.01.

3.5.6 Relative Card Address Register

The 16-bit Relative Card Address (RCA) Register carries the card address published by the card during the card identification. Refer to Section 5.4 in the SDA Physical Layer Specification, Version 3.01 for more information.

3.5.7 SD Card Configuration Register

The SD Card Configuration Register (SCR) is in addition to the CSD Register. The SCR provides information about special features in the SanDisk SD Card products. For more information, refer to Section 5.6 in the SDA Physical Layer Specification, Version 3.01.

3.5.8 SD Card Registers in SPI Mode

All card registers are accessible in SPI Mode. Their format is identical to the format in the SD Bus Mode. However a few fields are irrelevant in SPI Mode. In SPI Mode: The Card Status Register has a different, shorter, format as well. Refer to Section 7.4 in the SDA Physical Layer Specification, Version 3.01 for more details.

3.5.9 Data Interchange Format and Card Sizes

In general, a file system provides structure for data in SanDisk SD Card products. The SD Card File System Specification, published by the SDA, describes the file format system that is implemented in the SanDisk SD Card products. In general, each card is divided into two separate DOS-formatted partitions as follows:

- **User Area–**used for secured and non-secured data storage and can be accessed by the user with regular read/write commands.
- **Security Protected Area**–used by content protection applications to save security related data and can be accessed by the host using the secured read/write command after doing authentication as defined in the SD Security Specification. The security protected area size is defined by SanDisk as approximately one percent of the total size of the card.

Table 3-8 describes the user area for SanDisk SD Card.

Table 3-8 User Area DOS Image Parameters

Capacity	Total LBAs	No. of Partition System Area Sectors	Total Partition Sectors	User Data Sectors	User Data Bytes
2GB	3862528	505	3,858,489	3,857,984	1,975,287,808
4GB	7744512	8192	7,736,320	7,728,128	3,956,801,536
8GB	15523840	8192	15,515,648	15,507,456	7,939,817,472
16GB	31116288	8192	31,108,096	31,099,904	15,923,150,848
32GB	62333952	16384	62,325,760	62,309,376	31,902,400,512
64GB	125000704	66304	124967936	124934400	63,864,569,856

4 SD Card Protocol Description

4.1 General Description

SD Protocol information for the SanDisk SD Card is contained in this chapter; information includes SD bus protocol, card identification, and a functional description.

4.2 SD Bus Protocol

Communication over the SD bus is based on command and data-bit streams initiated by a start bit and terminated by a stop bit. See Section 3.6.1 of the SDA Physical Layer Specification, Version 3.01 for details.

4.3 Functional Description

The host controls all communication between itself and the cards. To demonstrate how this communication works, this section provides a general overview of the card identification and data transfer modes; commands; card dependencies; various card operation modes and restrictions for controlling the clock signal. All SD Card commands, together with corresponding responses, state transitions, error conditions, and timings are also provided. For detailed information, refer to Section 4 of the SDA Physical Layer Specification, Version 3.01.

4.3.1 Card Identification Mode

In Card Identification Mode, the host resets all cards, validates operation voltage range, identifies and requests cards to publish a relative card address. For more information see Section 4.2 in the SDA Physical Layer Specification, Version 3.01.

4.3.2 Data Transfer Mode

In Data Transfer Mode, the host may operate the SanDisk SD Card in the fPP frequency range. In the SDA Physical Specification, this section includes information about data read and write, erase, write-protect management, card lock/unlock operations, application-specific commands, switch function command, high-speed mode, command system, and the Send Interface Condition command (CMD8). CMD8 is part of identification mode and command functional differences in high capacity SD cards. For more detailed information, refer to Section 4.3 of the SDA Physical Layer Specification, Version 3.01.

4.3.3 Clock Control

The host can use the bus clock signal in SanDisk SD cards to switch them to energy saving mode or to control data flow on the bus. See Section 4.4 of the SDA Physical Layer Specification, Version 3.01.

4.3.4 Cyclic Redundancy Codes

The Cyclic Redundancy Check (CRC) protects against transmission errors that may occur on the bus in SanDisk SD Cards. Detailed information and examples for CRC7 and CRC16 are provided in Section 4.5 of the SDA Physical Layer Specification, Version 3.01.

4.3.5 Error Conditions

See Section 4.6 of the SDA Physical Layer Specification, Version 3.01.

4.3.6 Commands

See Section 4.7 of the SDA Physical Layer Specification, Version 3.01 for detailed information about card commands in the SanDisk SD Card.

4.3.7 Card State Transition

In SD cards, the state transition is dependent on the received command. The transition is defined in Section 4.8 of the SDA Physical Layer Specification, Version 3.01 along with responses sent on the command line.

4.3.8 Timing Diagrams and Values

See Section 4.12 of the SDA Physical Layer Specification, Version 3.01.

4.3.9 Speed Class Specification

The speed class specification classifies card performance by speed class number and offers the method to calculate performance. For more information, refer to Section 4.13 of the SDA Physical Layer Specification, Version 3.01.

4.3.10 Erase Timeout Calculation

See Section 4.14 of the SDA Physical Layer Specification, Version 3.01.

Appendix A: Ordering Information

Part Number	Capacity	Interface	Sequential Write Performance	Sequential Read Performance	Speed Class Rating
SDSDAA-001G	1GB	SD3.0	n/a	n/a	n/a
SDSDAA-002G	2GB	SD3.0	n/a	n/a	n/a
SDSDAB-002G	2GB	SD3.0	7 MB/s	15 MB/s	n/a
SDSDAA-004G	4GB	SD3.0	n/a	n/a	4
SDSDAB-004G	4GB	SD3.0	5 MB/s	15 MB/s	4
SDSDAC-004G	4GB	SD3.0 UHSI	30 MB/s	30 MB/s	10
SDSDAA-008G	8GB	SD3.0	n/a	n/a	4
SDSDAB-008G	8GB	SD3.0	7 MB/s	15 MB/s	4
SDSDAC-008G	8GB	SD3.0 UHSI	30 MB/s	30 MB/s	10
SDSDAA-016G	16GB	SD3.0	n/a	n/a	4
SDSDAB-016G	16GB	SD3.0	7 MB/s	15 MB/s	4
SDSDAC-016G	16GB	SD3.0 UHSI	30 MB/s	30 MB/s	10
SDSDAA-032G	32GB	SD3.0	n/a	n/a	4
SDSDAB-032G	32GB	SD3.0	7 MB/s	15 MB/s	4
SDSDAC-032G	32GB	SD3.0 UHSI	30 MB/s	30 MB/s	10
SDSDAB-064G	64GB	SD3.0	7 MB/s	15 MB/s	4