



## UC2843B

Preliminary

LINEAR INTEGRATED CIRCUIT

### HIGH-PERFORMANCE CURRENT-MODE PWM CONTROLLERS

#### DESCRIPTION

The UTC **UC2843B** provides off-line or DC-DC fixed-frequency current-mode control design with minimum external components. Internally-implemented circuits include an under-voltage lockout (UVLO) and a precision reference with accuracy at the error amplifier input. The UTC **UC2843B** also contain internal circuits which include a pulse width modulation (PWM) comparator providing current-limit control, logic ensuring latched operation, and a totem-pole output stage designed to source or sink high-peak current. The output stage is low when it is in off-state condition and suitable for N-channel MOSFETs driving.

The UTC **UC2843B** also has following advantages: the start-up current lower than 0.5mA while the oscillator discharge current is specified to 8.3mA (Typ.). In UVLO conditions, the output has a maximum saturation voltage of 1.2V when sinking 10mA@V<sub>CC</sub> = 5V.

The typical UVLO threshold of the UTC **UC2843B** is 8.4V (on) and 7.6V (off) and can operate to duty cycles approximately 100%.

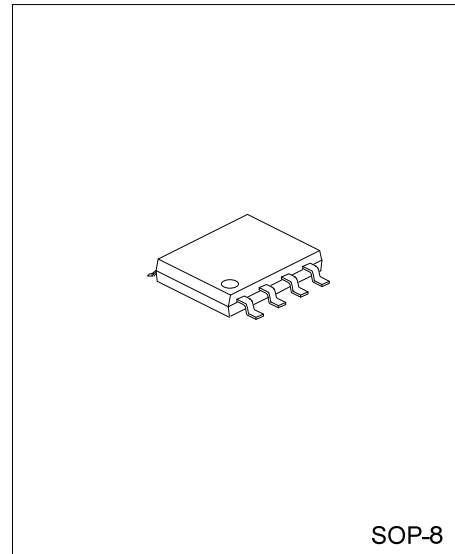
#### FEATURES

- \* Current mode operation:500 kHz
- \* Low start-up current value<0.5mA
- \* Latching PWM for cycle-by-cycle current limiting
- \* Trimmed oscillator discharge current
- \* Automatic feed-forward compensation
- \* Internally trimmed reference with UVLO
- \* High-current totem-pole output UVLO with hysteresis
- \* Double-pulse suppression
- \* Halogen free

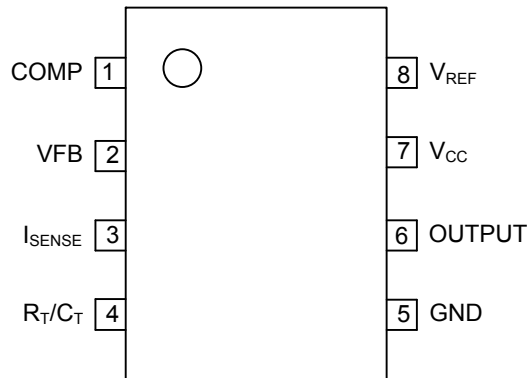
#### ORDERING INFORMATION

Ordering Number	Package	Packing
UC2843BG-S08-R	SOP-8	Tape Reel

<p>UC2843BG-S08-R</p> <p>(1)Packing Type (2)Package Type (3)Halogen Free</p>	<p>(1) R: Tape Reel (2) S08: SOP-8 (3) G: Halogen Free</p>
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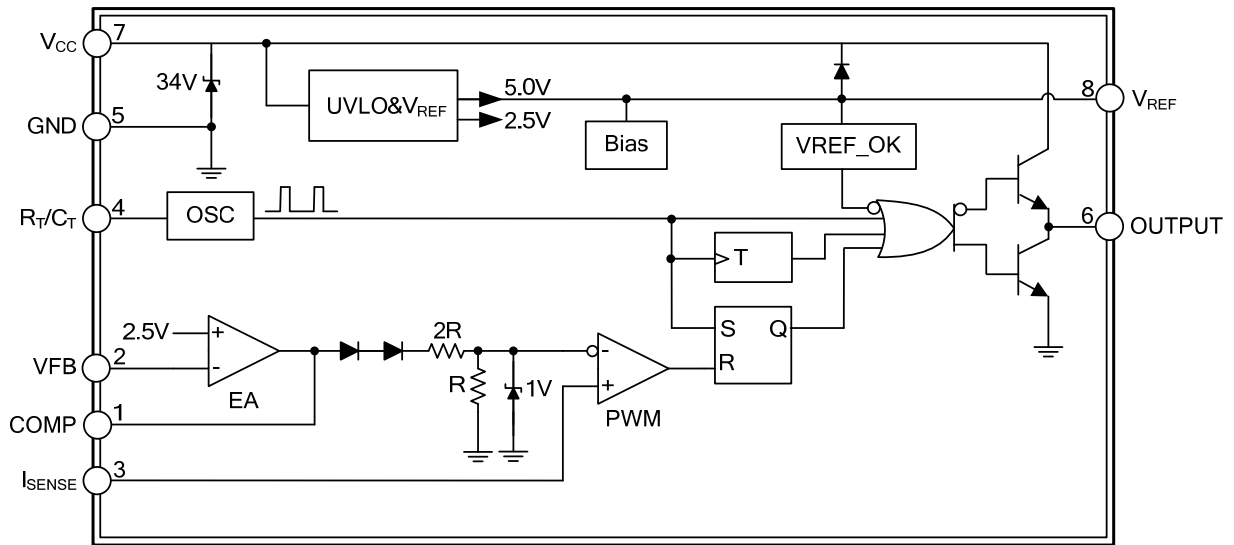
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	COMP	This pin is the Error Amplifier output and is made available for loop compensation.
2	VFB	This is the inverting input of the Error Amplifier. It is normally connected to the switching power supply output through a resistor divider.
3	$I_{SENSE}$	A voltage proportional to inductor current is connected to this input. The PWM uses this information to terminate the output switch conduction.
4	$R_T/C_T$	The Oscillator frequency and maximum Output duty cycle are programmed by connecting resistor $R_T$ to $V_{REF}$ and capacitor $C_T$ to ground. Operation to 500 kHz is possible.
5	GND	This pin is the combined control circuitry and power ground.
6	OUTPUT	This output directly drives the gate of a power MOSFET. Peak currents up to 1.0 A are sourced and sunk by this pin.
7	$V_{CC}$	This pin is the positive supply of the control IC.
8	$V_{REF}$	This is the reference output. It provides charging current for capacitor $C_T$ through resistor $R_T$ .

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING(Ta=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage (Low impedance source)	V <sub>CC</sub>	30	V
Analog Input Voltage (V <sub>FB</sub> and I <sub>SENSE</sub> )	V <sub>IN</sub>	-0.3~+6.3	V
Supply Current	I <sub>CC</sub>	30	mA
Output Current	I <sub>OUT</sub>	±1	A
Error Amplifier Output Sink Current	I <sub>O(SINK)</sub>	10	mA
Power Dissipation	P <sub>D</sub>	702	mW
Output Energy (Capacitive load)	W	5	μJ
Junction Temperature	T <sub>J</sub>	150	°C
Operating Temperature	T <sub>OPR</sub>	-40~+85	°C
Storage Temperature	T <sub>STG</sub>	-65~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.  
2. All voltages are concerning the device GND terminal.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction to Ambient	θ <sub>JA</sub>			178	°C/W

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V <sub>CC</sub>			30	V
Input Voltage	R <sub>T</sub> /C <sub>T</sub>	0		5.5	V
	V <sub>FB</sub> and I <sub>SENSE</sub>	0		5.5	V
Output Voltage (OUTPUT)	V <sub>OUT</sub>	0		30	V
Supply Current, Externally Limited	I <sub>CC</sub>			25	mA
Output Current	I <sub>OUT</sub>			200	mA
Reference Output Current	I <sub>O(REF)</sub>			-20	mA
Oscillator Frequency	f <sub>OSC</sub>		100	500	kHz
Operating Temperature	T <sub>a</sub>	-40		+85	°C

### ■ ELECTRICAL CHARACTERISTICS

( $V_{CC} = 15\text{ V}$ ,  $R_T = 10\text{ k}\Omega$ ,  $C_T = 3.3\text{ nF}$ ,  $T_J = 25^\circ\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REFERENCE SECTION</b>						
Reference Output Voltage	$V_{REF}$	$I_{OUT} = 1\text{ mA}$ , $T_J = 25^\circ\text{C}$	4.95	5	5.05	V
Line Regulation	$\Delta V_{OUT}$	$V_{CC} = 12\text{ V} \sim 25\text{ V}$		6	20	mV
Load Regulation	$\Delta V_{OUT}$	$I_{OUT} = 1\text{ mA} \sim 20\text{ mA}$		6	25	mV
Average Temperature Coefficient Of Output Voltage	$T_S$			0.2	0.4	mV/ $^\circ\text{C}$
Total Output Variation	$V_{REF}$	$V_{CC} = 12\text{ V} \sim 25\text{ V}$ , $I_{OUT} = 1\text{ mA} \sim 20\text{ mA}$	4.9		5.1	V
Output Noise Voltage	eN	$f = 10\text{ Hz} \sim 10\text{ kHz}$ , $T_J = 25^\circ\text{C}$		50		$\mu\text{V}$
Long Term Stability		$T_J = 25^\circ\text{C}$ FOR 1000 hours		5	25	mV
Output Short Circuit Current	$I_{SC}$		-30	-100	-180	mA
<b>OSCILLATOR SECTION</b>						
Frequency	$f_{OSC}$	$T_J = 25^\circ\text{C}$ , $R_T = 62\text{ k}\Omega$ , $C_T = 1\text{ nF}$ , Min = 225 kHz, Max = 275 kHz	49	52	55	kHz
		$T_J = \text{Full range}$	48		56	kHz
Frequency Change with Voltage	$\frac{\Delta f_{OSC}}{\Delta V}$	$V_{CC} = 12\text{ V} \sim 25\text{ V}$		0.2	1	%
Frequency Change with Temperature	$\frac{\Delta f_{OSC}}{\Delta T}$	$T_J = \text{Full range}$		5		%
Oscillator Voltage Swing	$V_{OSC}$	Peak to peak		1.7		V
Discharge Current	$I_{DISC}$	$T_J = 25^\circ\text{C}$ , $R_T/C_T = 2\text{ V}$	7.8	8.3	8.8	mA
		$R_T/C_T = 2\text{ V}$	7.5		8.8	mA
<b>ERROR-AMPLIFIER SECTION</b>						
Voltage Feedback Input	$V_{FB}$	COMP = 2.5V	2.45	2.5	2.55	V
Input Bias Current	$I_{I(BIAS)}$			-0.3	-1	$\mu\text{A}$
Open Loop Voltage Gain	$G_{VO}$	$V_{OUT} = 2\text{ V} \sim 4\text{ V}$	65	90		dB
Unity Gain Bandwidth	$G_{BW}$		0.7	1		MHz
Power Supply Rejection Ratio	PSRR	$V_{CC} = 12\text{ V} \sim 25\text{ V}$	60	70		dB
Output Sink Current	$I_{SINK}$	$V_{FB} = 2.7\text{ V}$ , COMP = 1.1V	2	6		mA
Output Source Current	$I_{SOURCE}$	$V_{FB} = 2.3\text{ V}$ , COMP = 5V	-0.5	-0.8		mA
Output Voltage Swing High State	$V_{OH}$	$V_{FB} = 2.3\text{ V}$ , $R_L = 15\text{ k}\Omega$ to GND	5	6		V
	$V_{OL}$	$V_{FB} = 2.7\text{ V}$ , $R_L = 15\text{ k}\Omega$ to GND		0.7	1.1	V
<b>CURRENT-SENSE SECTION</b>						
Current Sense Input Voltage Gain	$G_V$	(Note 2,3)	2.85	3	3.15	V/V
Maximum Current Sense Input Threshold	$V_{TH}$	COMP = 5V (Note 2)	0.9	1	1.1	V
Power Supply Rejection Ratio	PSRR	$V_{CC} = 12\text{ V} \sim 25\text{ V}$ (Note 2)		70		dB
Input Bias Current	$I_{I(BIAS)}$			-2	-10	$\mu\text{A}$
Propagation Delay	$t_D$	$V_{FB} = 0\text{ V} \sim 2\text{ V}$		150	300	ns
<b>OUTPUT SECTION</b>						
High-Level Output Voltage	$V_{OH}$	$I_{OH} = -20\text{ mA}$	13	13.5		V
		$I_{OH} = -200\text{ mA}$	12	13.5		V
Low-Level Output Voltage	$V_{OL}$	$I_{OL} = 20\text{ mA}$		0.1	0.4	V
		$I_{OL} = 200\text{ mA}$		1.5	2.2	V
Under-Voltage Lockout Output Voltage	$V_{UVLO}$	$V_{CC} = 5\text{ V}$ , $I_{OL} = 1\text{ mA}$		0.7	1.2	V
Output Voltage Rise Time	$t_R$	$C_L = 1\text{ nF}$ , $T_J = 25^\circ\text{C}$		50	150	ns
Output Voltage Fall Time	$t_F$	$C_L = 1\text{ nF}$ , $T_J = 25^\circ\text{C}$		50	150	ns

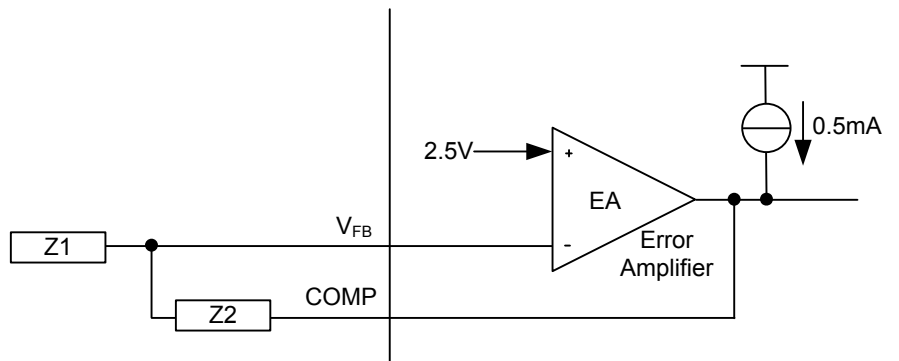
■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>UNDERVOLTAGE-LOCKOUT SECTION</b>						
Startup Threshold	$V_{TH}$		7.8	8.4	9	V
Minimum Operating Voltage After Start-Up	$V_{CC(MIN)}$		7	7.6	8.2	V
<b>PULSE-WIDTH MODULATOR SECTION</b>						
Maximum Duty Cycle	$D_{C(MAX)}$		94	96	100	%
Minimum Duty Cycle	$D_{C(MIN)}$				0	%
<b>SUPPLY VOLTAGE</b>						
Power Startup Supply Current	$I_{CC+I_C}$			0.3	0.5	mA
Power Operating Supply Current	$I_{CC+I_C}$	$V_{FB}$ and $I_{SENSE}$ at 0V		11	17	mA
Power Supply Zener Voltage	$V_Z$	$I_{CC} = 25mA$	30	34		V

- Notes: 1. Adjust  $V_{CC}$  above the start threshold before setting it to 15V.  
 2. Measured at the trip point of the latch, with  $V_{FB}$  at 0V.  
 3. Measured between  $I_{SENSE}$  and COMP, with the input changing from 0V ~ 0.8V.

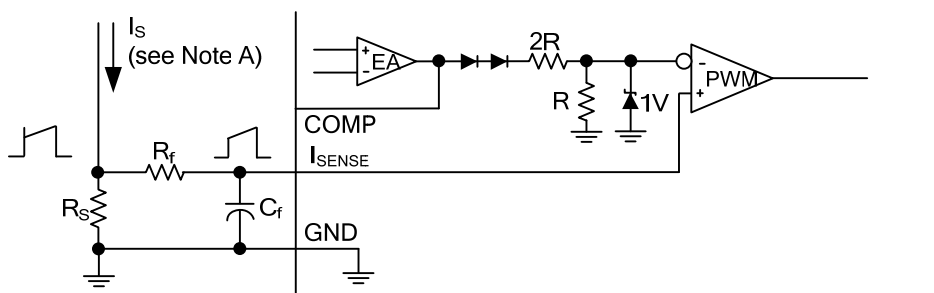
■ APPLICATION INFORMATION

**Error amplifier (EA) configuration circuit:**



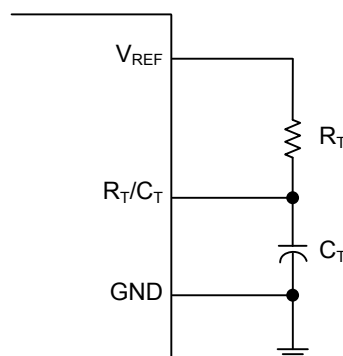
Note: Error amplifier can source or sink up to 0.5mA.

**Current-sense circuit:**



- Notes: 1. Peak current ( $I_S$ ) is determined by the formula:  $I_{S(max)} = 1 / V/R_S$   
 2. A small RC filter formed by resistor  $R_f$  and capacitor  $C_f$  may be required to suppress switch transients.

**The oscillator frequency is set using the circuit:**



The frequency is calculated as followed:

$$f = 1 / R_T C_T$$

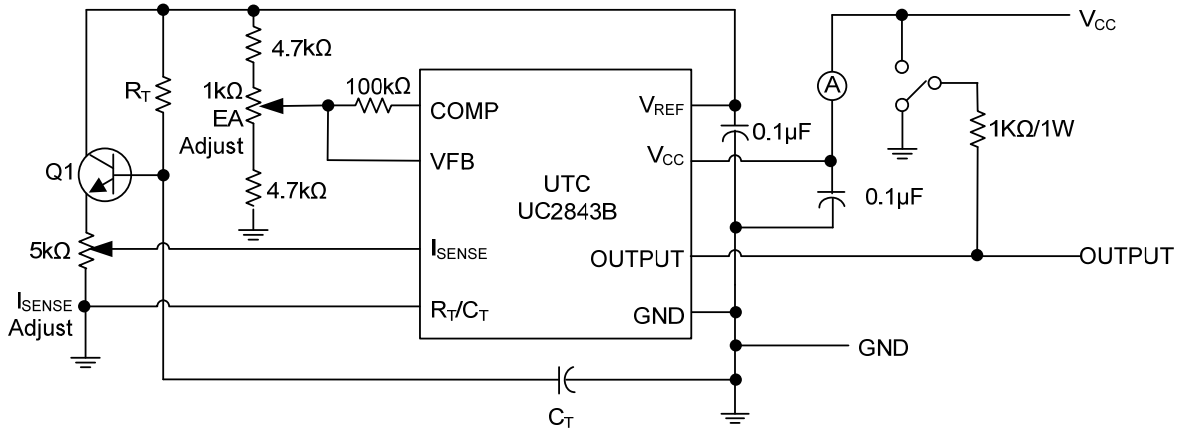
For  $R_T > 5k\Omega$ :

$$f = 1.72 / R_T C_T$$

■ APPLICATION INFORMATION(Cont.)

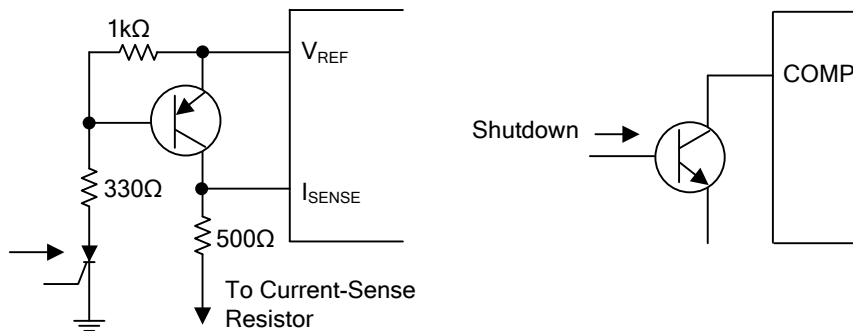
**Open-Loop Laboratory Test Fixture**

In the open-loop laboratory test fixture, high peak currents and loads need grounding techniques. The transistor and 5-k $\Omega$  potentiometer sample the oscillator waveform, applying an adjustable ramp to the I<sub>SENSE</sub> terminal. Timing and bypass capacitors should be connected closely to the GND terminal in a single-point ground.



**Shutdown Technique**

The PWM controller can be shut down through two methods: the one is raising voltage (above 1 V) at I<sub>SENSE</sub>, the other is pulling the COMP terminal below a voltage two diode drops above ground. Either method can leave the output of the PWM comparator high (refer to block diagram). To reset the PWM latch is dominant so the output can stay low in the case of the next clock cycle is coming and the COMP or I<sub>SENSE</sub> terminal is removed beyond this shutdown condition. For example, an externally-latched shutdown can be accomplished by adding an SCR reset by cycling V<sub>CC</sub> below the lower UVLO threshold. So the reference turns off then allows the SCR to reset at this condition.

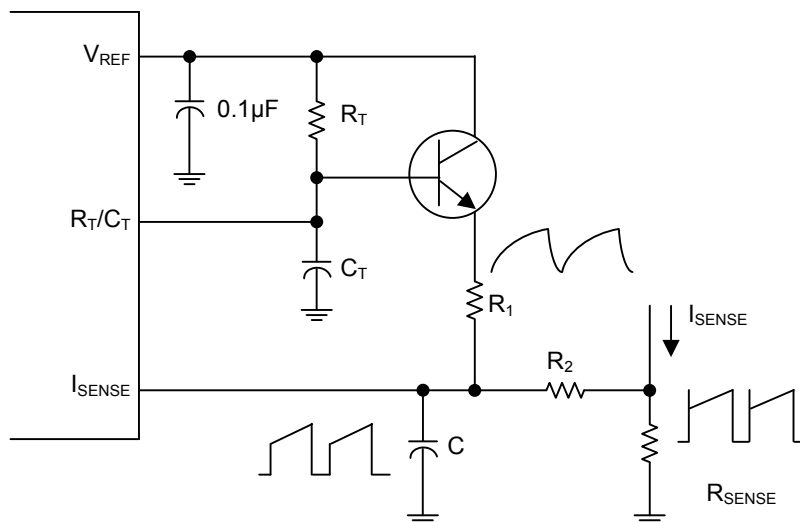




■ APPLICATION INFORMATION(Cont.)

**Shutdown Technique (cont.)**

A fraction of the triangular-wave oscillator can be summed resistively with the current-sense signal providing slope compensation for converters, which requiring duty cycles over 50%. Please note that capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.



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