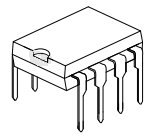
UC3869A

CMOS IC

HIGH VOLTAGE GREEN MODE PWM CONTROLLER



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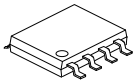


SOP-8

■ DESCRIPTION

The UTC **UC3869A** is a highly integrated current mode PWM control IC with high voltage start up, optimized for high performance, low standby power consumption and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is internally fixed and is trimmed to a tight range. At no load condition, the IC operates in power-saving mode for lower standby power, decreasing frequency for Higher conversion efficiency at light load condition. The internal slope compensation improves system stability at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch, which offering minimal external component count in the design.

The UTC **UC3869A** offers complete protection coverage including Cycle-by-Cycle current limiting (OCP), V_{DD} under voltage lockout (UVLO), over load protection (OLP), over temperature protection (OTP), and over voltage protection (OVP). Excellent EMI performance is achieved with UTC proprietary frequency hopping technique (ZL201020615247.1) together with soft driver control. Audio noise is eliminated due to switch frequency more than 20kHz during operation. The tone energy at below 22 kHz is minimized to avoid audio noise during operation.

■ FEATURES

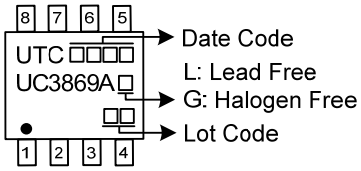
* High voltage startup
* Power on soft start reducing MOSFET Vds stress
* Efficiency and minimum standby power
* Frequency shuffling for EMI
* Audio noise free operation
* Fixed 65 kHz switching frequency
* Comprehensive protection coverage
  V_{DD} Under Voltage Lockout with Hysteresis (UVLO)
  Cycle-by-cycle over current protection (OCP)
  Overload Protection (OLP)
  External programmable Over Temperature Protection (OTP)
  V_{DD} Over voltage Protection(OVP)

■ ORDERING INFORMATION

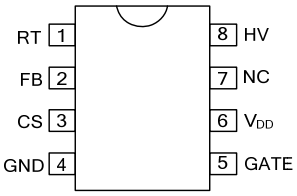
Ordering Number		Package	Packing
Lead Free	Halogen Free		
UC3869AL-D08-T	UC3869AG-D08-T	DIP-8	Tube
UC3869AG-S08-R	UC3869AG-S08-R	SOP-8	Tape Reel

UC3869AG-D08-T (1) Packing Type (2) Package Type (3) Green Package	(1) T: Tube, R: Tape Reel (2) D08: DIP-8, S08: SOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



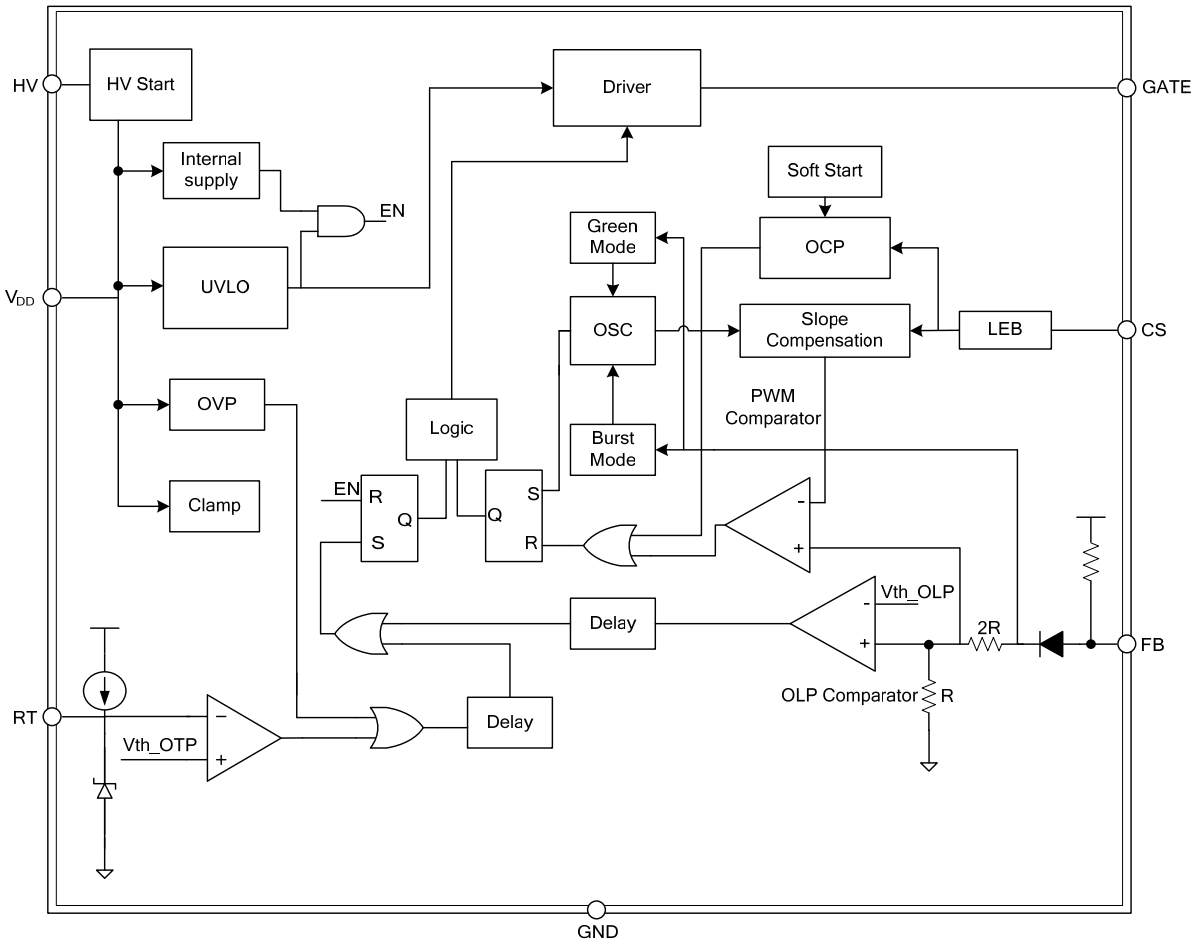
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	RT	Connected through a NTC resistor to ground for over temperature shutdown control
2	FB	Feedback input pin. The PWM duty cycle is determined by voltage level into this pin and the current-sense signal at CS pin
3	CS	Current sense input
4	GND	Ground
5	GATE	Totem-pole gate driver output for power Mosfet
6	V_{DD}	Power Supply
7	NC	
8	HV	Connected to the line input or bulk capacitor via resistors for startup

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
V_{DD} DC Supply Voltage		30	V
High-Voltage Pin, HV		-0.3 ~ 500	V
V_{DD} Zener Clamp Voltage (Note 1)		V_{DD_Clamp}+0.1	V
V_{DD} DC Clamp Current		10	mA
FB Input Voltage		-0.3 ~ 7	V
CS Input Voltage		-0.3 ~ 7	V
RT Input Voltage		-0.3 ~ 7	V
Operating Junction Temperature	T_J	-40 ~ +150	°C
Storage Temperature	T_{STG}	-55 ~ +160	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITION

PARAMETER	SYMBOL	RATINGS	UNIT
V_{DD} Supply Voltage	V_{DD}	10 ~ 24	V
Operating Ambient Temperature	T_A	-20 ~ +85	°C

■ ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{DD}=15V, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current from HV Pin	I_{HV}	V_{DD}=2V, HV=100V		0.75		mA
HV Pin Leakage Current After Startup	leakage	V_{DD}=15V, HV=500V			10	μA
SUPPLY VOLTAGE (V_{DD})						
V_{DD} Start up Current	Istartup	V_{DD}=UVLO(OFF)-1V, Measure Leakage Current into V_{DD}		2	15	μA
Operation Current	$I\_V_{DD\_Operation}$	V_{FB}=3V		0.8	1.8	mA
Start Threshold Voltage	$V_{THD(ON)}$		16.5	18	20	V
Min. Operating Voltage	$V_{DD(MIN)}$		6	7	8	V
VCC Zener Clamp Voltage	V_{DD_clamp}	IV_{DD}=20mA	31	33	35	V
Over Voltage Protection Voltage	$O_{VP(ON)}$	FB=4V Ramp up V_{DD} Until Gate Clock is Off	25	27	29	V
FEEDBACK INPUT SECTION (FB PIN)						
V_{FB} Open Loop Voltage	V_{FB_Open}			5.4		V
PWM Input Gain $\Delta V_{FB} / \Delta V_{CS}$	A_{VCS}			3		V/V
Max Duty Cycle	Maximum Duty Cycle	V_{FB}=3.5V, V_{SENSE}=0	70	78	90	%
Burst-Mode Out FB Voltage	$V_{FB(OUT)}$	V_{SENSE} =0		1.5		V
Burst-Mode Enter FB Voltage	$V_{FB(IN)}$	V_{SENSE} =0		1.35		V
FB Pin Short Circuit Current	I_{FB_Short}	Short FB Pin to GND and Measure Current		240		μA
Power Limiting FB Threshold Voltage	V_{TH_PL}			4.2		V
Power Limiting Debounce Time	T_{D_PL}		60	88	120	mS
OTP Threshold	$T_{(THR)}$			150		°C

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT SENSE INPUT (CS PIN)						
Soft Start Time	SST			5		ms
Leading Edge Blanking Time	T_blanking		200	350	550	ns
Peak Current Flat Threshold Voltage	V_{CS-F}			0.92		V
Peak Current Valley Threshold Voltage	V_{CS-V}	V_{FB}=4.0V, Duty=0%	0.60	0.65	0.70	V
OSCILLATOR						
Normal Oscillation Frequency	F_{OSC}	V_{DD}=15V, FB=3V	60	65	70	kHz
Frequency Jittering	△f_OSC		-9		+9	%
Frequency Temperature Stability	△f_Temp	T=-40~85°C			10	%
Frequency Voltage Stability	△f_V_{DD}				10	%
Burst Mode Switch Frequency	F_Burst		20			kHz
GATE DRIVER						
Output Low Level	V_{OL}	V_{DD}=15V, I_O=20mA			1	V
Output High Level	V_{OH}	V_{DD}=15V, I_O=20mA	11			V
Output Rising Time 1V~10V	T_r	C_L=1000pF		150		nS
Output Falling Time 10V~1V	T_f	C_L=1000pF		60		nS
Over temperature protection						
Output Current of RT Pin	I_{RT}	V_{RT}=0.9V	93	100	107	μA
Threshold Voltage for OTP	V_{TH_OTP}		0.98	1.04	1.10	V

■ OPERATION DESCRIPTION

The UTC **UC3869A** devices integrate many useful designs into one controller for low-power switch-mode power supplies. The following descriptions highlight some of the features of the UTC UC3800 series.

Internal High Voltage Startup and Under Voltage Lockout (UVLO)

UTC **UC3869A** integrated HV start circuit, and provide about 0.25mA current to charge V_{DD} pin during power on state from HV pin. When V_{DD} cap voltage is higher than UVLO(OFF), the charge current is switched off. At this moment, the V_{DD} capacitor provides current to UTC **UC3869A** until the auxiliary winding of the main transformer starts to provide the operation current.

Operating Current

The typical operating current of UTC **UC3869A** is 0.8mA. Good efficiency is achieved with this low operating current together with the 'Extended burst mode' control features.

Soft Start

UTC **UC3869A** features an internal 5ms soft start to soften the electrical stress occurring in the power supply during startup. It is activated during the power on sequence. As soon as V_{DD} reaches UVLO (OFF), the CS peak voltage is gradually increased from 0V to the maximum level. Every restart up begins with a soft start.

Frequency shuffling for EMI improvement

The frequency shuffling (switching frequency modulation) is implemented in UTC **UC3869A**. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

Power-Saving Mode Operation

The proprietary Power-Saving Mode function provides linearly decreasing the switching frequency under light-load conditions for higher efficiency. The feedback voltage, which is sampled from the voltage feedback loop, is taken as the reference. Once the feedback voltage dropped below the threshold voltage, the switching frequency starts to decrease. This Power-Saving Mode function dramatically reduces power consumption under light-load conditions. The 22 kHz minimum frequency control also eliminates the audio noise at any loading conditions.

At zero load condition, the magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy. The UTC **UC3869A** enter burst mode at standby condition to minimize the switching loss and reduces the standby power consumption. Power supplies using the UTC **UC3869A** can easily meet even the strictest regulations regarding standby power consumption.

Oscillator Operation

The switching frequency is internally fixed at 65 kHz. No external frequency setting components are required for PCB design simplification.

Current Sensing and Leading Edge Blanking

Cycle-by-Cycle current limiting is offered in UTC **UC3869A** current mode PWM control. The switching current is detected by a sense resistor connected to the CS pin. An internal leading edge blanking circuit chops off the sensed voltage spikes due to snubber diode reverse recovery and surge gate current of power MOSFET at initial internal power MOSFET on state. The current limiting comparator is disabled and cannot turn off the internal power MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

Internal Synchronized Slope Compensation

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and eliminates the sub-harmonic oscillation and thus reduces the output ripple voltage.

■ OPERATION DESCRIPTION (Cont.)

Gate Output

The UTC **UC3869A** output stage is a fast totem pole gate driver. Cross conduction has been avoided to minimize heat dissipation, increase efficiency, and enhance reliability. A good tradeoff is achieved through dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 16V clamp is added for MOSFET gate protection at higher than expected V_{DD} input.

Protection Controls

The IC takes on more protection functions such as OVP, OLP and OTP etc. In case of those failure modes,the driver works as follows.

OVP

The OVP will shut down the switching of the power MOSFET whenever V_{DD} >V_{OVP}. The OVP event as followed Fig.3.

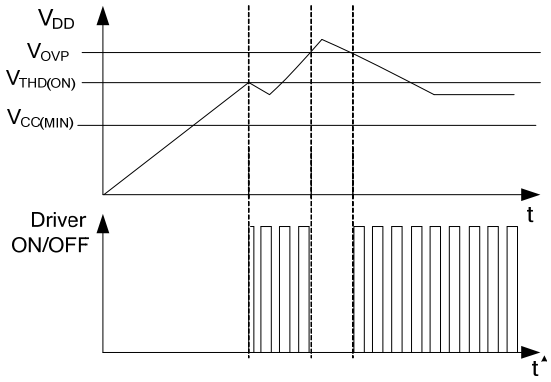


Fig.3 OVP case

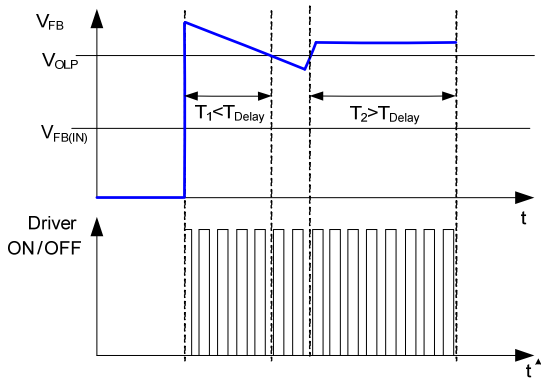


Fig.4 OLP case

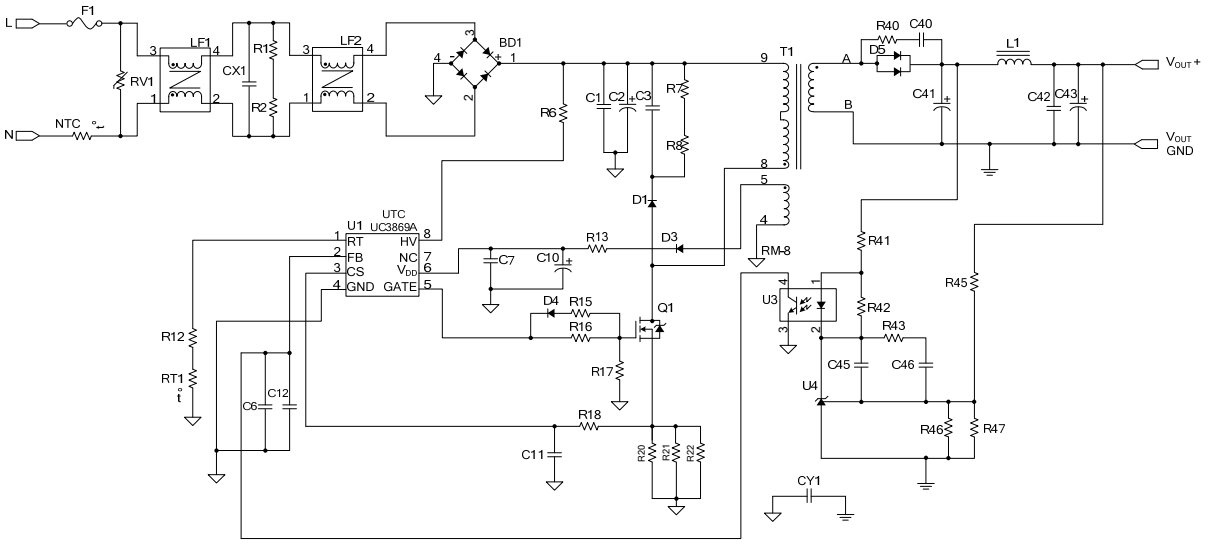
OLP

OLP will shut down driver when V_{FB}> V_{OLP} for continual a blanking time. The OLP event as followed Fig.4.

OTP

OTP will shut down driver when junction temperature T_{RT}<V_{TH_OTP}

■ TYPICAL APPLICATION CIRCUIT (19.5V / 3.07A)



BOM

Reference	Component	Reference	Component
F1	3.15A / 250V	R20, R21	1Ω
RV1	10Φ471	R22	0.68Ω
LF1, LF2	choke	R18	1K
CX1	0.33uF/275VAC	C11	100P/50V
BD1	2A / 600V KBP	T1	RM-10
Q1	UTC 8NM65, 8A/650V, TO-220	D5	MGBR30V200CL , 30A/200V,TO-220
C10	10uF/50V	U3	LTV-357-T-C
R1, R2	1.5M	L1	choke
D1	S1M 1A/1000V	C41, C43	1000uF/25V
R6	100K	C42	1uF/50V
R7, R8	62K	R41	820Ω
D3	BAV20W	R42	2.2K
C1	10nF/1KV	R43	680Ω
C2	120uF/400V	R45	68K ±1%
RT1	10K~100K	R46	10K ±1%
R12	0Ω	R47	N.C
C6, C12	1n/50V	C45	0.47uF/50V
C7	0.1uF/50V	C46	10nF/50V
D4	1N4148 0.15A/75V	U4	TL431 2.495V +-0.5% SOT-23
R13	5.6Ω	R40	47Ω
R15	10Ω	C40	220PF/1KV
R16	47Ω	CY1	Y1, 1000pF/250V
R17	10K	HS1	For D5
U1	PWM UTC UC3869A, SOP-8		