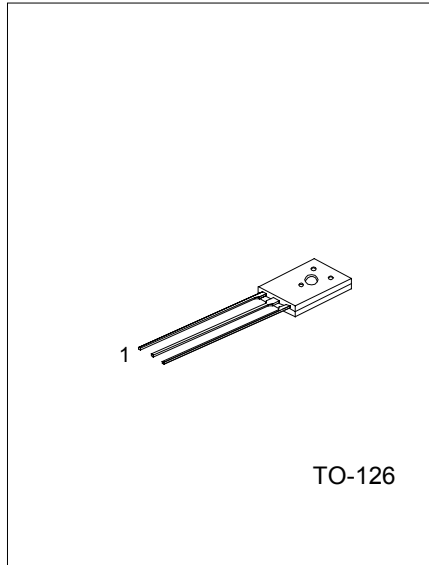
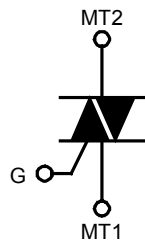


TRIACS

DESCRIPTION

Glass passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

SYMBOL



1:MT1 2:MT2 3:GATE

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Repetitive peak off-state voltages UT134E-5 UT134E-6 UT134E-8	V _{DRM}	500 600* 800	V
RMS on-state current full sine wave; T _{mb} ≤ 107 °C	I _{T(RMS)}	4	A
Non-repetitive peak on-state current (Full sine wave; T _j = 25 °C prior to surge) t = 20ms t = 16.7 ms	I _{TSM}	25 27	A
I ² t for fusing t = 10 ms	I ² t	3.1	A ² s
Repetitive rate of rise of on-state current after triggering I _{TM} = 6 A; I _G = 0.2A; di _G /dt = 0.2A/ μ s	di _T /dt	50 50 50 10	A/ μ s
Peak gate voltage	V _{GM}	5	V
Peak gate current	I _{GM}	2	A
Peak gate power	P _{GM}	5	W
Average gate power (over any 20 ms period)	P _{G(AV)}	0.5	W
Storage temperature	T _{stg}	-40 ~ 150	°C
Operating junction temperature	T _j	125	°C

*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3A/μs.

THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal resistance Junction to mounting base Full cycle Half cycle	$R_{th\ j-mb}$			3.0 3.7	K/W
Thermal resistance Junction to ambient (In free air)	$R_{th\ j-a}$		100		K/W

STATIC CHARACTERISTICS (T_j=25°C, unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Gate trigger current	I_{GT}	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$ T2+ G+ T2+ G- T2- G- T2- G+		2.5 4.0 5.0 11	10 10 10 25	mA
Latching current	I_L	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$ T2+ G+ T2+ G- T2- G- T2- G+		3.0 10 2.5 4.0	15 20 15 20	mA
Holding current	I_H	$V_D = 12\text{ V}; I_{GT} = 0.1\text{ A}$		2.2	15	mA
On-state voltage	V_T	$I_T = 5\text{ A}$		1.4	1.7	V
Gate trigger voltage	V_{GT}	$V_D = 12\text{ V}; I_T = 0.1\text{ A}$ $V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125^\circ\text{C}$	0.25	0.7 0.4	1.5	V
Off-state leakage current	I_D	$V_D = V_{DRM(max)}; T_j = 125^\circ\text{C}$		0.1	0.5	mA

DYNAMIC CHARACTERISTICS (T_j=25°C, unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Critical rate of rise of Off-state voltage	dV_D/dt	$V_{DM} = 67\% V_{DRM(max)}; T_j = 125^\circ\text{C};$ exponential waveform; gate open circuit		50		V/μs
Gate controlled turn-on time	t_{gt}	$I_{TM} = 6\text{ A}; V_D = V_{DRM(max)}; I_G = 0.1\text{ A};$ $dI_G/dt = 5\text{ A}/\mu\text{s}$		2		μs

TYPICAL CHARACTERISTICS

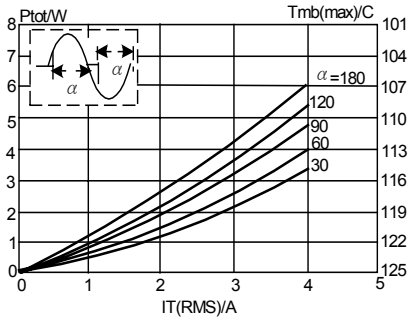


Fig.1. Maximum on-state dissipation, P_{tot} , versus rms on-state current, $I_{T(RMS)}$ where α = conduction angle.

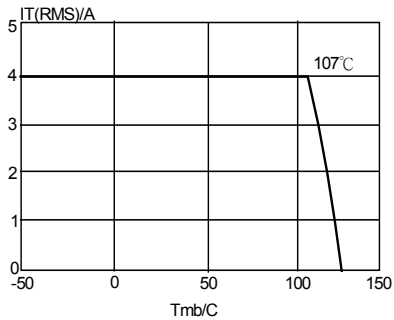


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}

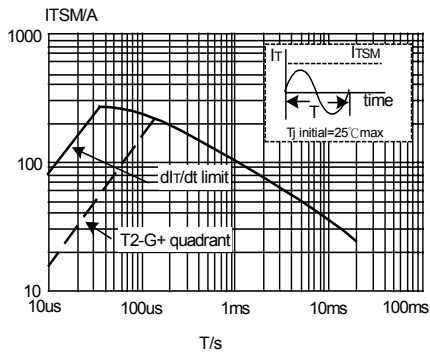


Fig.2. Maximum Permissible non-repetitive peak on-state Current I_{TSM} , versus pulse width t_p for sinusoidal currents, $t_p \leq 20ms$

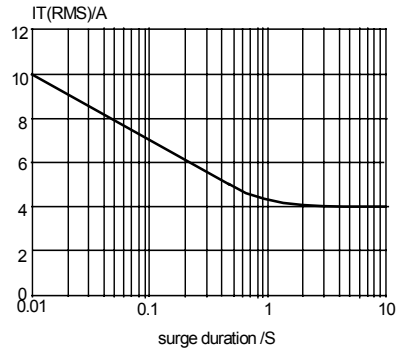


Fig. 5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, $f=50Hz$; $T_{mb} \leq 107^\circ C$

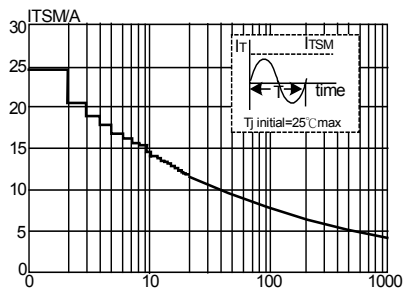


Fig.3. Maximum Permissible non-repetitive peak on-state current I_{TSM} , versus number of cycles, for sinusoidal currents, $f=50Hz$.

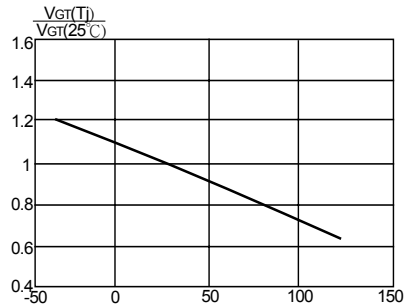


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/V_{GT}(25^\circ C)$, versus junction temperature T_j

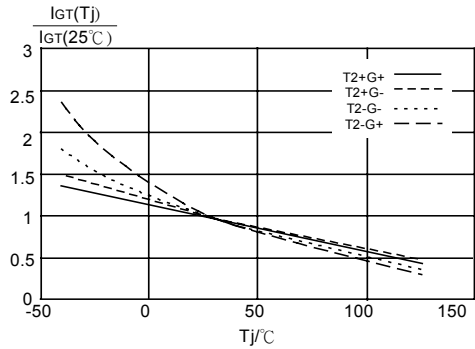


Fig. 7. Normalised gate trigger Current $I_{GT}(T_j)/I_{GT}(25^\circ\text{C})$, versus junction temperature T_j

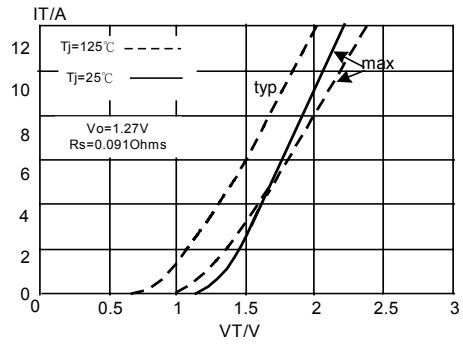


Fig. 10. Typical and maximum on-state characteristic.

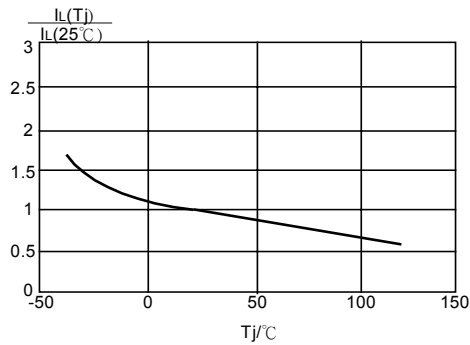


Fig. 8. Normalised latching Current $I_L(T_j)/I_L(25^\circ\text{C})$, versus junction temperature T_j

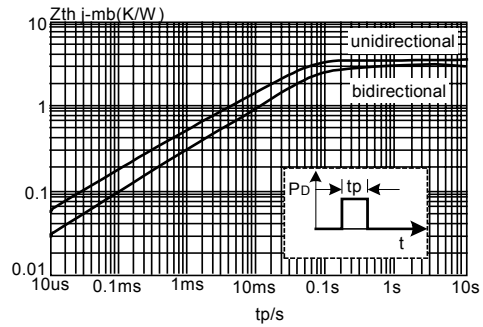


Fig. 11. Transient thermal impedance Z_{thj-mb} , versus pulse width t_p .

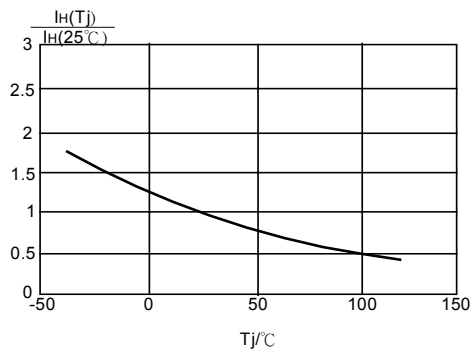


Fig. 9. Normalised holding current $I_H(T_j)/I_H(25^\circ\text{C})$, versus junction temperature T_j

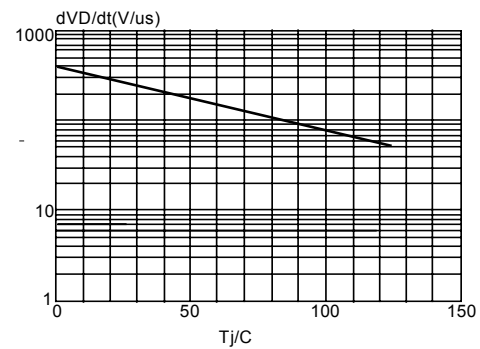


Fig. 12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j

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