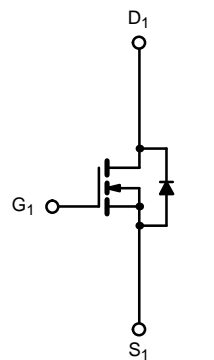
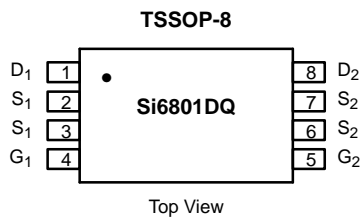




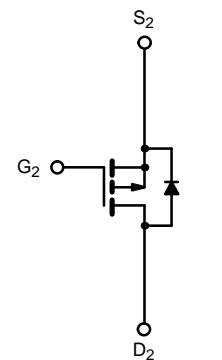
## N- and P-Channel, Reduced $Q_g$ , Fast Switching MOSFET

**High-Efficiency  
PWM Optimized**

PRODUCT SUMMARY			
	$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
N-Channel	20	0.160 @ $V_{GS} = 4.5$ V	$\pm 1.9$
		0.260 @ $V_{GS} = 3.0$ V	$\pm 1.5$
P-Channel	-20	0.190 @ $V_{GS} = -4.5$ V	$\pm 1.7$
		0.280 @ $V_{GS} = -3.0$ V	$\pm 1.3$



N-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage	$V_{DS}$	20	-20	V
Gate-Source Voltage	$V_{GS}$	$\pm 12$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$I_D$	$T_A = 25^\circ\text{C}$	$\pm 1.9$	$\pm 1.7$
		$T_A = 70^\circ\text{C}$	$\pm 1.5$	$\pm 1.3$
Pulsed Drain Current	$I_{DM}$	$\pm 8$		A
Continuous Source Current (Diode Conduction) <sup>a</sup>	$I_S$	1.0	-1.0	
Maximum Power Dissipation <sup>a</sup>	$P_D$	$T_A = 25^\circ\text{C}$	1.0	
		$T_A = 70^\circ\text{C}$	0.64	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	N- or P-Channel	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$R_{thJA}$	125	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board,  $t \leq 10$  sec.



SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)							
Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
<b>Static</b>							
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	N-Ch	0.6			V
		V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA	P-Ch	-0.6			
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±12 V	N-Ch			±100	nA
			P-Ch			±100	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V	N-Ch			1	μA
		V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V	P-Ch			-1	
		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	N-Ch			25	
		V <sub>DS</sub> = -20 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	P-Ch			-25	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 4.5 V	N-Ch	6			A
		V <sub>DS</sub> = -5 V, V <sub>GS</sub> = -4.5 V	P-Ch	-6			
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 1.9 A	N-Ch		0.120	0.160	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -1.7 A	P-Ch		0.155	0.190	
		V <sub>GS</sub> = 3.0 V, I <sub>D</sub> = 1.5 A	N-Ch		0.160	0.260	
		V <sub>GS</sub> = -3.0 V, I <sub>D</sub> = -1.3 A	P-Ch		0.210	0.280	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.9 A	N-Ch		5.4		S
		V <sub>DS</sub> = -15 V, I <sub>D</sub> = -1.7 A	P-Ch		4.0		
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 1.0 A, V <sub>GS</sub> = 0 V	N-Ch		0.77	1.2	V
		I <sub>S</sub> = -1.0 A, V <sub>GS</sub> = 0 V	P-Ch		-0.77	-1.2	
<b>Dynamic<sup>b</sup></b>							
Total Gate Charge	Q <sub>g</sub>	N-Channel V <sub>DS</sub> = 3.5 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 0.3 A  P-Channel V <sub>DS</sub> = -3.5 V, V <sub>GS</sub> = -4.5 V I <sub>D</sub> = -0.3 A	N-Ch		1.7	3.5	nC
Gate-Source Charge	Q <sub>gs</sub>		P-Ch		3.5	7.0	
Gate-Drain Charge	Q <sub>gd</sub>		N-Ch		0.26		
Turn-On Delay Time	t <sub>d(on)</sub>	N-Channel V <sub>DD</sub> = 3.5 V, R <sub>L</sub> = 11.5 Ω I <sub>D</sub> ≅ 0.3 A, V <sub>GEN</sub> = 4.5 V, R <sub>G</sub> = 6 Ω  P-Channel V <sub>DD</sub> = -3.5 V, R <sub>L</sub> = 11.5 Ω I <sub>D</sub> ≅ -0.3 A, V <sub>GEN</sub> = -4.5 V, R <sub>G</sub> = 6 Ω	N-Ch		7.3	15	ns
			P-Ch		6.0	15	
Rise Time	t <sub>r</sub>		N-Ch		10.0	20.0	
			P-Ch		10.0	20.0	
Turn-Off Delay Time	t <sub>d(off)</sub>		N-Ch		11.0	20.0	
			P-Ch		10.0	20.0	
Fall Time	t <sub>f</sub>		N-Ch		6.0	15	
			P-Ch		7.0	15	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	N-Channel—I <sub>F</sub> = 1.0 A, di/dt = 100 A/μs	N-Ch		31	60	
		P-Channel—I <sub>F</sub> = -1.0 A, di/dt = 100 A/μs	P-Ch		35	60	

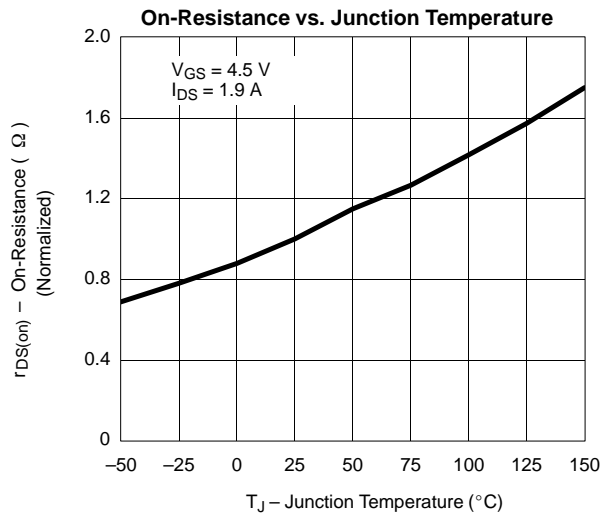
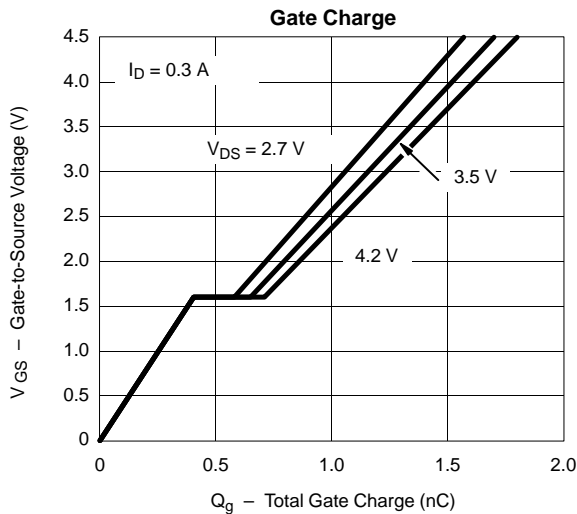
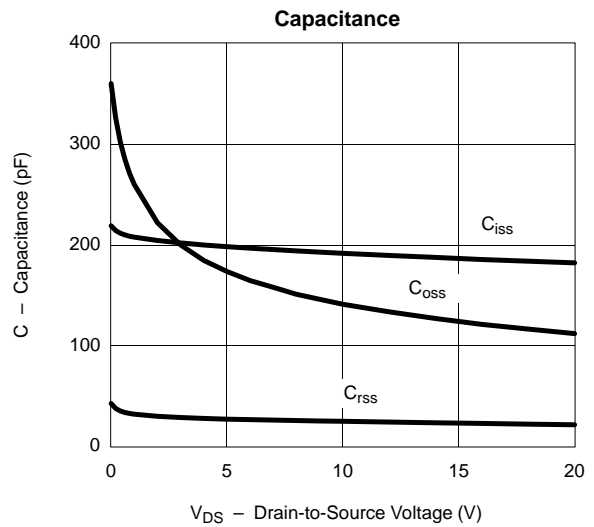
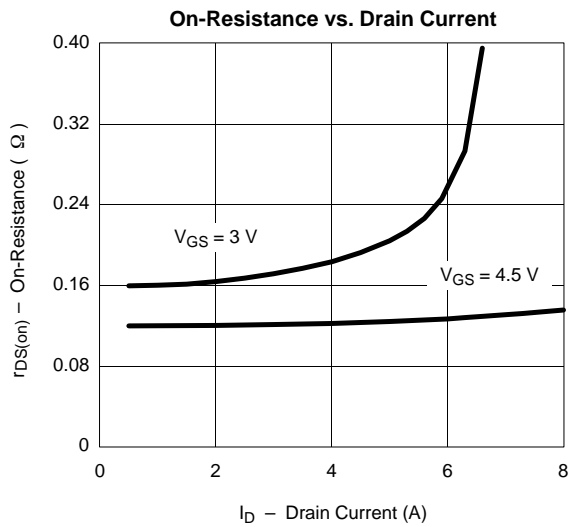
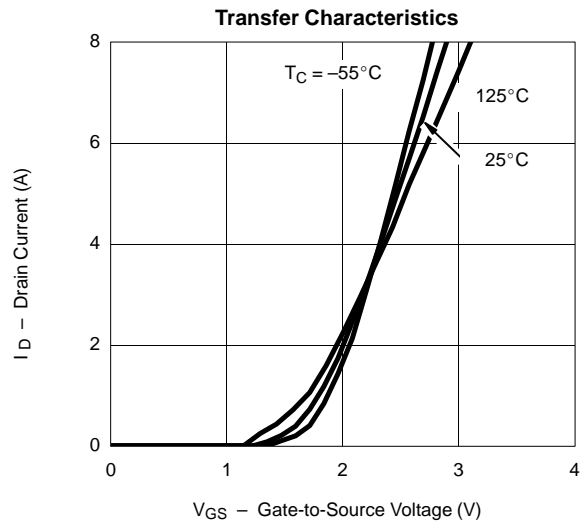
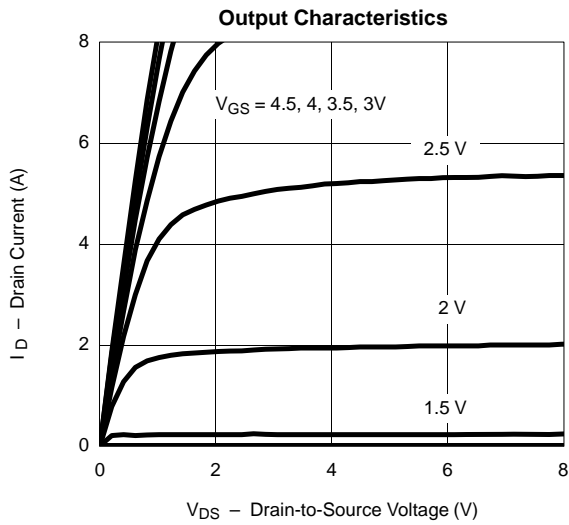
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

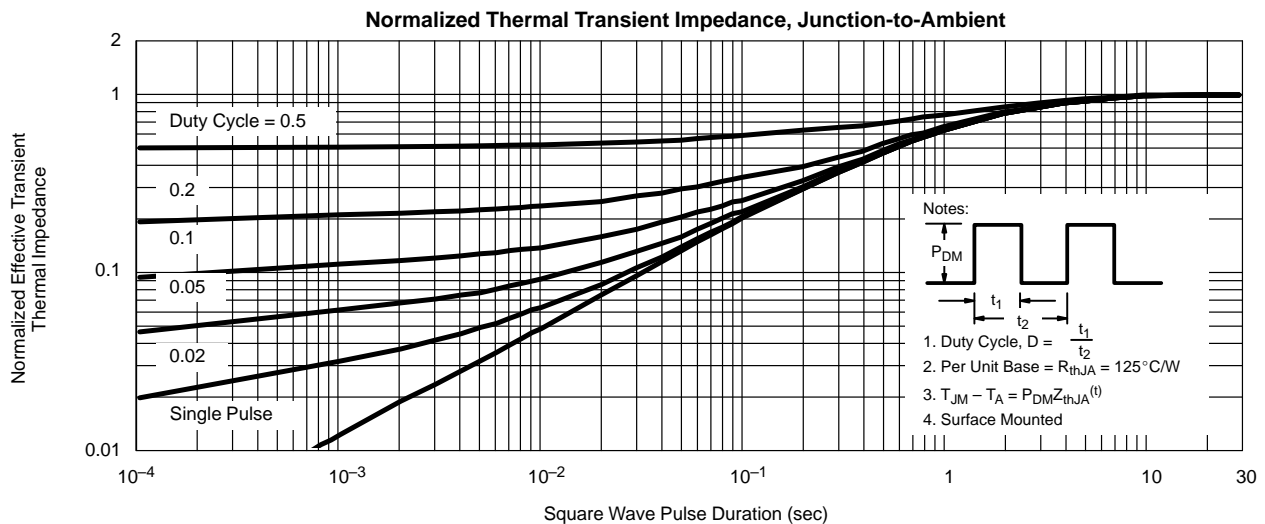
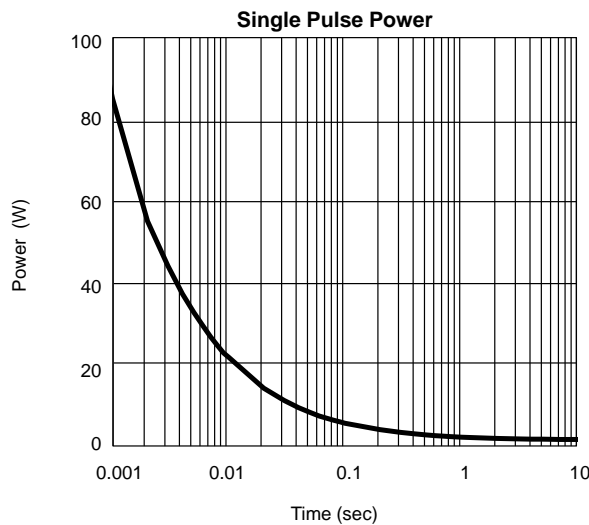
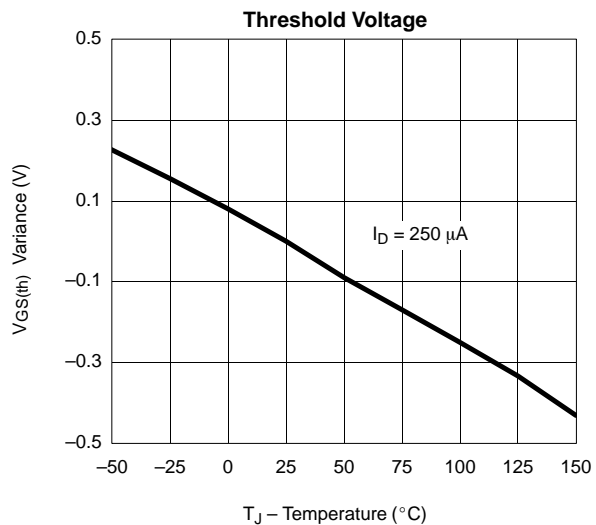
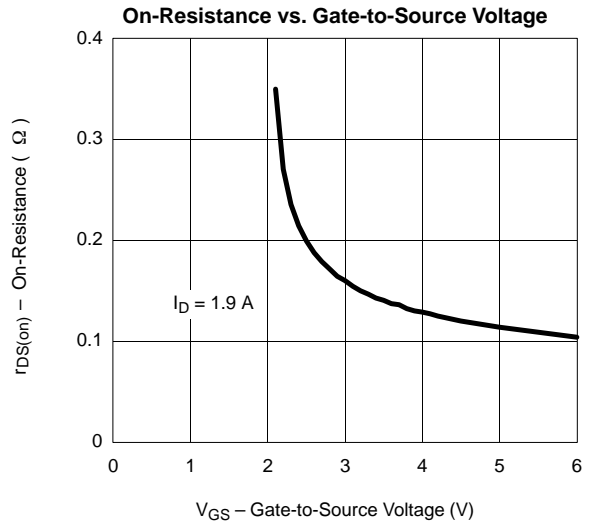
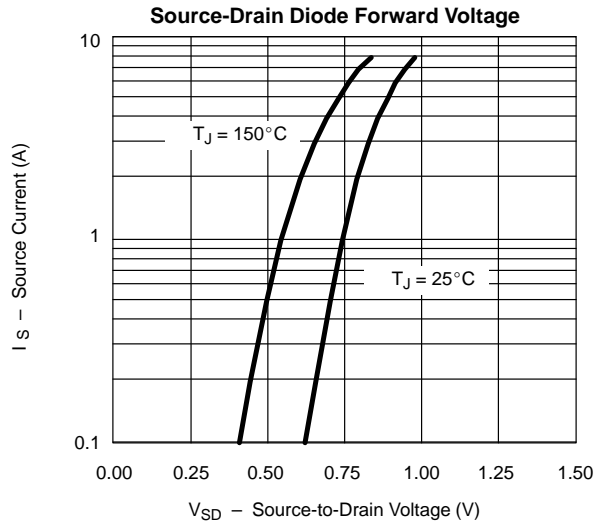


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**N-CHANNEL**



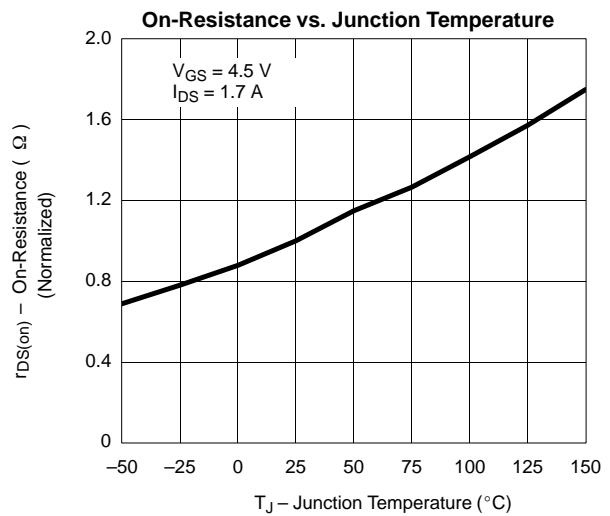
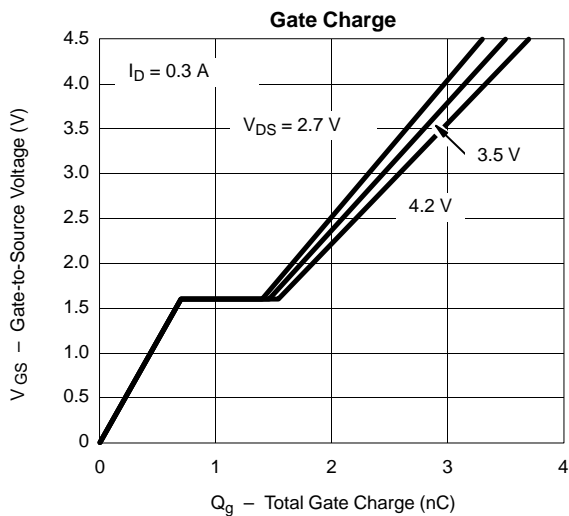
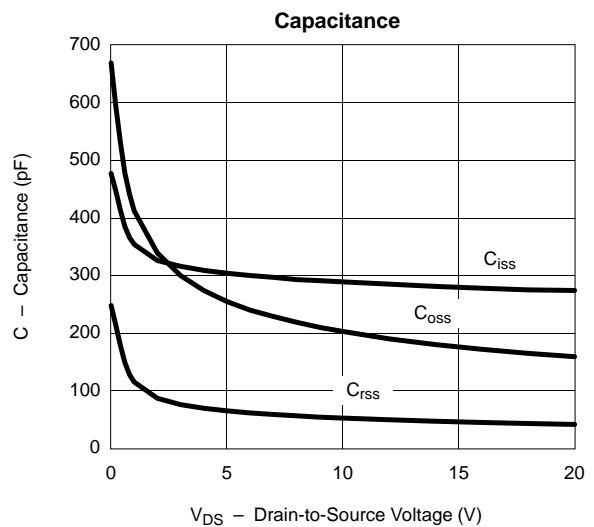
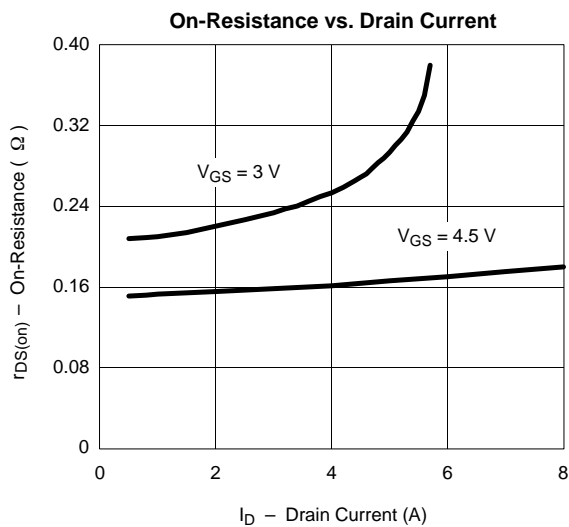
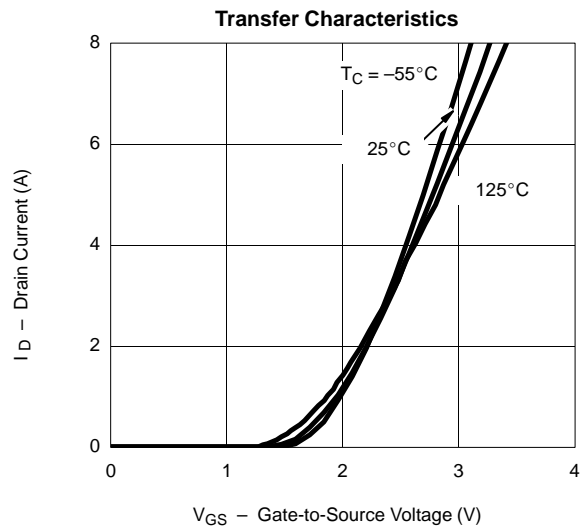
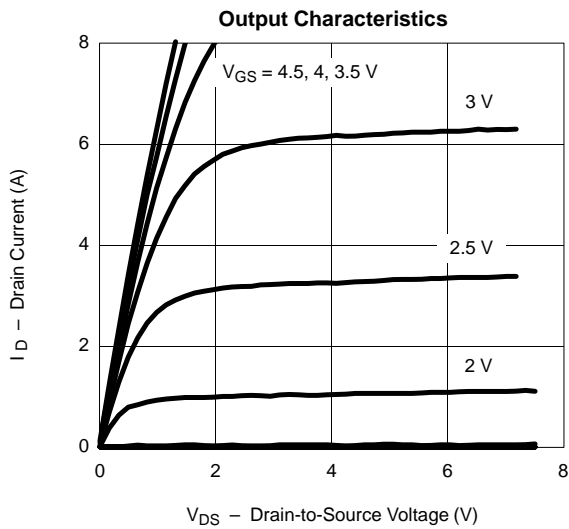
**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED) N-CHANNEL**



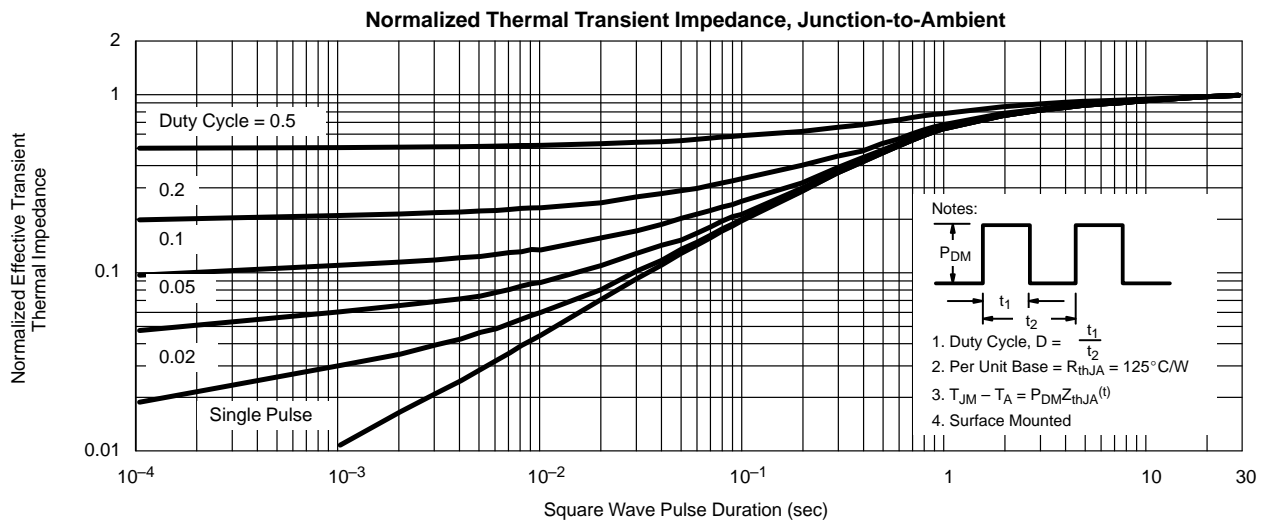
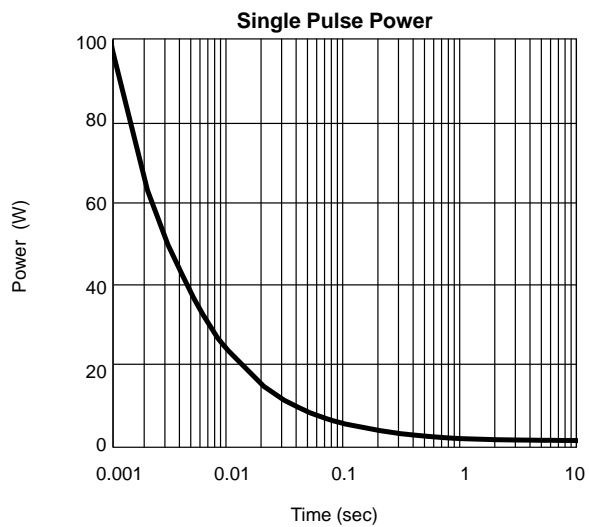
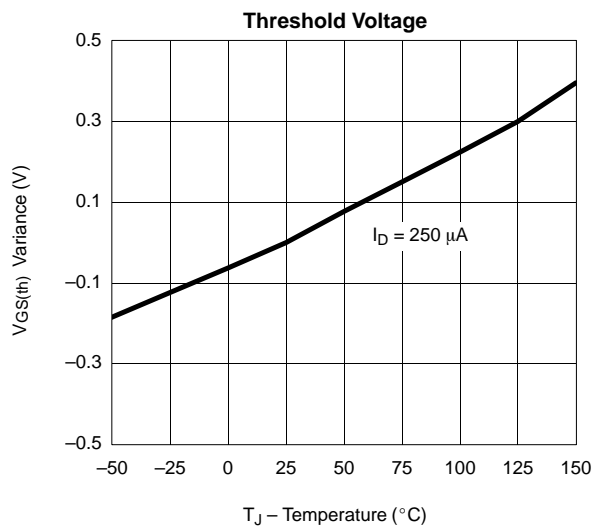
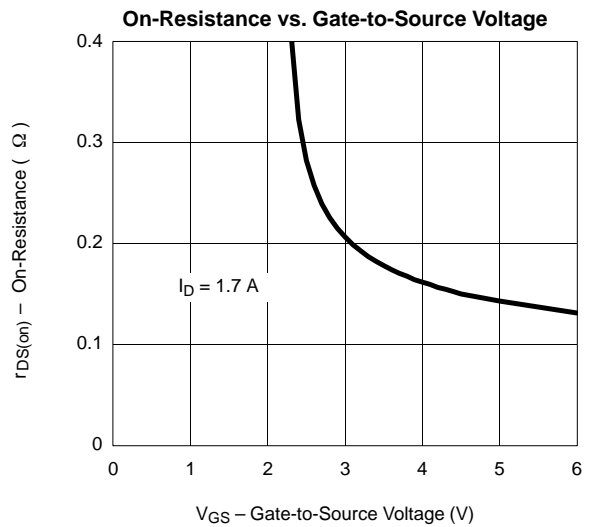
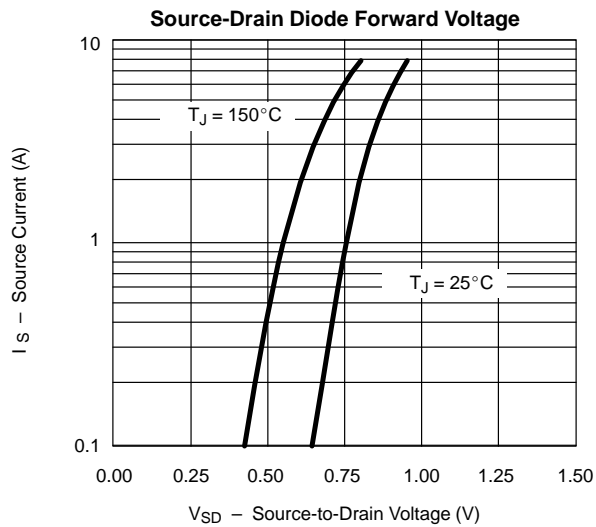


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

**P-CHANNEL**



**TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED) P-CHANNEL**





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