TwinDie™ 1.35V Automotive DDR3L SDRAM

MT41K512M16 – 64 Meg x 16 x 8 Banks

Description

The 8Gb (TwinDie™) DDR3L SDRAM (1.35V) uses two Micron 4Gb DDR3L SDRAM x8 die for a 2 byte x16 device in one package. Refer to Micron's 4Gb DDR3L SDRAM data sheet (x8 option) for specifications not included in this document, specifications for base part number MT41K512M8 correlate to TwinDie manufacturing base part number MT41K512M16.

Features

- Uses two x8, 4Gb Micron die to make one x16 package
  - Single rank TwinDie
  - One external ZQ ball and one internal ZQ connected to V_{SSQ} through an embedded serial resistor
- $V_{DD} = V_{DDQ} = 1.35V$ (1.283–1.45V)
- Backward compatible to $V_{DD} = V_{DDQ} = 1.5V \pm 0.075V$
- Differential bidirectional data strobe
- 8*n*-bit prefetch architecture
- Differential clock inputs (CK, CK#)
- 8 internal banks
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Programmable CAS (READ) latency (CL)
- Programmable posted CAS additive latency (AL)
- Programmable CAS (WRITE) latency (CWL)
- Fixed burst length (BL) of 8 and burst chop (BC) of 4 (via the mode register set [MRS])
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self refresh mode
- T_C of –40°C to +105°C
  - 64ms, 8192-cycle refresh at –40°C to +85°C
  - 32ms at +85°C to +105°C
- Self refresh temperature (SRT)
- Automatic self refresh (ASR)
- Write leveling
- Multipurpose register
- Output driver calibration
- AEC-Q100
- PPAP submission
- 8D response time

Options

Options	Marking
• Configuration	
– 512 Meg x 16	512M16
• TFBGA package (Pb-free) – x16	
– 96-ball (8mm x 14mm)	VRN
• Timing – cycle time	
– 1.07ns @ CL = 13 (DDR3-1866)	-107
• Product certification	
– Automotive	A
• Operating temperature	
– Industrial (–40°C ≤ T_C ≤ +95°C)	IT
– Automotive (–40°C ≤ T_C ≤ +105°C)	AT
• Revision	:P

Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

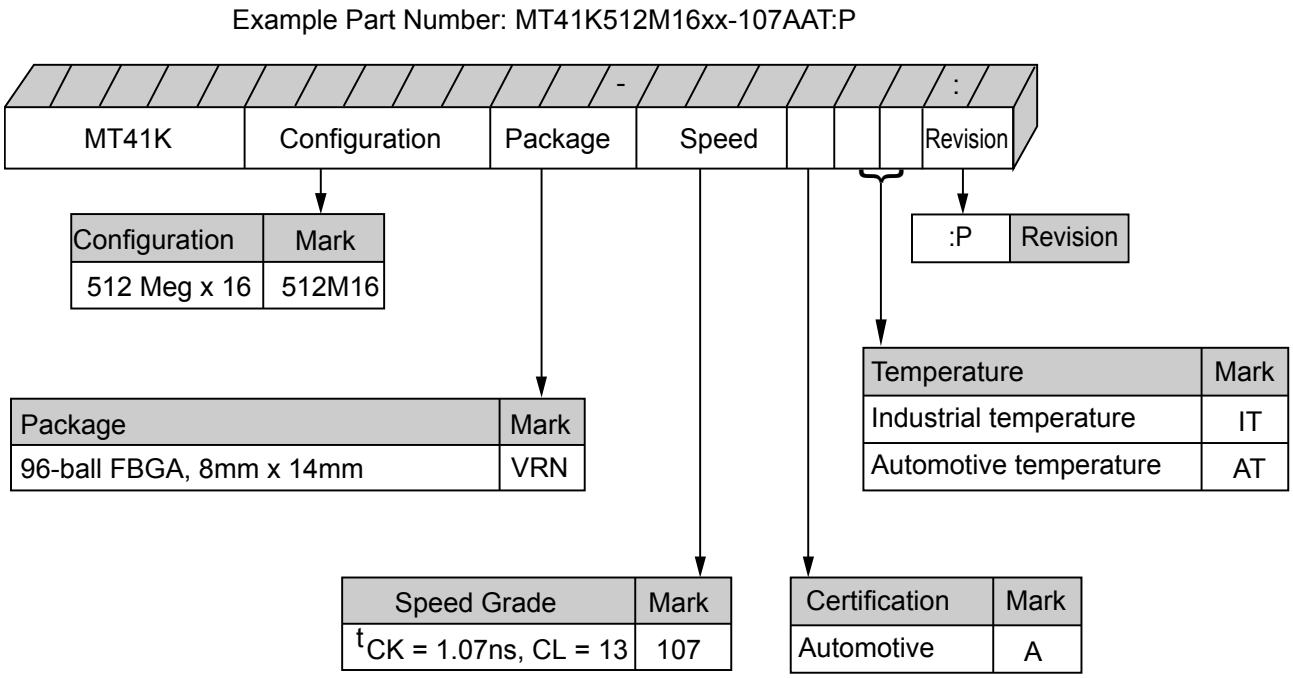
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)	Target ^{t}RCD-^{t}RP-CL	^{t}RCD (ns)	^{t}RP (ns)	CL (ns)
-107	1866	13-13-13	13.91	13.91	13.91

Table 2: Addressing

Parameter	512 Meg x 16
Configuration	64 Meg x 8 x 8 banks x 2 die
Die per package	2
Refresh count	8K
Row address	64K (A[15:0])
Bank address	8 (BA[2:0])
Column address	1K (A[9:0])
Page size per die	1KB

Figure 1: DDR3L Part Numbers



Note: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.

FBGA Part Marking Decoder

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. For a quick conversion of an FBGA code, see the FBGA Part Marking Decoder on Micron's Web site: http://www.micron.com.

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Functional Description

The TwinDie DDR3L SDRAM is a high-speed, CMOS dynamic random access memory device internally configured as two 8-bank DDR3L SDRAM devices.

Although each die is tested individually within the dual-die package, some TwinDie test results may vary from a like die tested within a monolithic die package.

The DDR3L SDRAM uses a double data rate architecture to achieve high-speed operation. The double data rate architecture is an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O balls. A single read or write access consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O balls.

The differential data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the DDR3L SDRAM input receiver. DQS is center-aligned with data for WRITEs. The read data is transmitted by the DDR3L SDRAM and edge-aligned to the data strobes.

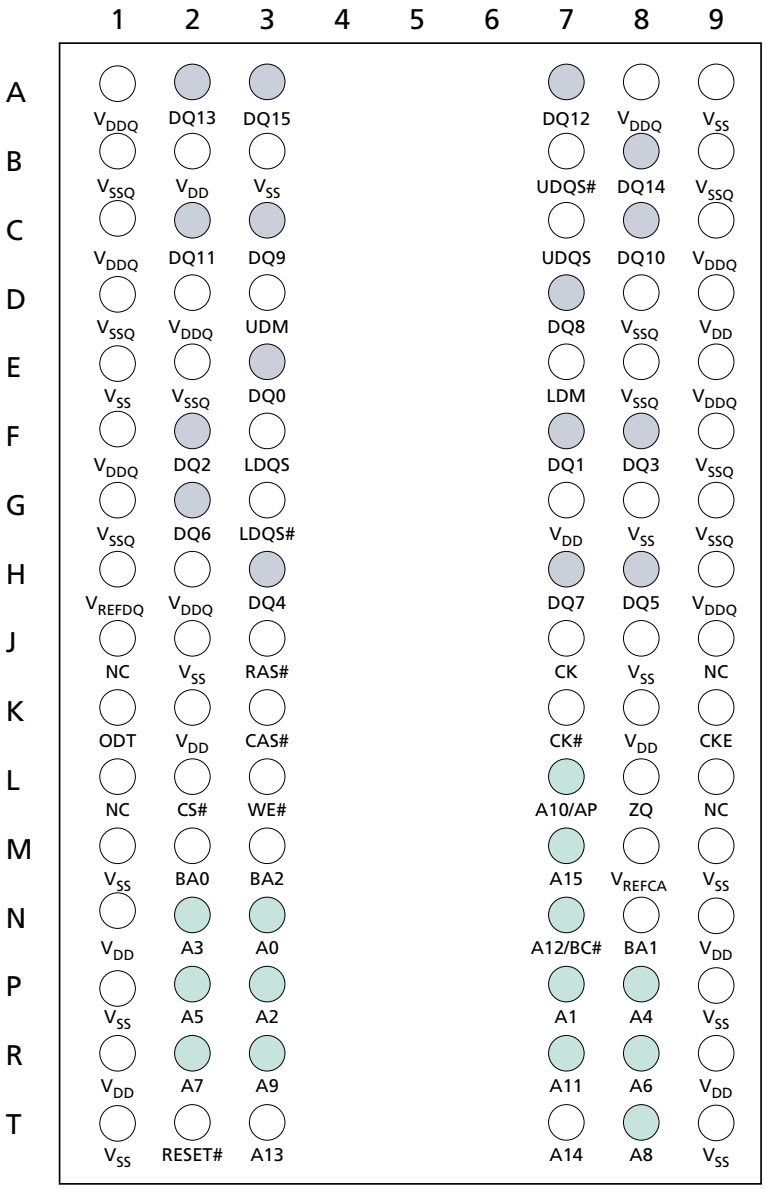
The DDR3 SDRAM operates from a differential clock (CK and CK#). The crossing of CK going HIGH and CK# going LOW is referred to as the positive edge of CK. Control, command, and address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

Read and write accesses to the DDR3L SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and row to be accessed. The address bits (including CS*n*#, BA*n*, and A*n*) registered coincident with the READ or WRITE command are used to select the rank, bank, and starting column location for the burst access.

This data sheet provides a general description, package dimensions, and the package ballout. Refer to the Micron monolithic DDR3L data sheet for complete information regarding individual die initialization, register definition, command descriptions, and die operation.

Ball Assignments and Descriptions

Figure 2: 96-Ball FBGA – x16 (Top View)



Notes:
1. Ball descriptions listed in Table 3 are listed as "x4, x8" if unique; otherwise, x4 and x8 are the same.
2. A comma separates the configuration; a slash defines a selectable function. Example D7 = NF, NF/TDQS#. NF applies to the x4 configuration only. NF/TDQS# applies to the x8 configuration only—selectable between NF or TDQS# via MRS (symbols are defined in Table 3).

Table 3: 96-Ball FBGA – x16 Ball Descriptions

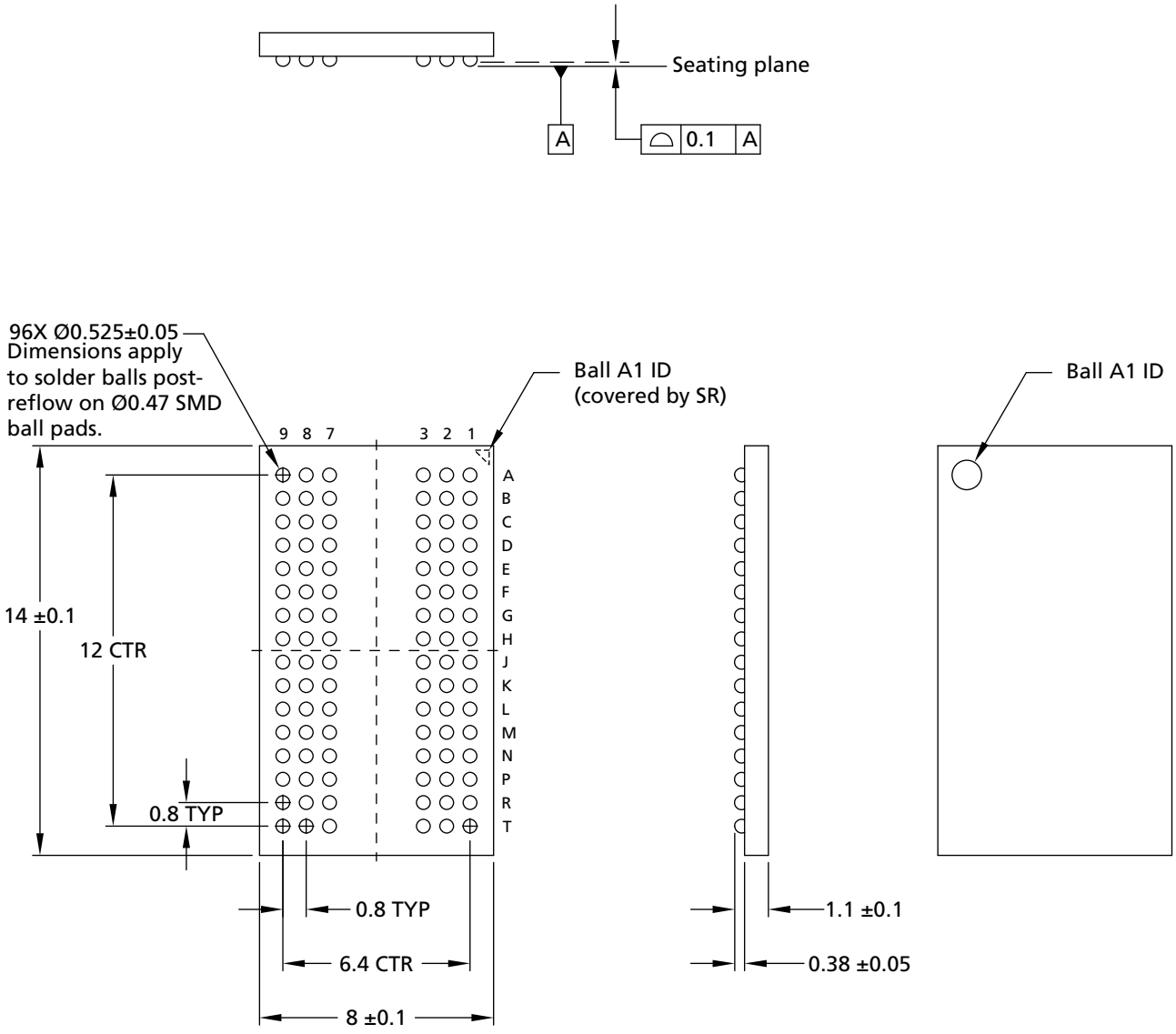
Symbol	Type	Description
A[15:13], A12/BC#, A11, A10/AP, A[9:0]	Input	**Address inputs:** Provide the row address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BA[2:0]) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to V_{REFCA}. A12/BC#: When enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop (on-the-fly) will be performed (HIGH = BL8 or no burst chop, LOW = BC4). See the Truth Table – Command section.
BA[2:0]	Input	**Bank address inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to V_{REFCA}.
CK, CK#	Input	**Clock:** CK and CK# are differential clock inputs. All control and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data strobe (DQS, DQS#) is referenced to the crossings of CK and CK#.
CKE	Input	**Clock enable:** CKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle),or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CK, CK#, CKE, RESET#, and ODT) are disabled during POWER-DOWN. Input buffers (excluding CKE and RESET#) are disabled during SELF REFRESH. CKE is referenced to V_{REFCA}.
CS#	Input	**Chip select:** CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external rank selection on systems with multiple ranks. CS# is considered part of the command code. CS# is referenced to V_{REFCA}.
LDM	Input	**Input data mask:** LDM is a lower-byte, input mask signal for write data. Lower-byte input data is masked when LDM is sampled HIGH along with the input data during a write access. Although the LDM ball is input-only, the LDM loading is designed to match that of the DQ and DQS balls. LDM is referenced to V_{REFDQ}.
ODT	Input	**On-die termination:** ODT enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following balls: DQ[15:0], LDQS, LDQS#, UDQS, UDQS#, LDM, and UDM for the x16; DQ0[7:0], DQS, DQS#, DM/TDQS, and NF/TDQS# (when TDQS is enabled) for the x8; DQ[3:0], DQS, DQS#, and DM for the x4. The ODT input is ignored if disabled via the LOAD MODE command. ODT is referenced to V_{REFCA}.
RAS#, CAS#, WE#	Input	**Command inputs:** RAS#, CAS#, and WE# (along with CS#) define the command being entered and are referenced to V_{REFCA}.

Table 3: 96-Ball FBGA – x16 Ball Descriptions (Continued)

Symbol	Type	Description
RESET#	Input	**Reset:** RESET# is an active LOW CMOS input referenced to V_{SS}. The RESET# input receiver is a CMOS input defined as a rail-to-rail signal with DC HIGH ≥ 0.8 × V_{DD} and DC LOW ≤ 0.2 × V_{DDQ}. RESET# assertion and desertion are asynchronous.
UDM	Input	**Input data mask:** UDM is an upper-byte, input mask signal for write data. Upper-byte input data is masked when UDM is sampled HIGH along with that input data during a WRITE access. Although the UDM ball is input-only, the UDM loading is designed to match that of the DQ and DQS balls. UDM is referenced to V_{REFDQ}.
DQ[7:0]	I/O	**Data input/output:** Lower byte of bidirectional data bus for the x16 configuration. DQ[7:0] are referenced to V_{REFDQ}.
DQ[15:8]	I/O	**Data input/output:** Upper byte of bidirectional data bus for the x16 configuration. DQ[15:8] are referenced to V_{REFDQ}.
LDQS, LDQS#	I/O	**Lower byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. Center-aligned to write data.
UDQS, UDQS#	I/O	**Upper byte data strobe:** Output with read data. Edge-aligned with read data. Input with write data. DQS is center-aligned to write data.
V_{DD}	Supply	**Power supply:** 1.35V (1.283–1.45V) / 1.5V ±0.075V (backward compatible).
V_{DDQ}	Supply	**DQ power supply:** 1.35V (1.283–1.45V) / 1.5V ±0.075V (backward compatible). Isolated on the device for improved noise immunity.
V_{REFCA}	Supply	**Reference voltage for control, command, and address:** V_{REFCA} must be maintained at all times (including self refresh) for proper device operation.
V_{REFDQ}	Supply	**Reference voltage for data:** V_{REFDQ} must be maintained at all times (excluding self refresh) for proper device operation.
V_{SS}	Supply	Ground.
V_{SSQ}	Supply	**DQ ground:** Isolated on the device for improved noise immunity.
ZQ	Reference	**External reference ball for output drive calibration:** This ball is tied to an external 240Ω resistor (RZQ), which is tied to V_{SSQ}.
NC	–	**No connect:** These balls should be left unconnected (the ball has no connection to the DRAM or to other balls).

Package Dimensions

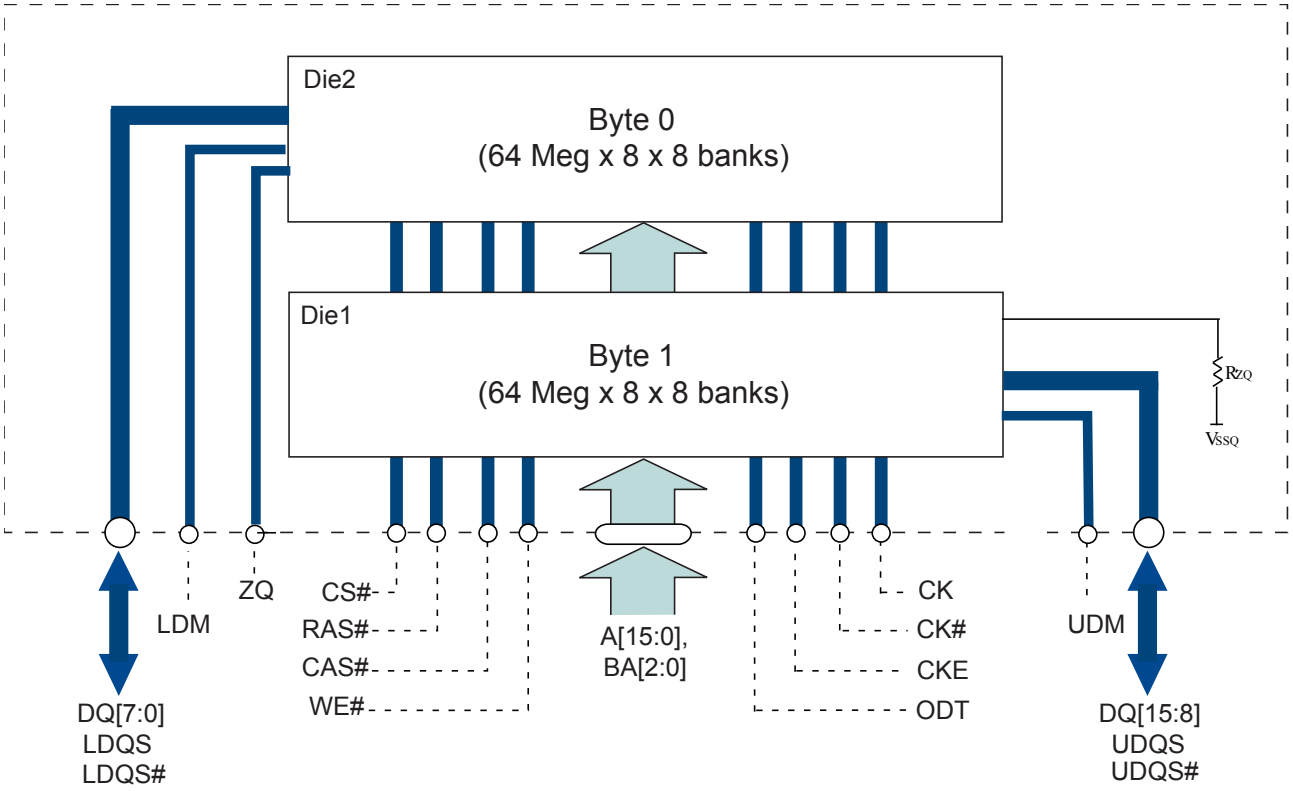
Figure 3: 96-Ball FBGA – x16



Notes:
1. All dimensions are in millimeters.
2. Material composition: Pb-free SAC302 (96.8% Sn, 3% Ag, 0.2% Cu).

Functional Block Diagram

Figure 4: Functional Block Diagram (512Meg x 16)



Thermal Characteristics

Table 4: Thermal Characteristics

Notes 1–3 apply to entire table

Parameter	Symbol	Value	Units	Notes
Operating case temperature – Industrial	T_C	–40 to +95	°C	1, 2, 3, 4
Operating case temperature – Automotive	T_C	–40 to +105	°C	1, 2, 3, 4
Operating case temperature – Ultra-high	T_C	–40 to +125	°C	1, 2, 3, 4 ,5

Notes:
1. MAX operating case temperature T_C is measured in the center of the package, as shown below.
2. A thermal solution must be designed to ensure that the device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the device exceeds maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2x refresh, which is a 3.9µs interval refresh rate. The use of SRT or ASR must be enabled.
5. Ultra-high temperature use based on automotive usage model. Please contact Micron sales representative if you have questions.

Figure 5: Thermal Measurement Point

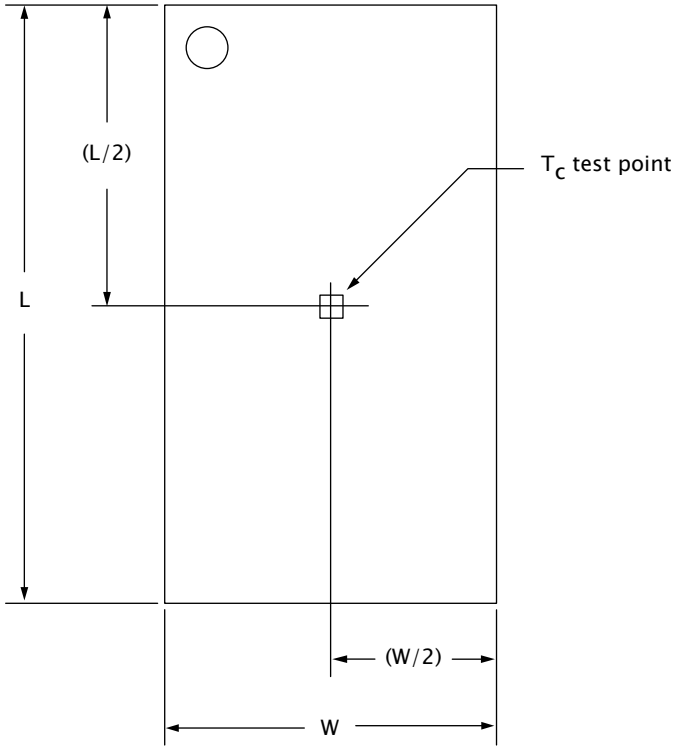


Table 5: Thermal Impedance

Die Rev.	Package	Substrate	Θ_{JA} (°C/W)			Θ_{JB} (°C/W)	Θ_{JC} (°C/W)
			Airflow = 0m/s	Airflow = 1m/s	Airflow = 2m/s		
P	96-ball	Low conductivity	52.2	41.1	36.7	N/A	4.9
		High conductivity	33.9	28.7	26.9	19.0	N/A

Note: 1. Thermal resistance data is based on a number of samples from multiple lots and should be viewed as a typical number.

Electrical Specifications

Absolute Ratings

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.975	V	1
V_{DDQ}	V_{DD} supply voltage relative to V_{SSQ}	–0.4	1.975	V	
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.975	V	
T_C	Operating case temperature – Commercial	0	95	°C	2, 3
	Operating case temperature – Industrial	–40	95	°C	2, 3
	Operating case temperature – Automotive	–40	105	°C	2, 3
T_{STG}	Storage temperature	–55	150	°C	

Notes:
1. V_{DD} and V_{DDQ} must be within 300mV of each other at all times, and V_{REF} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are <500mV, V_{REF} can be ≤300mV.
2. MAX operating case temperature. T_C is measured in the center of the package.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. Ultra-high temperature use based on automotive usage model. Please contact Micron sales representative if you have questions.

Input/Output Capacitance

Table 7: DDR3L Input/Output Capacitance

Note 1 applies to the entire table

Capacitance Parameters	Sym	DDR3L -1866		Unit	Notes
		Min	Max		
CK and CK#	C_{CK}	2.4	4.0	pF	
ΔC: CK to CK#	C_{DCK}	0.0	0.3	pF	
Single-end I/O: DQ, DM	C_{IO}	2.8	4.2	pF	2
Differential I/O: DQS, DQS#, TDQS, TDQS#	C_{IO}	2.8	4.2	pF	3
ΔC: DQS to DQS#, TDQS, TDQS#	C_{DDQS}	0.0	0.3	pF	3
ΔC: DQ to DQS	C_{DIO}	–1.0	0.6	pF	4
Inputs (CTRL, CMD, ADDR)	C_I	2.4	4.6	pF	5
ΔC: CTRL to CK	C_{DI_CTRL}	–0.8	0.8	pF	6
ΔC: CMD_ADDR to CK	$C_{DI\_CMD\_ADDR}$	–0.8	0.8	pF	7
ZQ pin capacitance	C_{ZQ}	–	6.1	pF	
Reset pin capacitance	C_{RE}	–	6.0	pF	

Notes:
1. V_{DD} = 1.35V (1.283–1.45V), V_{DDQ} = V_{DD}, V_{REF} = V_{SS}, *f* = 100 MHz, T_C = 25°C. $V_{OUT(DC)}$ = 0.5 × V_{DDQ}, V_{OUT} = 0.1V (peak-to-peak).
2. DM input is grouped with I/O pins, reflecting the fact that they are matched in loading.
3. Includes TDQS, TDQS#. C_{DDQS} is for DQS vs. DQS# and TDQS vs. TDQS# separately.
4. $C_{DIO} = C_{IO(DQ)} - 0.5 \times (C_{IO(DQS)} + C_{IO(DQS\#)})$.
5. Excludes CK, CK#; CTRL = ODT, CS#, and CKE; CMD = RAS#, CAS#, and WE#; ADDR = A[*n*:0], BA[2:0].
6. $C_{DI\_CTRL} = C_{I(CTRL)} - 0.5 \times (C_{CK(CK)} + C_{CK(CK\#)})$.
7. $C_{DI\_CMD\_ADDR} = C_{I(CMD\_ADDR)} - 0.5 \times (C_{CK(CK)} + C_{CK(CK\#)})$.

Electrical Specifications – I_{CDD} Parameters

Table 8: DDR3L I_{CDD} Specifications and Conditions (Rev. P)

Notes 1 and 2 apply to the entire table

Combined Symbol	Individual Die Status	Bus Width	-107	Units
I_{CDD0}	$I_{CDD0} = 2 \times I_{DD0}$	x16	58	mA
I_{CDD1}	$I_{CDD1} = 2 \times I_{DD1}$	x16	88	mA
I_{CDD2P0} (slow exit)	$I_{CDD2P0} = 2 \times I_{DD2P0}$	x16	22	mA
I_{CDD2P1} (fast exit)	$I_{CDD2P1} = 2 \times I_{DD2P1}$	x16	22	mA
I_{CDD2Q}	$I_{CDD2Q} = 2 \times I_{DD2Q}$	x16	30	mA
I_{CDD2N}	$I_{CDD2N} = 2 \times I_{DD2N}$	x16	34	mA
I_{CDD2NT}	$I_{CDD2NT} = 2 \times I_{DD2NT}$	x16	44	mA
I_{CDD3P}	$I_{CDD3P} = 2 \times I_{DD3P}$	x16	30	mA
I_{CDD3N}	$I_{CDD3N} = 2 \times I_{DD3N}$	x16	42	mA
I_{CDD4R}	$I_{CDD4R} = 2 \times I_{DD4R}$	x16	180	mA
I_{CDD4W}	$I_{CDD4W} = 2 \times I_{DD4W}$	x16	180	mA
I_{CDD5B}	$I_{CDD5B} = 2 \times I_{DD5B}$	x16	304	mA
I_{CDD6}	$I_{CDD6} = 2 \times I_{DD6}$	x16	30	mA
I_{CDD6ET}	$I_{CDD6ET} = 2 \times I_{DD6ET}$	x16	46	mA
I_{CDD7}	$I_{CDD7} = 2 \times I_{DD7}$	x16	292	mA
I_{CDD8}	$I_{CDD8} = 2 \times I_{DD8}$	x16	26	mA

Notes:
1. I_{CDD} values reflect the combined current of both individual die. I_{DDx} represents individual die values.
2. The I_{DD} values must be derated (increased) on IT-option devices when operated outside of the range $0°C \le T_C \le 85°C$:

   2a. When $T_C < 0°C$: I_{DD2P0}, I_{DD2P1} and I_{DD3P} must be derated by 4%; I_{DD4R} and I_{DD4W} must be derated by 2%; and I_{DD6}, I_{DD6ET} and I_{DD7} must be derated by 7%.

   2b. When $T_C > 85°C$: I_{DD4R}, I_{DD4W}, I_{DD5B}, and I_{DD7} must be derated by 5%; I_{DD0}, I_{DD1}, I_{DD2P1}, I_{DD3N}, and I_{DD3P} must be derated by 15%; I_{DD2P0}, I_{DD2Q}, I_{DD2N}, and I_{DD2NT} must be derated by 40%.

   2c. When $T_C > 95°C$: all IDD values must be derated (increased) by 30% from the 85°C specifications.

   2d. When $T_C > 105°C$: all IDDx values must be derated (increased) by 50% from the 85°C specifications.

Revision History

Rev. C – 04/19

- 04/10/2019 Updated DDR3L Input/Output Capacitance table: C_{CK}, C_I, and C_{DI_CTRL}

Rev. B – 02/19

- 01/08/2019 Updated legal status to Production
- 01/08/2019 Updated DDR3L Input/Output Capacitance table in Input/Output Capacitance section

Rev. A – 08/18

- 07/26/2018 Updated thermal characteristics section
- 07/01/2018 Changed Die 0 to Die 1 in Functional Block Diagram
- 04/01/2018 Initial release for DDR3L_8Gb_x16_1_35V_Single_rank_TwinDie

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