ALTERA

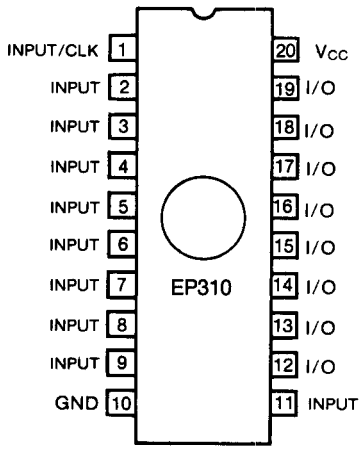
8 MACROCELL EPLD

EP310

FEATURES

- Programmable replacement for conventional fixed logic.
- EPROM technology allows reprogrammability, ensures high programming yield and ease of use.
- Second generation programmable logic architecture allows up to 18 inputs and 8 outputs.
- Each output is *User Programmable* for combinatorial or registered operation, in active high or low mode.
- Each output also has an independently *User Programmable* feedback path.
- 100% generically testable—provides 100% programming yield.
- Programmable "Security Bit" allows total protection of proprietary designs.
- Advanced software support featuring Schematic Capture, Interactive Netlist, Boolean Equation and State Machine design entry.
- Advanced CHMOS II-E circuitry for systems requiring low power, high performance speeds, and immunity to noise.

CONNECTION DIAGRAM

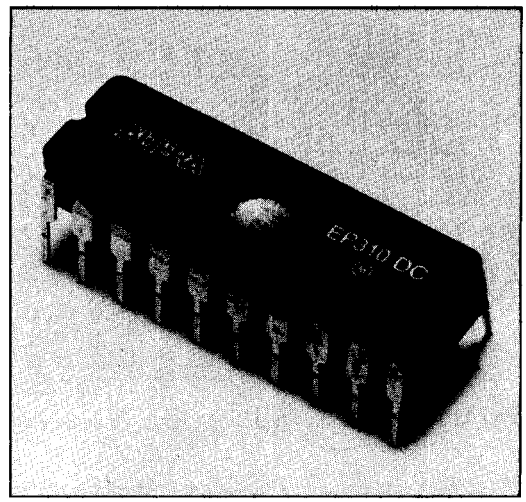


GENERAL DIAGRAM

The ALTERA EP310 combines the power, flexibility, and density advantages of CMOS, EPROM technology with second generation programmable logic array architecture. This combination defines a new capability in electrically programmable logic. The EP310 utilizes the familiar sum-of-products architecture which allows users to program complex custom logic functions quickly and easily. Up to 18 inputs and 8 outputs are provided, with eight product terms and a separate Output Enable term for each output.

A unique feature of the EP310 is the ability to program each output architecture on an individual basis. This gives the user the flexibility to assign either combinatorial or registered output, in either active high or active low mode, to each output pin. In addition, the feedback path can be programmed independently of the output to be either combinatorial, registered, or I/O. Other advantages include: 100% generic testing (all devices are 100% tested at the factory). The device can be erased with ultraviolet light. Design changes are no longer costly, nor is there a need for post programming testing.

Programming the EP310 is accomplished with the use of Altera's A+PLUS development software which supports four different design entry methods. Once the circuit has been entered, the A+PLUS software performs automatic translation into logical equations, boolean minimization, and design fitting directly into an EP310.



REV. 6.0

FUNCTIONAL DESCRIPTION

A block diagram of the EP310, along with logic diagrams of the I/O Architecture Control function and the Logic Array Macrocell are shown in figures 2 and 3. The EP310 is organized in the familiar sum-of-products format with a total of 74 product terms and 36 input lines.

At each intersecting point in the logic array, there exists an EPROM type programmable connection. Initally, all connections are made. This means that both the true and complement of all inputs are connected to each product term. Connections are opened during the programming process. Therefore any product term can be connected to the true or complement of any input. When both the true and complement connection of any input are left intact, a logical false results on the output of the AND gate. If both the true and complement connections of any input are programmed open, then a logical "don't care" results for that input. If all inputs for a product term are programmed open, then a logical true results on the output of the AND gate.

A dramatic improvement in the flexibility of programmable logic is achieved in the ALTERA EP310 through programmable I/O architecture. Each output can be combinatorial (i.e. direct output of the OR gate) or registered (i.e. output through a D type flip-flop). Both types of output can also be inverted. Independent of the output mode, the feedback can be programmed to be combinatorial, registered, I/O (i.e directly from the pin), or none. These features enable the user to optimize the device for precise application requirements.

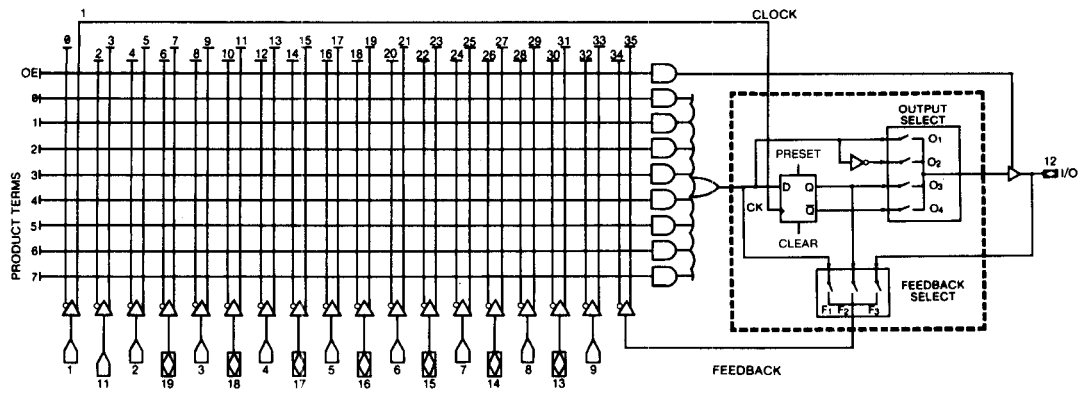
To improve functionality, the ALTERA EP310 has additional Synchronous Preset and Asynchronous Clear product terms. These terms are connected to all D-type Flip-Flops. When the Synchronous Preset product term is asserted (HIGH), the output register will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Clear product term is asserted (HIGH), the output register will immediately be loaded with a LOW (independent of the clock). An Asynchronous Clear overrides a Synchronous Preset requirement. On power-up, the EP310 performs the Clear function automatically.

The EP310 is manufactured using a CMOS EPROM process. This advanced process, along with built in test features, allows 100% pre-test of each programmable connection at the factory.

DESIGN SECURITY

The EP310 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset simply by erasing the device.

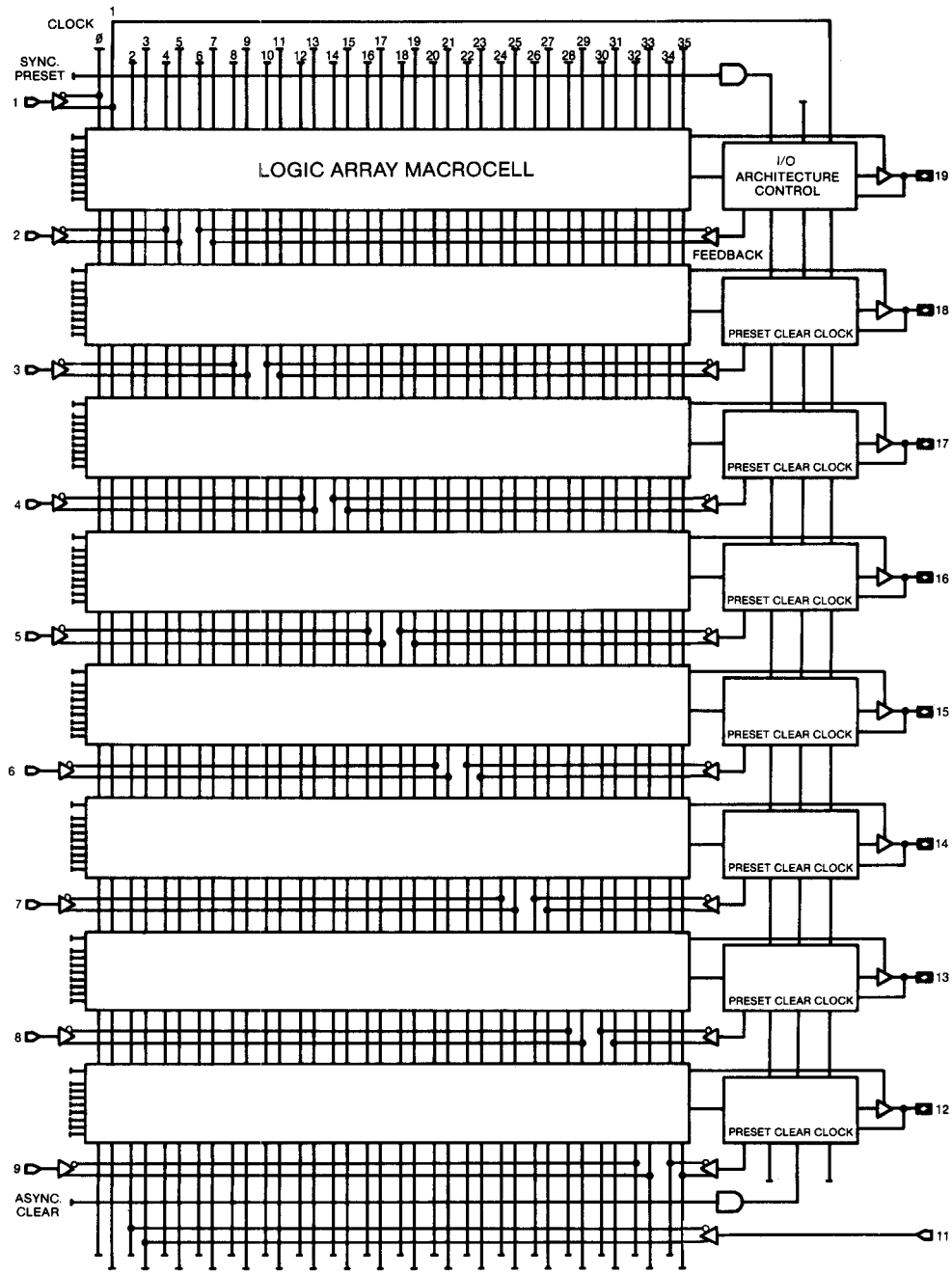
Figure 2. EP310 Macrocell



Note: ▯ I/O Pin in which Logic Array input is from feedback path

This diagram shows one of the eight Macrocells within the EP310.

Figure 3. EP310 Block Diagram



ABSOLUTE MAXIMUM RATINGS

Note: See Design Recommendations

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage	With respect to GND note (3)	-2.0	7.0	V
V_{PP}	Programming supply voltage		-2.0	13.5	V
V_I	DC INPUT voltage		-2.0	7.0	V
I_{MAX}	DC V_{CC} or GND current		-80	+80	mA
I_{OUT}	DC OUTPUT current, per pin		-25	+25	mA
P_D	Power dissipation			320	mW
T_{STG}	Storage temperature	No bias	-65	+150	°C
T_{AMB}	Ambient temperature	Under bias	-65	+135	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply Voltage	note (5)	4.75 (4.5)	5.25 (5.5)	V
V_I	INPUT voltage		0	V_{CC}	V
V_O	OUTPUT voltage		0	V_{CC}	V
T_A	Operating temperature	For Commercial	0	70	°C
T_A	Operating temperature	For Industrial	-40	85	°C
T_C	Case temperature	For Military	-55	125	°C
T_R	INPUT rise time			500	ns
T_F	INPUT fall time			500	ns

DC OPERATING CHARACTERISTICS

(V_{CC} = 5V ±5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ±10%, T_C = -55°C to 125°C for Military)*
Note (1) and (5)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	HIGH level input voltage		2.0		V_{CC} + 0.3	V
V_{IL}	LOW level input voltage		-0.3		0.8	V
V_{OH}	HIGH level TTL output voltage	I_{OH} = -4mA DC	2.4			V
V_{OH}	HIGH level CMOS output voltage	I_{OH} = -2mA DC	3.84			V
V_{OL}	LOW level output voltage	I_{OL} = 4mA DC			0.45	V
I_I	Input leakage current	V_I = V_{CC} or GND	-10		+10	μA
I_{OZ}	3-state output off-state current	V_O = V_{CC} or GND	-10		+10	μA
I_{CC1}	V_{CC} supply current (standby)	V_I = V_{CC} or GND No load		15	30 (35)	mA
I_{CC3}	V_{CC} supply current (active)	V_I = V_{CC} or GND No load, f = 1.0 MHz note (6)		16	40	mA

CAPACITANCE

Note (4)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V f = 1.0 MHz		12	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V f = 1.0 MHz		12	pF
C_{CLK}	Clock Pin Capacitance	V_{IN} = 0V f = 1.0 MHz		12	pF

AC CHARACTERISTICS

(V_{CC} = 5V ± 5%, T_A = 0°C to 70°C for Commercial)
(V_{CC} = 5V ± 10%, T_A = -40°C to 85°C for Industrial)
(V_{CC} = 5V ± 10%, T_C = -55°C to 125°C for Military)*

			EP310-2		EP310-3		EP310		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t_{PD1}	Input to non-registered output	C_1 = 30pF		35		40		50	ns
t_{PD2}	I/O input to non-registered output			37		42		52	ns
t_{PZX}	Input to output enable			35		40		50	ns
t_{PXZ}	Input to output disable	C_1 = 5pF note (2)		35		40		50	ns
t_{CLR}	Asynchronous output clear time	C_1 = 30pF		45		50		55	ns
t_{IO}	I/O input buffer delay			2		2		2	ns

SYNCHRONOUS CLOCK MODE

			EP310-2		EP310-3		EP310		
SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
f_{MAX}	Maximum frequency	note (7)	35.7		33.3		31.3		MHz
t_{SU}	Input setup time		28		30		32		ns
t_H	Input hold time		0		0		0		ns
t_{CH}	Clock high time		14		15		16		ns
t_{CL}	Clock low time		14		15		16		ns
t_{CO1}	Clock to output delay			22		24		28	ns
t_{CNT}	Minimum clock period (register output feedback to register input - internal path)	note (6)		33		37		42	ns
f_{CNT}	Internal maximum frequency ($1/t_{CNT}$)	note (6)	30.3		27.0		23.8		MHz
t_{SET}	Synchronous preset input or I/O input set-up time		28		31		35		ns

Notes:
1. Typical values are for T_A = 25°C, V_{CC} = 5V
2. Sample tested only for an output change of 500mV.
3. Minimum DC input is -0.3V. During transitions, the inputs may undershoot to -2.0V for periods less than 20ns.
4. Capacitance measured at 25°C. Sample tested only. Pin 11, (used for programming), has capacitance of 50 pf max.
5. Figures in ( ) pertain to military and industrial temperature version.
6. Measured with device programmed as 8-Bit Counter.
7. The f_{MAX} values shown represent the highest frequency for pipelined data.

GRADE	AVAILABILITY
Commercial (0°C to 70°C)	EP310-2 EP310-3 EP310
Industrial (-40°C to 85°C)	EP310
Military (-55°C to 125°C)	EP310

*** The specifications noted above apply to military operating range devices. MIL-STD-883 compliant product specifications are provided in military product drawings available on request from Altera marketing at 408/984-2805, ext. 101. These military product drawings should be used for the preparation of source control drawings.**

Figure 4. Output Drive Currents

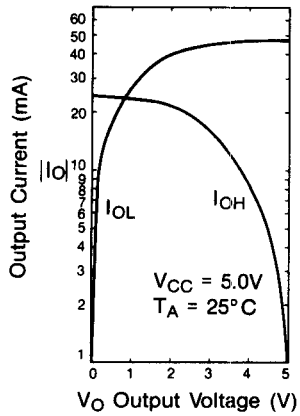
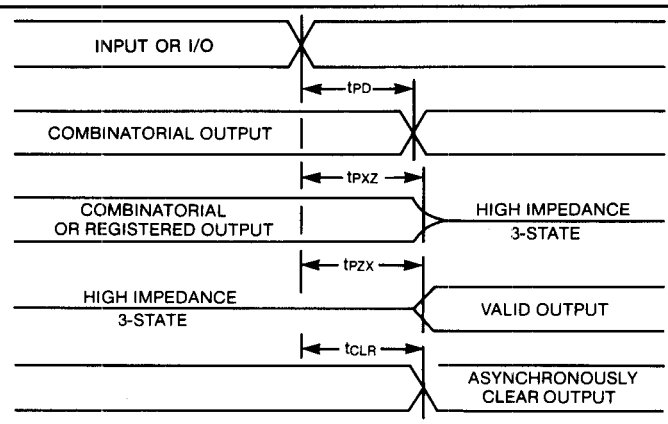
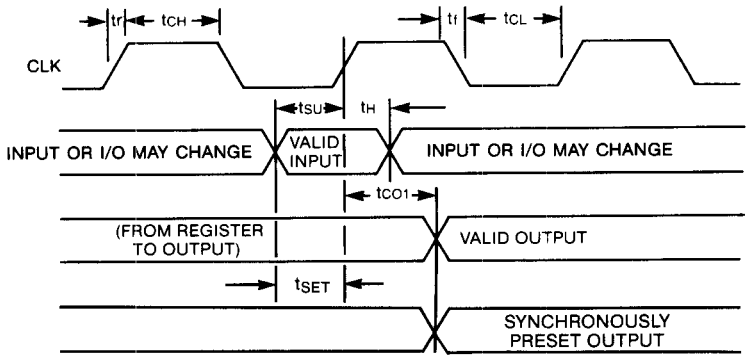


Figure 5. Switching Waveforms

COMBINATORIAL MODE

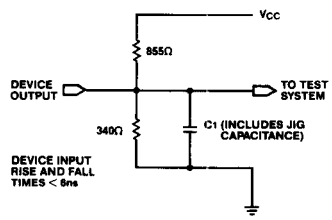


SYNCHRONOUS CLOCK MODE



Notes: t_r & t_f < 6ns; t_{CL} & t_{CH} measured at 0.3V and 2.7V; all other timings at 1.5V; Input voltage levels at 0V and 3V

Figure 6. AC Test Conditions



Power supply transients can affect AC measurements, simultaneous transitions of multiple outputs should be avoided for accurate measurement. Do not attempt to perform threshold tests under AC conditions. Large amplitude, fast ground current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground pin and the test system ground can create significant reductions in observable input noise immunity.

Figure 7. I_{CC} vs. F_{MAX}