

MJW3281A (NPN) MJW1302A (PNP)

Complementary NPN-PNP Silicon Power Bipolar Transistors

The MJW3281A and MJW1302A are PowerBase™ power transistors for high power audio, disk head positioners and other linear applications.

Features

- Designed for 100 W Audio Frequency
- Gain Complementary:
Gain Linearity from 100 mA to 7 A
 $h_{FE} = 45$ (Min) @ $I_C = 8$ A
- Low Harmonic Distortion
- High Safe Operation Area – 1 A/100 V @ 1 Second
- High f_T – 30 MHz Typical
- Pb-Free Packages are Available*

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|----------------|-------------|--------------------------|
| Collector-Emitter Voltage | V_{CEO} | 230 | Vdc |
| Collector-Base Voltage | V_{CBO} | 230 | Vdc |
| Emitter-Base Voltage | V_{EBO} | 5.0 | Vdc |
| Collector-Emitter Voltage – 1.5 V | V_{CEX} | 230 | Vdc |
| Collector Current – Continuous – Peak (Note 1) | I_C | 15 25 | Adc |
| Base Current – Continuous | I_B | 1.5 | Adc |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above 25°C | P_D | 200 1.43 | W W/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -65 to +150 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------------|-------|---------------------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 0.625 | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 40 | $^\circ\text{C}/\text{W}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle < 10%.

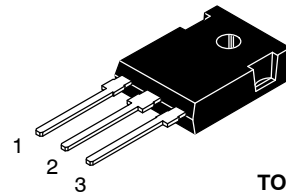
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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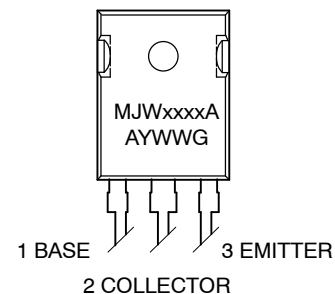
<http://onsemi.com>

**15 AMPERES
COMPLEMENTARY
SILICON POWER TRANSISTORS
230 VOLTS 200 WATTS**



TO-247
CASE 340L

MARKING DIAGRAM



xxxx = 3281 or 1302
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

| Device | Package | Shipping |
|-----------|---------------------|---------------|
| MJW3281A | TO-247 | 30 Units/Rail |
| MJW3281AG | TO-247 (Pb-Free) | 30 Units/Rail |
| MJW1302A | TO-247 | 30 Units/Rail |
| MJW1302AG | TO-247 (Pb-Free) | 30 Units/Rail |

MJW3281A (NPN) MJW1302A (PNP)

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|--|-----------------------|--|--------------------------------------|---|------------------|
| OFF CHARACTERISTICS | | | | | |
| Collector-Emitter Sustaining Voltage (I _C = 100 mA _{dc} , I _B = 0) | V _{CEO(sus)} | 230 | – | – | V _{dc} |
| Collector Cutoff Current (V _{CB} = 230 V _{dc} , I _E = 0) | I _{CBO} | – | – | 50 | μA _{dc} |
| Emitter Cutoff Current (V _{EB} = 5 V _{dc} , I _C = 0) | I _{EBO} | – | – | 5 | μA _{dc} |
| SECOND BREAKDOWN | | | | | |
| Second Breakdown Collector with Base Forward Biased (V _{CE} = 50 V _{dc} , t = 1 s (non-repetitive) (V _{CE} = 100 V _{dc} , t = 1 s (non-repetitive) | I _{S/b} | 4 1 | – – | – – | A _{dc} |
| ON CHARACTERISTICS | | | | | |
| DC Current Gain (I _C = 100 mA _{dc} , V _{CE} = 5 V _{dc}) (I _C = 1 A _{dc} , V _{CE} = 5 V _{dc}) (I _C = 3 A _{dc} , V _{CE} = 5 V _{dc}) (I _C = 5 A _{dc} , V _{CE} = 5 V _{dc}) (I _C = 7 A _{dc} , V _{CE} = 5 V _{dc}) (I _C = 8 A _{dc} , V _{CE} = 5 V _{dc}) (I _C = 15 A _{dc} , V _{CE} = 5 V _{dc}) | h _{FE} | 50 50 50 50 50 45 12 | 125 – – – 115 – 35 | 200 200 200 200 200 – – | – |
| Collector-Emitter Saturation Voltage (I _C = 10 A _{dc} , I _B = 1 A _{dc}) | V _{CE(sat)} | – | 0.4 | 2 | V _{dc} |
| Base-Emitter On Voltage (I _C = 8 A _{dc} , V _{CE} = 5 V _{dc}) | V _{BE(on)} | – | – | 2 | V _{dc} |
| DYNAMIC CHARACTERISTICS | | | | | |
| Current-Gain – Bandwidth Product (I _C = 1 A _{dc} , V _{CE} = 5 V _{dc} , f _{test} = 1 MHz) | f _T | – | 30 | – | MHz |
| Output Capacitance (V _{CB} = 10 V _{dc} , I _E = 0, f _{test} = 1 MHz) | C _{ob} | – | – | 600 | pF |

MJW3281A (NPN) MJW1302A (PNP)

TYPICAL CHARACTERISTICS

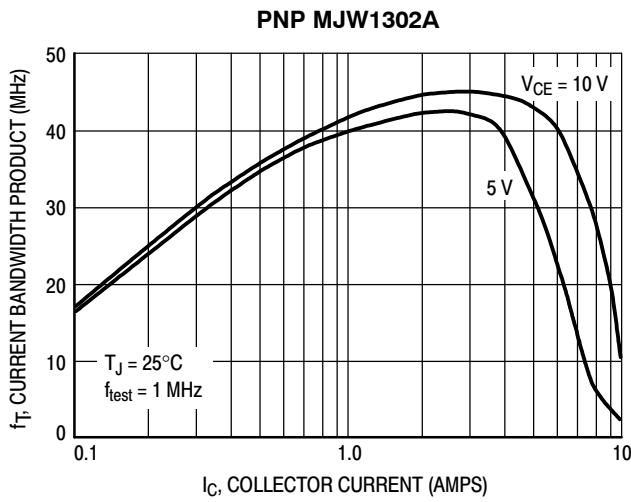


Figure 1. Typical Current Gain Bandwidth Product

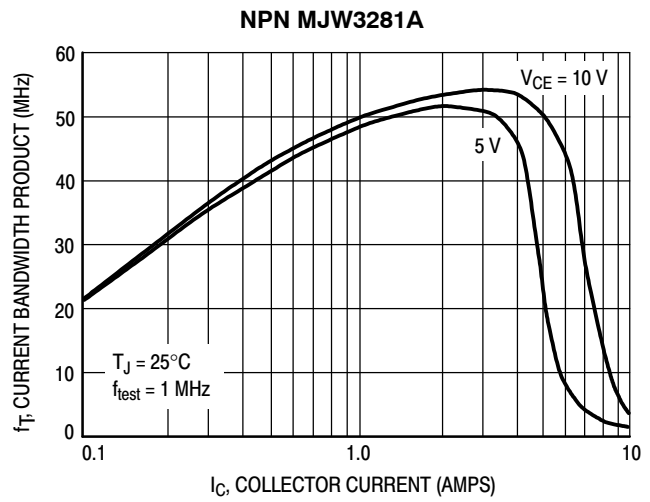


Figure 2. Typical Current Gain Bandwidth Product

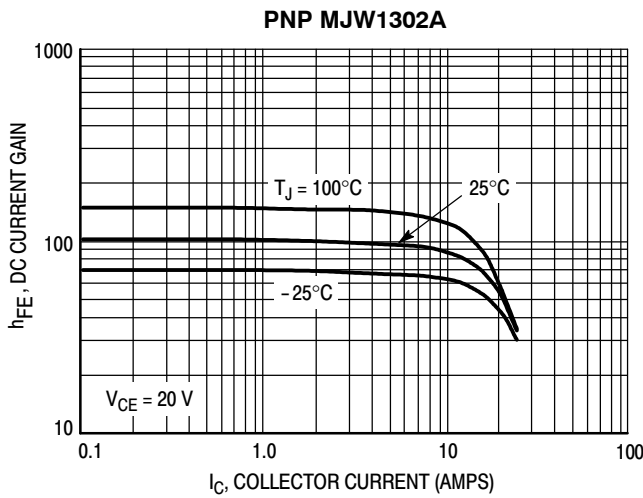


Figure 3. DC Current Gain, $V_{CE} = 20 \text{ V}$

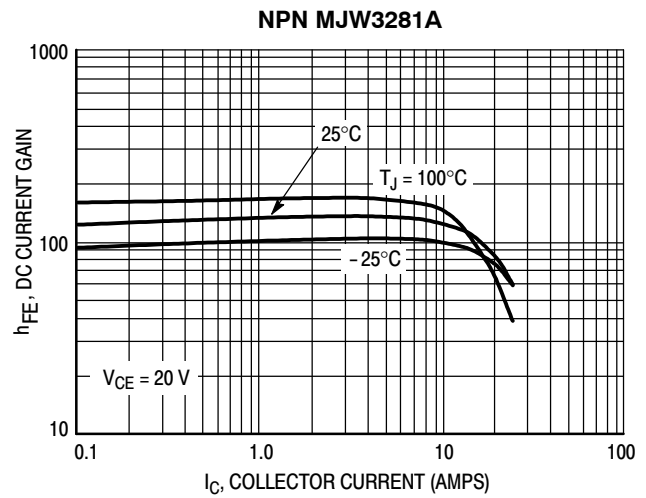


Figure 4. DC Current Gain, $V_{CE} = 20 \text{ V}$

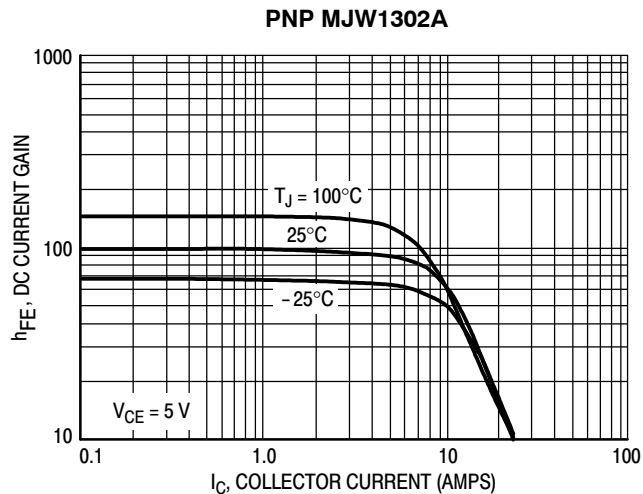


Figure 5. DC Current Gain, $V_{CE} = 5 \text{ V}$

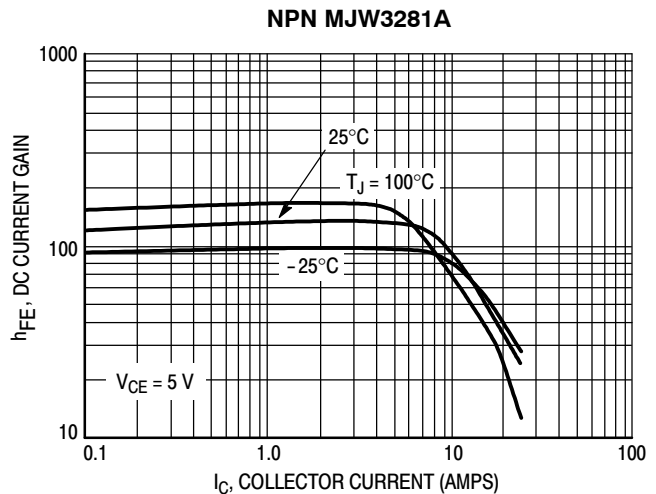


Figure 6. DC Current Gain, $V_{CE} = 5 \text{ V}$

MJW3281A (NPN) MJW1302A (PNP)

TYPICAL CHARACTERISTICS

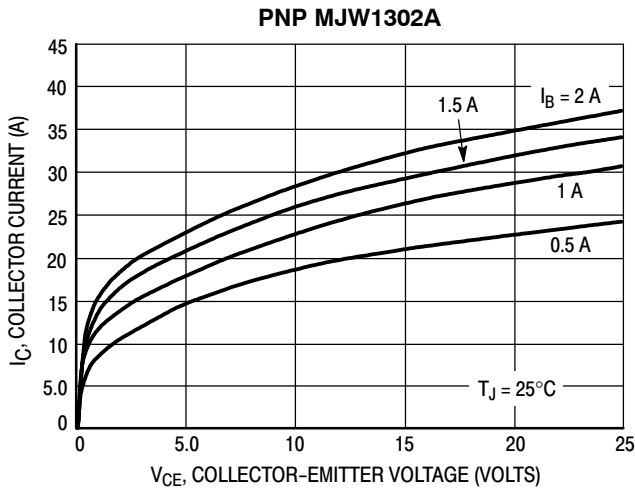


Figure 7. Typical Output Characteristics

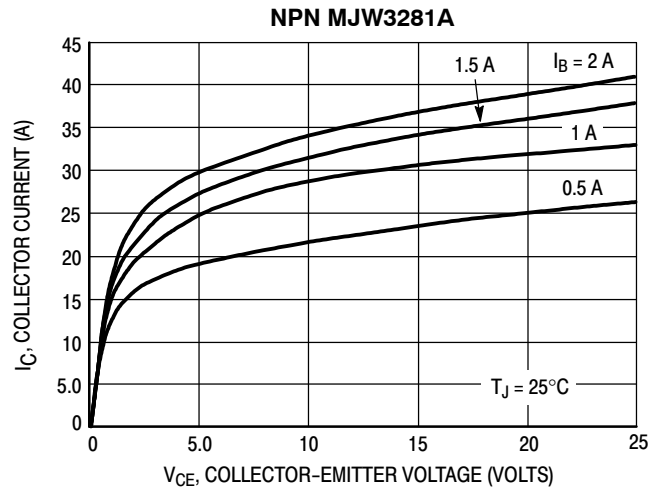


Figure 8. Typical Output Characteristics

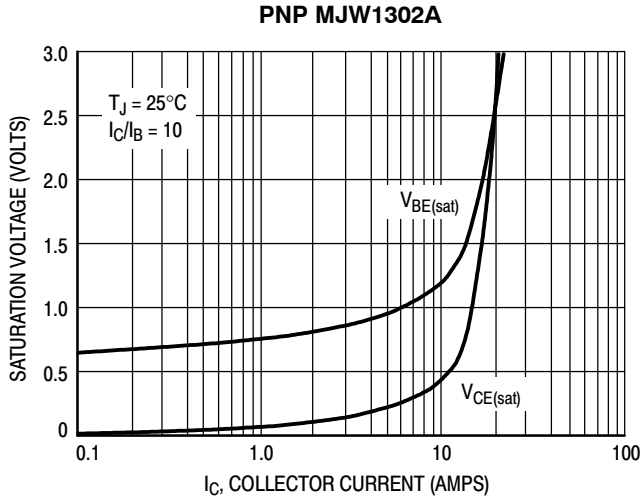


Figure 9. Typical Saturation Voltages

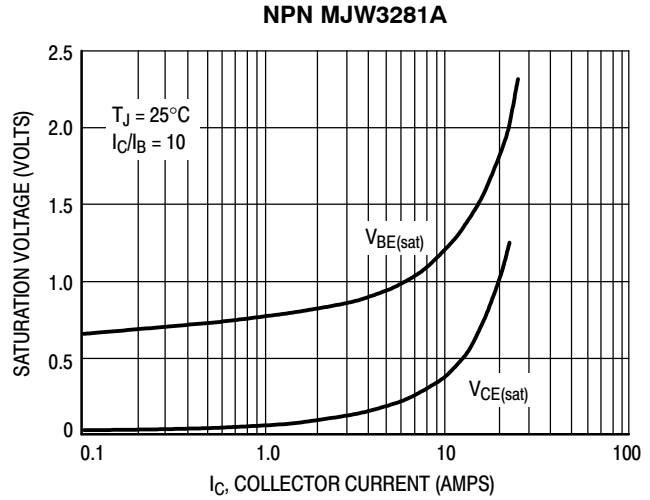


Figure 10. Typical Saturation Voltages

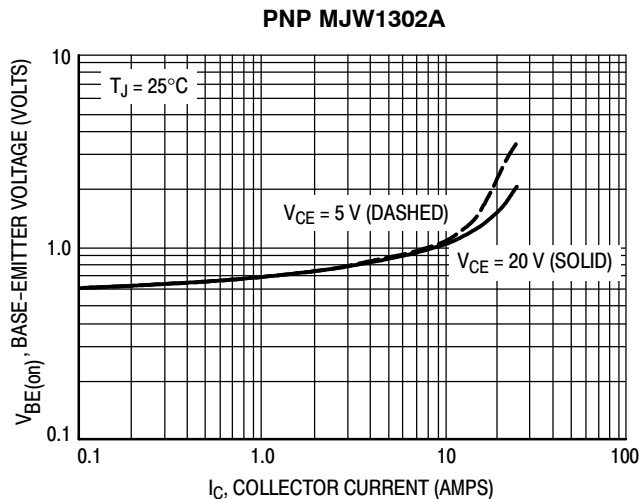


Figure 11. Typical Base-Emitter Voltage

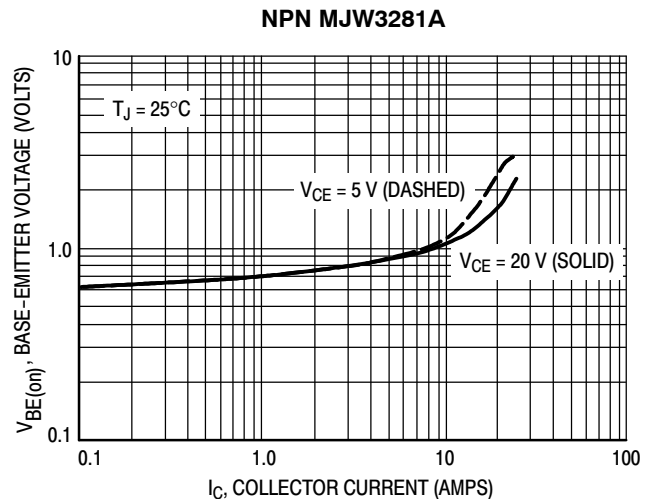


Figure 12. Typical Base-Emitter Voltage

MJW3281A (NPN) MJW1302A (PNP)

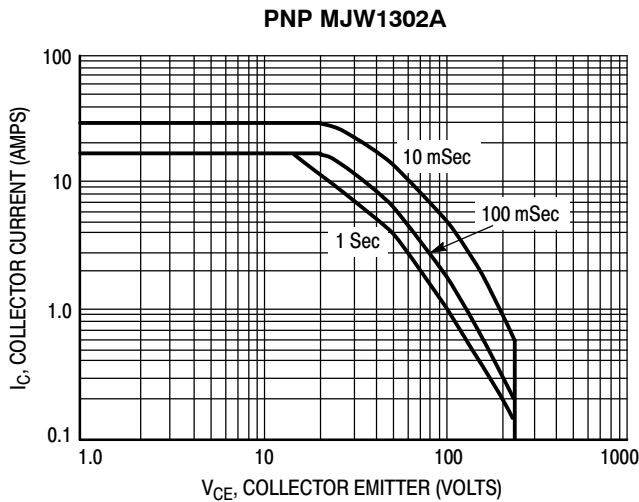


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

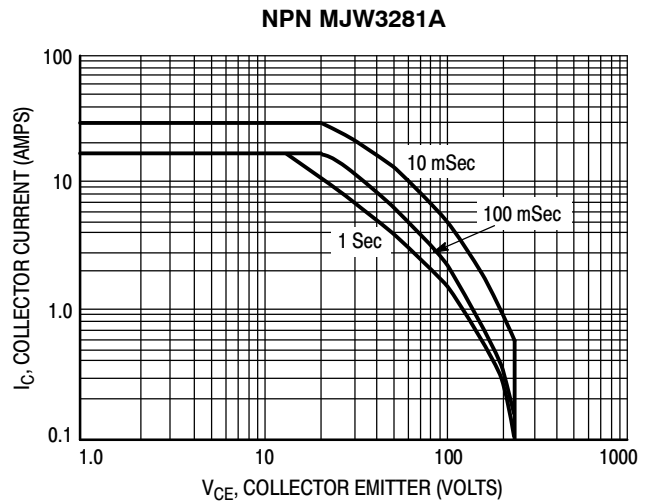


Figure 14. Active Region Safe Operating Area

The data of Figures 13 and 14 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

TYPICAL CHARACTERISTICS

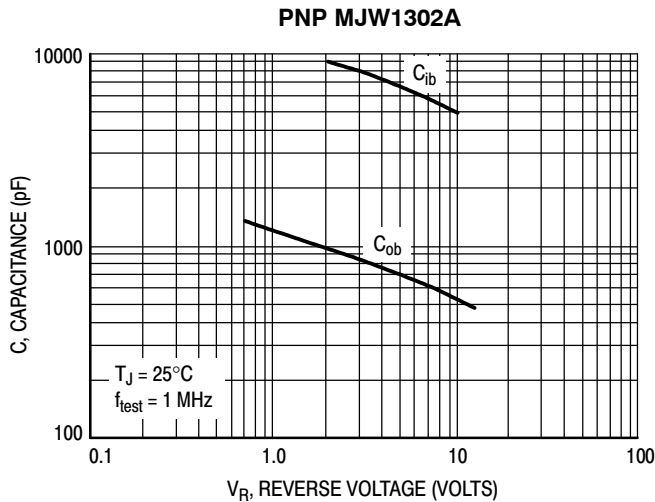


Figure 15. MJW1302A Typical Capacitance

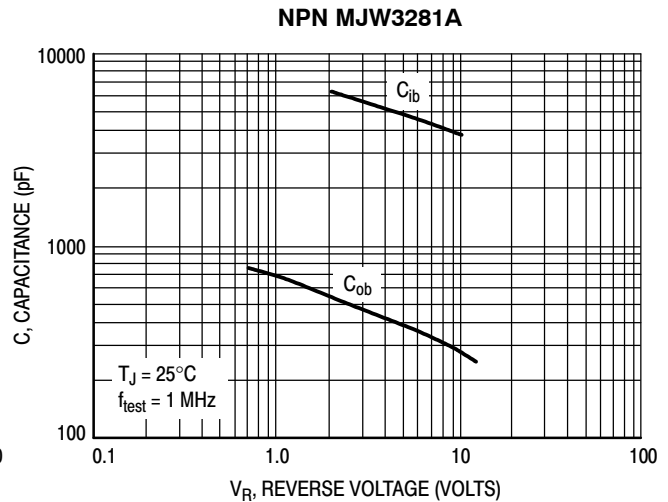
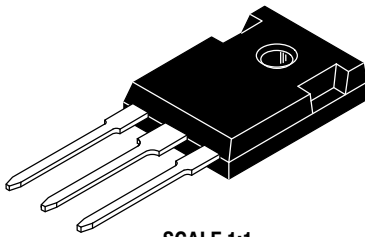


Figure 16. MJW3281A Typical Capacitance

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

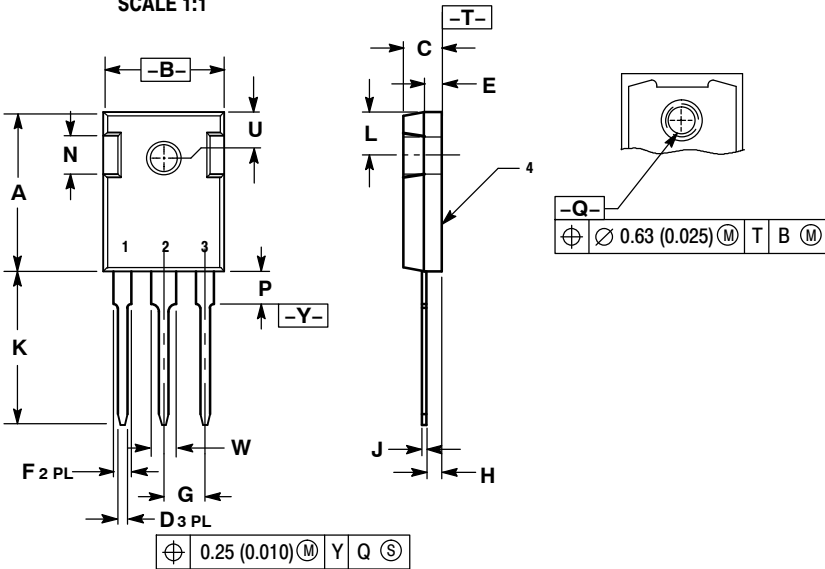
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TO-247
CASE 340L-02
ISSUE F

DATE 26 OCT 2011

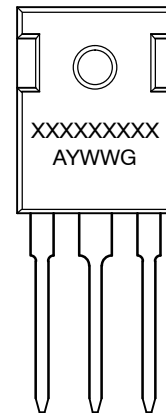
SCALE 1:1



- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: MILLIMETER.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 20.32 | 21.08 | 0.800 | 0.830 |
| B | 15.75 | 16.26 | 0.620 | 0.640 |
| C | 4.70 | 5.30 | 0.185 | 0.209 |
| D | 1.00 | 1.40 | 0.040 | 0.055 |
| E | 1.90 | 2.60 | 0.075 | 0.102 |
| F | 1.65 | 2.13 | 0.065 | 0.084 |
| G | 5.45 BSC | | 0.215 BSC | |
| H | 1.50 | 2.49 | 0.059 | 0.098 |
| J | 0.40 | 0.80 | 0.016 | 0.031 |
| K | 19.81 | 20.83 | 0.780 | 0.820 |
| L | 5.40 | 6.20 | 0.212 | 0.244 |
| N | 4.32 | 5.49 | 0.170 | 0.216 |
| P | --- | 4.50 | --- | 0.177 |
| Q | 3.55 | 3.65 | 0.140 | 0.144 |
| U | 6.15 BSC | | 0.242 BSC | |
| W | 2.87 | 3.12 | 0.113 | 0.123 |

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 G = Pb-Free Package

- STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN
- STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)
- STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR
- STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE
- STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

| | | |
|------------------|---------------------------|--|
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