

# NTD2955, NVD2955

## MOSFET – Power, P-Channel, DPAK

**-60 V, -12 A**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low-voltage, high-speed switching applications in power supplies, converters, and power motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer an additional safety margin against unexpected voltage transients.

### Features

- Avalanche Energy Specified
- $I_{DSS}$  and  $V_{DS(on)}$  Specified at Elevated Temperature
- Designed for Low-Voltage, High-Speed Switching Applications and to Withstand High Energy in the Avalanche and Commutation Modes
- NVD and SVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	-60	Vdc
Gate-to-Source Voltage	$V_{GS}$ $V_{GSM}$	$\pm 20$ $\pm 25$	Vdc Vpk
Drain Current	$I_D$ $I_{DM}$	-12 -18	Adc Apk
Total Power Dissipation @ $T_a = 25^\circ\text{C}$	$P_D$	55	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 25\text{ Vdc}$ , $V_{GS} = 10\text{ Vdc}$ , Peak $I_L = 12\text{ Apk}$ , $L = 3.0\text{ mH}$ , $R_G = 25\ \Omega$ )	$E_{AS}$	216	mJ
Thermal Resistance	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	2.73 71.4 100	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8 in. from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

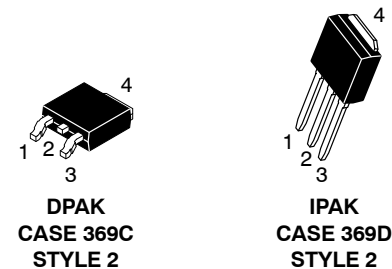
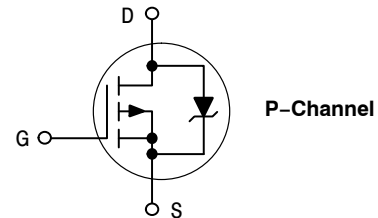
1. When surface mounted to an FR4 board using 1 in pad size (Cu area = 1.127 in<sup>2</sup>).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu area = 0.412 in<sup>2</sup>).



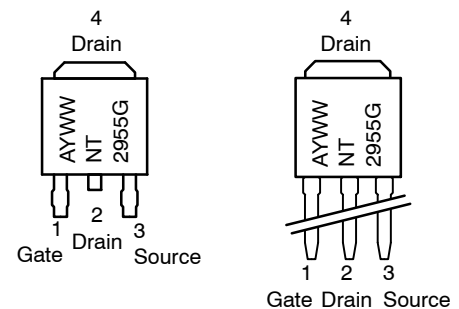
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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-60 V	155 m $\Omega$ @ -10 V, 6 A	-12 A



### MARKING DIAGRAMS & PIN ASSIGNMENTS



A = Assembly Location\*  
 NT2955/NV2955 = Specific Device Code (DPAK)  
 NT2955 = Specific Device Code (IPAK)  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

# NTD2955, NVD2955

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = -0.25 mA) (Positive Temperature Coefficient)	V <sub>(BR)DSS</sub>	-60 -	- 67	- -	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = -60 Vdc, T <sub>J</sub> = 25°C) (V <sub>GS</sub> = 0 Vdc, V <sub>DS</sub> = -60 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	- -	- -	-10 -100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ± 20 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	-	-	-100	nAdc

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μAdc) (Negative Temperature Coefficient)	V <sub>GS(th)</sub>	-2.0 -	-2.8 4.5	-4.0 -	Vdc mV/°C
Static Drain-Source On-State Resistance (V <sub>GS</sub> = -10 Vdc, I <sub>D</sub> = -6.0 Adc)	R <sub>DS(on)</sub>	-	0.155	0.180	Ω
Drain-to-Source On-Voltage (V <sub>GS</sub> = -10 Vdc, I <sub>D</sub> = -12 Adc) (V <sub>GS</sub> = -10 Vdc, I <sub>D</sub> = -6.0 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	-	-1.86 -	-2.6 -2.0	Vdc
Forward Transconductance (V <sub>DS</sub> = 10 Vdc, I <sub>D</sub> = 6.0 Adc)	g <sub>FS</sub>	-	8.0	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = -25 Vdc, V <sub>GS</sub> = 0 Vdc, F = 1.0 MHz)	C <sub>iSS</sub>	-	500	750	pF
Output Capacitance		C <sub>oSS</sub>	-	150	250	
Reverse Transfer Capacitance		C <sub>rSS</sub>	-	50	100	

### SWITCHING CHARACTERISTICS (Notes 3 and 4)

Turn-On Delay Time	(V <sub>DD</sub> = -30 Vdc, I <sub>D</sub> = -12 A, V <sub>GS</sub> = -10 V, R <sub>G</sub> = 9.1 Ω)	t <sub>d(on)</sub>	-	10	20	ns
Rise Time		t <sub>r</sub>	-	45	85	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	26	40	
Fall Time		t <sub>f</sub>	-	48	90	
Gate Charge	(V <sub>DS</sub> = -48 Vdc, V <sub>GS</sub> = -10 Vdc, I <sub>D</sub> = -12 A)	Q <sub>T</sub>	-	15	30	nC
		Q <sub>GS</sub>	-	4.0	-	
		Q <sub>GD</sub>	-	7.0	-	

### DRAIN-SOURCE DIODE CHARACTERISTICS (Note 3)

Diode Forward On-Voltage (I <sub>S</sub> = 12 Adc, V <sub>GS</sub> = 0 V) (I <sub>S</sub> = 12 Adc, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	- -	-1.6 -1.3	-2.5 -	Vdc
Reverse Recovery Time (I <sub>S</sub> = 12 A, di <sub>S</sub> /dt = 100 A/μs, V <sub>GS</sub> = 0 V)	t <sub>rr</sub>	-	50	-	ns
	t <sub>a</sub>	-	40	-	
	t <sub>b</sub>	-	10	-	
Reverse Recovery Stored Charge	Q <sub>RR</sub>	-	0.10	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperature.

# NTD2955, NVD2955

## TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

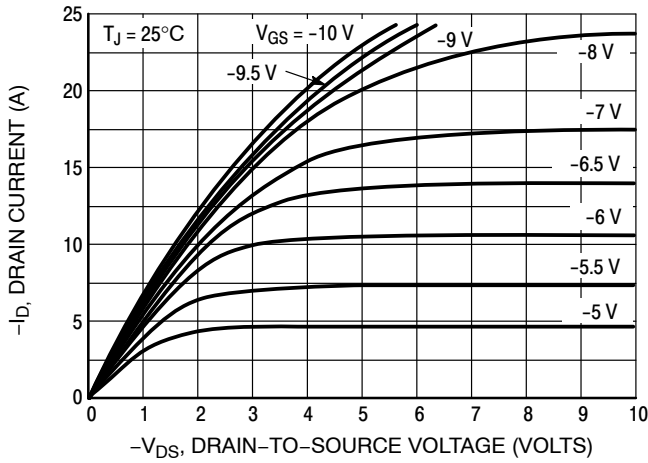


Figure 1. On-Region Characteristics

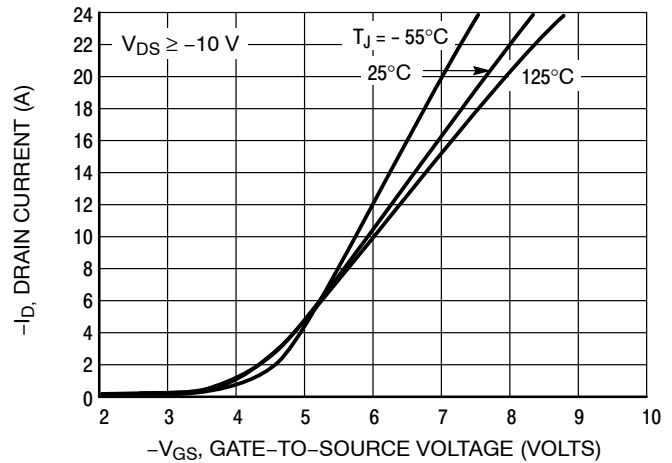


Figure 2. Transfer Characteristics

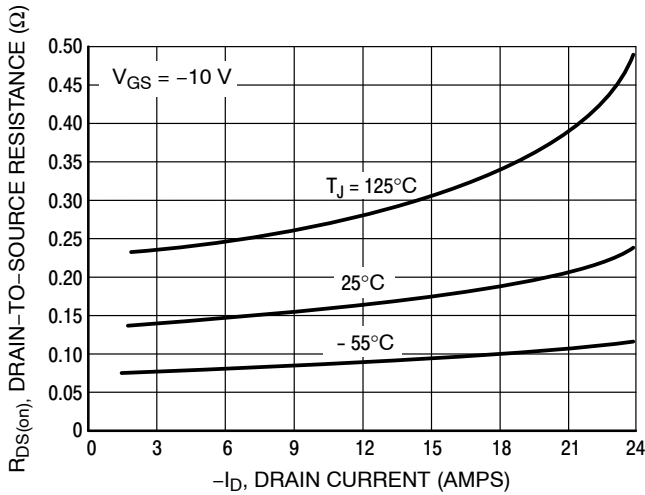


Figure 3. On-Resistance versus Drain Current and Temperature

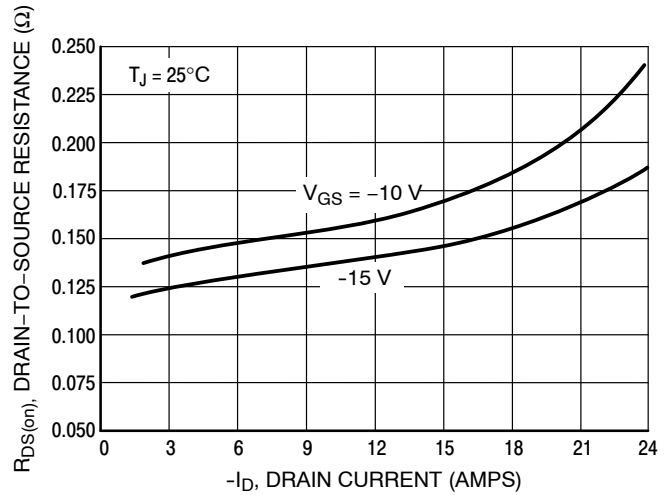


Figure 4. On-Resistance versus Drain Current and Gate Voltage

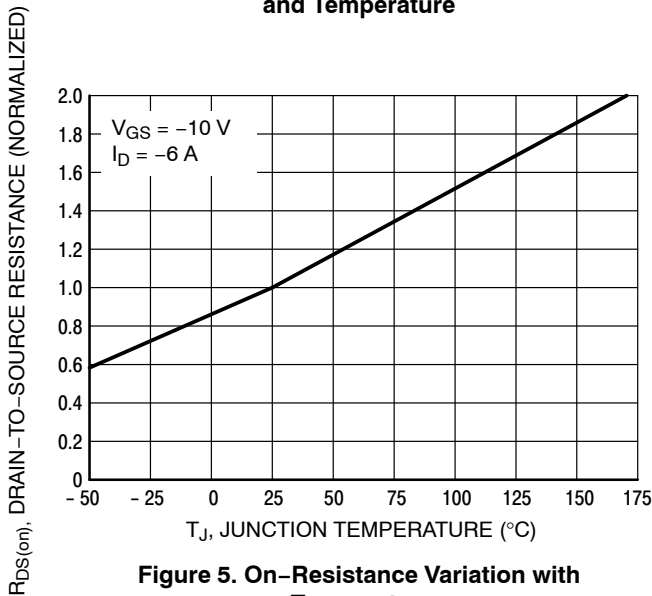


Figure 5. On-Resistance Variation with Temperature

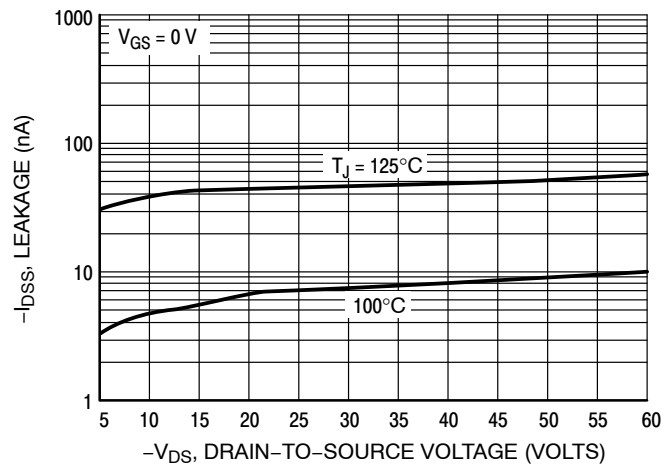
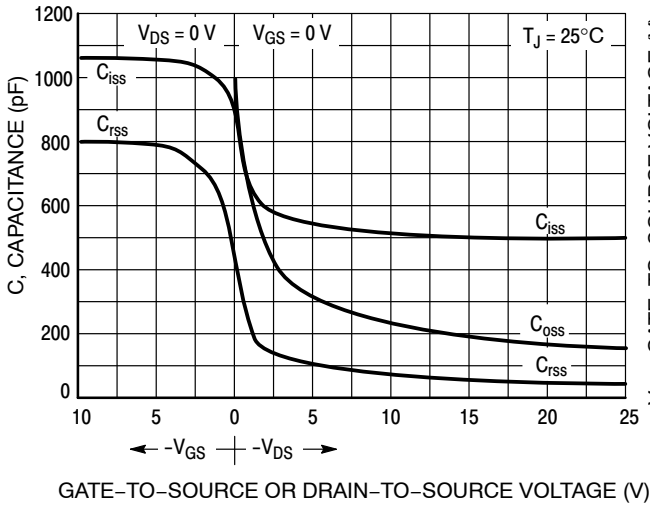
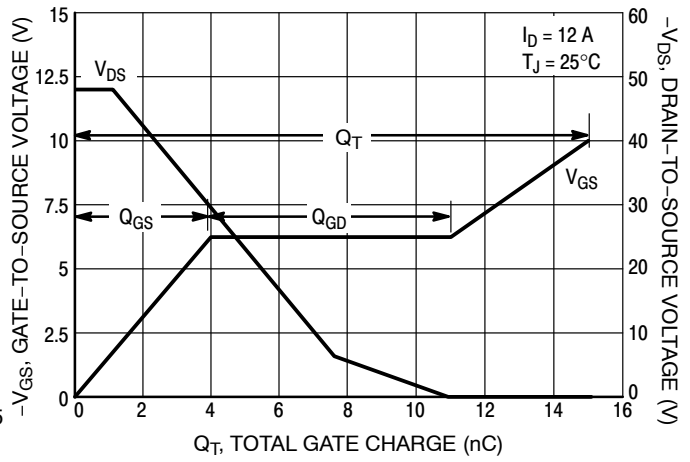


Figure 6. Drain-To-Source Leakage Current versus Voltage

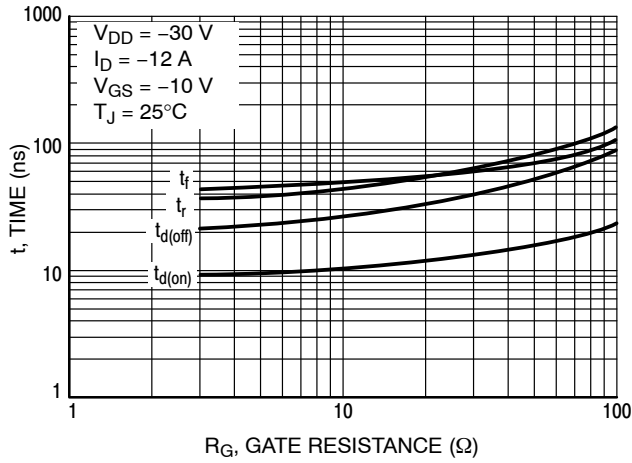
# NTD2955, NVD2955



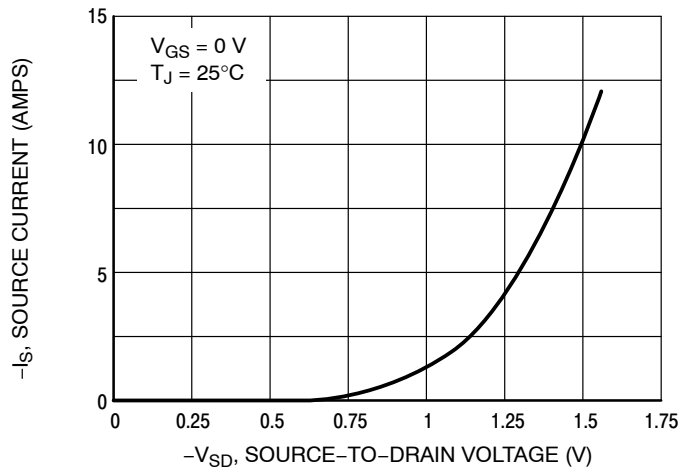
**Figure 7. Capacitance Variation**



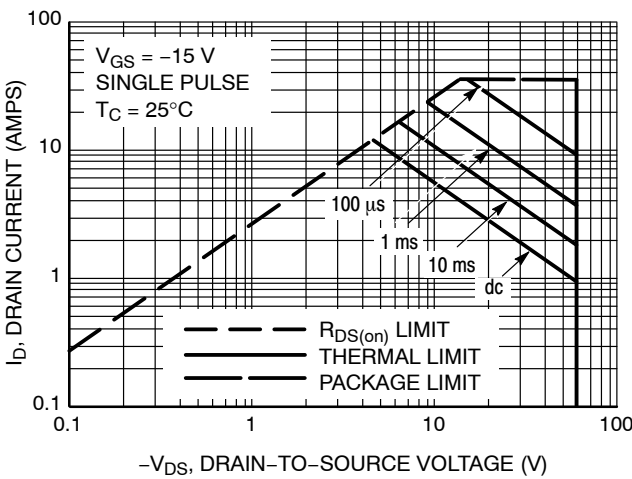
**Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge**



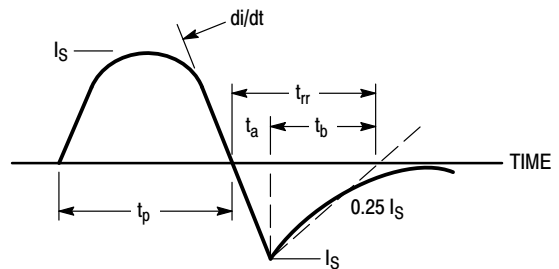
**Figure 9. Resistive Switching Time Variation versus Gate Resistance**



**Figure 10. Diode Forward Voltage versus Current**

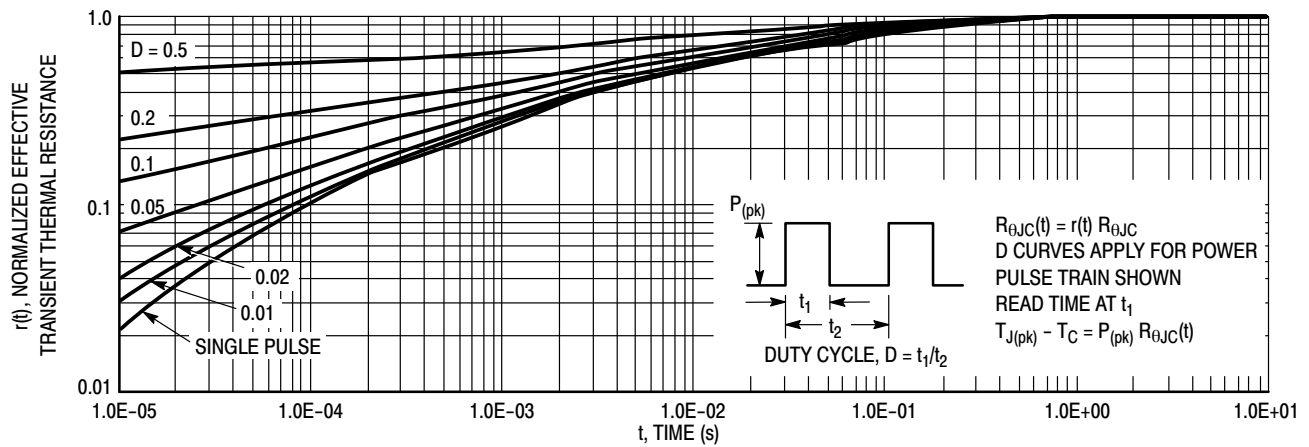


**Figure 11. Maximum Rated Forward Biased Safe Operating Area**



**Figure 12. Diode Reverse Recovery Waveform**

## NTD2955, NVD2955



**Figure 13. Thermal Response**

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTD2955G	DPAK (Pb-Free)	75 Units / Rail
NTD2955-1G	IPAK (Pb-Free)	75 Units / Rail
NTD2955T4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD2955T4G*	DPAK (Pb-Free)	2500 / Tape & Reel
SVD2955T4G*	DPAK (Pb-Free)	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NVD and SVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010



SCALE 1:1



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### MARKING DIAGRAMS



- xxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

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DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369C

#### ISSUE F

DATE 21 JUL 2015



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

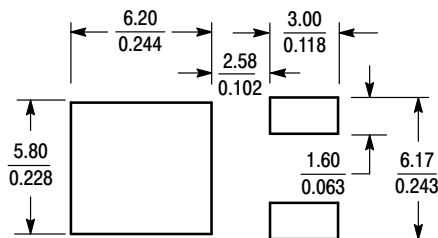


- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm / inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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