E. FACTORS AFFECTING CAPACITANCE

For any given voltage the capacitance value of the single plate device of Figure C-1 is directly proportional to the geometry and dielectric constant of the device:

$$C = KA/f(t)$$

K = dielectric constant
A = area of electrode
t = thickness of dielectric
f = conversion factor

In the English system of units, f=4.452, and using dimensions in inches for A and t, the capacitance value is expressed in picofarads (pF). For example: for a device as in Figure C-1, with a 1.0 X 1.0" area, .056" dielectric thickness, and a dielectric constant of 2500,

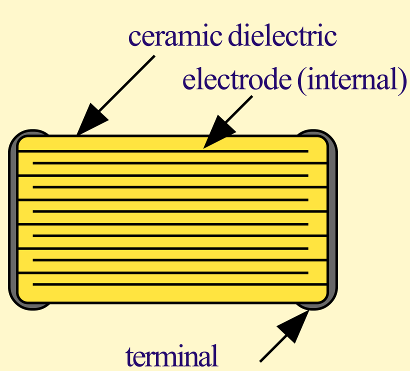
$$C = 2500\ (1.0)(1.0)/4.452\ (.056) = 10{,}027\ \text{pF}$$

utilizing the Metric System, the conversion factor is f= 11.31, and dimensions are in centimeters.

$$C = 2500\ (2.54)(2.54)/11.31\ (.1422) = 10{,}028\ \text{pF.}$$

As is evident from the above relationship of capacitance to geometry, greater capacitance can be achieved by increasing the electrode area while decreasing the dielectric thickness. As it is physically impractical to increase area in a single plate device with thinner dielectric, the concept of stacking capacitors in a parallel array was conceived to produce a physically sound device with more capacitance per unit volume, as illustrated in Figure E -1.

FIGURE E-1
MULTILAYER CAPACITOR



In this "multilayer" configuration, the area A is increased by virtue of many electrodes in parallel arrangement, in a construction permitting very thin dielectric thickness between opposing electrodes, such that the capacitance C is enlarged by the factor N (number of dielectric layers) and reduced dielectric thickness t', where A' is now the area of overlap of opposing electrodes:

$$C = KA'N/4.4452(t')$$

The capacitance value previously obtained for the inch square by 056" single plate device can now be produced with the same dielectric in a multilayer unit of only .050" x .050" x .040" dimensions and thirty (30) dielectric layers of thickness .001" (where A', the electrode overlap, is .030 x .020").

$$C = 2500\ (.030)\ (.020)\ 30/4.452\ (.001) = 10{,}107\ \text{pf}$$

This example, in effect, shows that multilayer construction can deliver the same capacitance in a volume 700 times smaller than that of the single plate device. Chip capacitors are therefore designed and manufactured to maximize the volumetric efficiency of capacitance, by optimizing the geometry and by the selection of dielectric formulations with high dielectric constant and general electrical properties, namely good insulation resistance and dielectric strength, which permit very thin layer construction.