NOVACAP TECHNICAL BROCHURE

O. CHIP USER GUIDELINES

Multilayer ceramic capacitors are sold as chip (leadless) components, or as encapsulated leaded devices. Traditionally, the chip version has been used in densely packed hybrid and delay line circuits, while the leaded capacitor has dominated the high volume printed circuit board market, which is tooled for automatic insertion of axial or radial lead devices of all types. Leaded components, packaged in tape and reel format, per EIA Standard RS 296, are assembled or "stuffed" into plated through holes on P.C. boards by high speed in line assembly machines.

The need for higher packaging densities of components on P.C. boards has led to the development by the Japanese of " surface mount technology" which involves high speed automatic placement of leadless components. As with leaded devices, this method requires the chip components to be packaged in tape and reel format, to serve as feeder spool to placement machines, or handled at high speed by chip feeders. Chip components are typically placed in 8 mm wide perforated and sealed cardboard tape, or in embossed plastic carrier (EIA Standard RS 481). The placement machine removes the chip from the carrier and "tacks" the devices to a hybrid substrate or P.C. board, with non conductive epoxy. Subsequent soldering and attachment of the components onto the circuit is accomplished with conventional solder wave processing.

The advent of surface mount technology, and high speed placement of chip capacitors in bulk form, has greatly increased the use of chip capacitors in all circuitry. Variables affecting attachment of chips to substrates are therefore of increasing importance, regardless of the method used for placement of the devices. The inherent mismatch of thermal and physical properties of components to substrates and solders is somewhat buffered with the use of leaded devices, which are isolated by virtue of the leads themselves. In contrast, this mismatch is intensified by the use of chip components directly bonded to the substrate material.

CHIP CAPACITOR ATTACHMENT METHODS

Chip bonding to substrates can be categorized into two general classes; methods involving solder, which are prevalent, such as reflow soldering, and those involving other bonds, such as epoxies, and wire bonds (thermal-compression and ultrasonic bonding).

Soldering

Solder attachment can be accomplished in a variety of ways: hand soldering of chips to substrate pads; reflow of pre-tinned capacitors on pre-tinned substrate pads; reflow of capacitors on substrate pads covered with a solder preform or with screened on solder paste, or wave soldering of chips and substrate, with chips held in position with non conductive epoxy. The latter provides the advantage

that units may be attached to both sides of the substrate, thus increasing packing densities.

A common method used in the surface mount industry is the solder paste reflow technique, and involves the following basic steps:

The surfaces to be joined are to be prepared by cleaning and pre-fluxing. Capacitors and substrate are cleaned with isopropanol or other mild solvent which does not leave residues detrimental to the circuit. Chips with excessively tarnished end metallizations, due to prolonged storage, may cause soldering difficulties. A new metal surface can be attained by firing of the chips to approximately 700°C.

Chip and substrate contact areas are pre-fluxed with a mild organic flux, which is easily removed with an azeotrope solvent after soldering. Examples of such fluxes are Kester 1544 and Kester 1545.

The substrate is pre-tinned with solder, using screened on solder paste, or by dipping of the substrate into molten solder, or with the use of solder preforms. The volume of solder required is one that results in a well formed solder fillet. Inadequate or excessive solder may result in undesirable residual stresses on the chip component.

The capacitor-substrate assembly is heated to the solder flow point temperature, allowing sufficient time for wetting of the solder to the metallized surfaces to occur, to form a well rounded fillet. Excessive time at the solder reflow temperature is undesirable due to the formation of intermetallic compounds. A controlled temperature profile, as obtained with a reflow furnace, is required to preclude thermal shock hazards.

The assembled substrate is cleaned with a mild solvent, usually by ultrasonic means, to remove flux residues from under and around the bonded chip. Total cleaning is possible as the component is somewhat elevated above the substrate surface, by virtue of the combined thickness of the conductor pad, the chip end metallization and the surface tension action of the solder in the molten state.

The advent of high component density circuits, which utilize surface mount technology, has resulted in the need for more thermal efficient and reliable soldering methods. Surface mount components are attached to the substrate by pick and place machines, and held in place by epoxy or solder paste for subsequent processing, which may involve any of the following:

Infrared (IR) solder reflow: (briefly described above): The advantage of this method is that precise temperature profiles are possible, and hence control of the many parameters of the circuit assembly can be maintained, including volatilization of solvents, activation of fluxes,

solder reflow and wetting time, and uniform and gradual cooling.

IR heat transfer is by direct radiation, and different, specific profiles need to be established for variations in board type and configuration. In general, however, IR profiles should include several minutes of time at temperatures below 100°C where solvents volatilize, to cure the thick film solder paste, and thus minimize the occurrence of blow holes, or solder splash, which result in solder balls. A preheat cycle of one to three minutes should follow, to gradually increase the temperature from 100°C to a temperature just below the solder melting point, before a rapid, less than 10 second 30°C spike, to attain solder wetting, and the formation of clean, well formed fillets. Several minutes of gradual cooling are required to terminate the cycle without inducing undesirable thermal stresses (see section 0-2.)

Vapor Phase Reflow: This method is based on rapid and thermally efficient transfer of heat from hot vapors to the hybrid assembly. Boards are located above a boiling fluid which creates a vapor phase of specific peak temperature; fluids are selected to suit the reflow point of solder types. The advantage of this system is that total immersion of the circuit in the hot vapor provides a more uniform heat transfer. The process is therefore less selective as to the characteristics of the board, but also more stressful, as the heat transfer can be very rapid. Problems may arise unless a preheat cycle is incorporated to prevent sudden outgassing of paste constituents and thermal shocking of components, and profiles are thus restricted by the circuit assembly, as with other reflow methods.

Solder Wave: This technique is in contrast to the above in that soldering is accomplished by direct contact of the hybrid assembly to molten solder. The circuit is transported through programmed flux, preheat, soldering and cooling cycles. Total immersion in flux and molten solder is attained by pumping of these through a fixture to create a constantly flowing crest or “wave” of sufficient height to cover the circuit in its entirety as it is conveyed through. Some machines utilize dual solder waves to maximize solder wetting,

The preheat cycle is included to prevent thermal shocking of components; the preheat dwell time and temperature are adjusted to attain rapid yet controlled heating of the board to approach the peak temperature of the solder wave within 50°C, in 20 to 60 seconds. Similarly, a controlled cooling cycle of several minutes follows to minimize thermal stresses within the components and/or bonds, which arise due to the thermal properties of chip capacitors, as described in section 0-2.

Regardless of which of the above methods is utilized for chip attachment, it should be noted that as with all situations of heat transfer, whether by radiation, convection or conduction, other factors over which there is little degree of freedom play a limiting role. These factors include the physical properties of the material, such as its mass, heat capacity, thermal coefficient and diffusivity, en-

thalpy, and other extraneous factors, such as velocity of gases, reflectivity to radiation, and temperature differences within the system.

The objective of any solder attachment system is the same: to attain clean and smooth solder joints, with no bridging or open areas, i.e. wetting quality and solder quantity should be optimized, and without physical defects, such as cracks, cold joints, pinholes, etc. Not all these parameters are solder processing dependent, as certain defects can be attributed to component or circuit faults, or selection of materials.

The degree of bond strength of the components to the board is also dependent on the quality of the chip termination, its own intrinsic strength, solderability and resistance to solder leach, as well as the selection of solder.

Defects of misaligned parts or units which rotate vertically to the board, to stand on end, (referred to as "tombstoning") can occur more easily with small chips, such as 0402 or 0805, and be process or material dependent. Too rapid a temperature rise in the IR or vapor phase reflow cycle can cause sudden outgassing of solder pastes, dislodging the component off its circuit pad. Also, chips with end terminations of dissimilar solderability, due to tarnishing or contaminants, or leaching of the metallization, or, pad dimensional variations, can create preferential wetting on one end of the device; the solder surface tension may pull the unit up on end, or off at an angle to create an open circuit. The same phenomenon can occur if the circuit pad terminals exhibit the same variability, or excessive solder is applied to one end of the device.

The industry has developed "barrier" type terminations for chip capacitors with superior properties, namely solderability and leach resistance which has optimized the product for these attachment processes. Refer to sections 0-3 and 0-4 for details on barrier terminations, and selection of solder types.

Epoxy Bonding

Nonconductive thermosetting epoxies are utilized to affix the capacitor body to the substrate, in preparation for secondary electrical connection, either by soldering (solder reflow or solder wave) or by wire bonding (ultrasonic or thermal-compression bonding).

An electrical mechanical bond, analogous to soldering of chips, can be achieved by using conductive epoxies, which contain metal powders of silver, copper or aluminum. Epoxies require a low temperature cure in the range of 25°C to 150°C.

Wire Bonding

Wire bonding methods involve welding of very thin gold or aluminum wires to components, to effect an electrical connection; physical attachment of the capacitor body to the substrate must be made by other means, such as epoxy bonding. The wire bond to the chip metallization or substrate pad is attained with heat and pressure, applied to the fine diameter (.001') wire tip. Localized heat at the bond is applied from an external source, as in thermal-compression bonding, or by pulsation of the wire tip, as in ultrasonic bonding. In both cases, the heat and pressure result in intermetallic mingling of the wire and host material, effecting a bond.

THERMAL PROPERTIES OF CHIP CAPACITORS

Chip attachment methods invariably involve thermal cycling of the component. The expansion characteristics of the chip and substrate, as well as the mechanical properties of the bonding medium result in residual stresses, the degree of which determine the reliability of the bonded chip.

Chip capacitors can tolerate relatively high temperatures, by virtue of their processing, which typically involves a 1100°C to 1200°C firing of the dielectric body, followed with a second firing of the end metallization at approximately 850°C. Chips therefore could be cycled to as high as 850°C with no detrimental effect on the devices, provided the process does not expose the product to sudden or nonuniform temperature changes, which can cause thermal shock failure. Capacitors with nickel barrier terminations, which have a solder coat over the nickel, (or solder coated terminations) are restricted to the reflow temperature of the solder.

Temperature cycling causes a change in the mean interatomic spacing of the atoms in the crystal lattice, due to variations in thermal energy. The characteristic dimensional change of materials with temperature is a function of temperature, and is reported as the volumetric or linear coefficient of thermal expansion, expressed as:

$$\text{(linear coefficient)} \propto = dl/IdT \text{ (cm/cm/°C, or in/in °C)}$$

If the dimensional changes caused by temperature cycling are not uniform, the resultant differential strains cause stresses within the material. These stresses are significant in ceramic materials, which, unlike metals, lack ductility to relieve the stress. Heating of a material causes a positive expansion, resulting in compressive stress. Conversely, cooling results in tensile forces, as the material attempts to contract. As ceramics are characteristically weaker under tensile load, it follows that the type of temperature change, i.e. heating or cooling, as well as the rate, uniformity and degree of change are critical. Thermal cycling of chip capacitors therefore involves the following general precautions:

The rate of heating must be uniform and controlled to preclude the occurrence of differential strains in the chip, as is accomplished in a reflow furnace. Other soldering methods, such as hand or wave soldering should be preceded with a preheat cycle to bring the components to the solder flow temperature gradually. Although heating generally produces the more benign compressive stresses in the ceramic body, it should be noted that the more heat conductive chip end metallizations heat preferentially, i.e., the chip ends expand more rapidly than the main body of the chip, resulting in tensile stresses between the body and metallized ends.

Chip capacitors are even more vulnerable to failure during the cooling cycle, as negative temperature gradients cause primarily tensile stress. Cooling must therefore be gradual and uniform, with no localized forced cooling or contact of the chip with any efficient heat sink.

The effects of capacitor geometry are self evident; thermal gradients and resultant stresses are directly proportional to chip mass, hence larger units are more susceptible to thermal shock than smaller devices. Also, the contribution of preferential heat conduction of end terminations to undesirable stresses increases with larger or longer chips, as more mass is available to maintain the thermal gradients.

Without mechanical restriction, thermally induced stresses are released once the capacitor attains a steady state condition, at any given temperature. Capacitors bonded to substrates, however, will retain some stress, due primarily to the mismatch of expansion of the component to the substrate; the residual stress on the chip is also influenced by the ductility and hence the ability of the bonding medium to relieve the stress. Unfortunately, the thermal expansions of chip capacitors differ significantly from those of substrate materials. At 25°C to 300°C, capacitors typically range in expansion coefficient from 8.3×10^{-6} to 12.2×10^{-6} in/in/°C, while 99% Alumina is approximately 6.0×10^{-6} in/in/°C and P.C. board is typically 16.0×10^{-6} in/in/°C.

Chips bonded to alumina therefore will retain a tensile stress, as the expansion coefficient of the dielectric material exceeds that of the substrate. On cooling, the chip capacitor will attempt to shrink more than the substrate, but is restrained from doing so by the substrate material and solder or epoxy bond. Chips bonded to P.C. board will retain a compressive stress, as the substrate material attempts to shrink more than the chip. In either case, a shear stress is incorporated into the bond medium; the reliability of the bond therefore is greatly dependent on the load bearing capability of the bonding material.

SELECTION OF SOLDER

Solders are the most common bonding alloys used in capacitor attachment. ‘Low temperature’

solders, with flow points under 250°C, are generally tin-lead alloys, with or without silver additions. 'High temperature' solders, with flow points of 260°C to 370°C are based on high lead content, alloyed with silver and/or tin, or based on gold, alloyed with germanium or tin.

Solders are selected based on the assembly temperature restrictions of the circuit, the hardness or ductility of the alloy, and the comparability of the solder to the chip termination and substrate conductor composition. Common solder types, flow points and hardness are tabulated in Table 0-1. Of importance are the following considerations:

Solder Leach: At the solder flow temperature, tin-lead alloys absorb silver (or gold) from the chip termination and/or the substrate pad. This effect is minimized by using solders which contain some percentage of silver, such as Sn62, and by limiting the time at reflow temperature to the minimum required to obtain good wetting and a well rounded fillet (approximately 5 seconds). Excursion of temperature above the flow point of the solder need also be avoided, as the leaching rate increases rapidly with temperature. The leaching effect is cumulative; repeated reflow of the solder during processing of the circuit will aggravate the problem.

Capacitor termination alloys and geometry are designed to reduce the leaching effects of solders. Termination materials have evolved from pure silver to silver-palladium alloys, typically 80Ag-20Pd, as the palladium inhibits silver leaching. Leaching, if it occurs, is predominant at the corners and edges of the chip termination, where the termination alloy is thinnest. This effect is minimized by the chip manufacturer by rounding of the corners and edges of the chip, with a tumbling process, before terminations are applied, to obtain a more uniform thickness of coverage.

Vapor phase reflow, and dual wave soldering, utilized with surface mount technology, have imposed solder leach requirements on components which preclude the use of silver-palladium terminations. Best resistance to solder heat is attained by the use of barrier type terminations, which have a nickel layer plated over a silver termination, with a solder or tin protective overcoat, to enhance solderability and prevent oxidation of the base metal layer. Capacitors with such terminations will survive molten solder at 260°C, with no discernible leaching effect, for several minutes, versus less than twenty seconds for the best Pd-Ag alloys, as nickel is relatively insoluble in Sn, Pb or Ag, and therefore acts as a barrier to solder leaching.

Solder Hardness: As described previously, thermal expansion mismatch of the chip capacitor and the substrate material results in residual shear stress at the bond. Theoretical calculations indicate that this stress can exceed 7000 psi, sufficient to lead to rupture of the chip, if the latter is under tension, or failure of the bond, if the chip is under compression. Fortu-

nately, this condition is alleviated by the ability of the bonding alloy to deform and absorb the majority of the stress. The ductility of the solder alloys is inversely proportional to the hardness of the material, hence use of softer solders (of lower Brinell hardness) is desirable.

The most common solder used in hybrid circuit application is Sn62 (62Sn,36Pb,2Ag). Selection of other solders is often predicated on the need for higher temperature tolerance of the circuit, i.e., bonding alloys with higher flow points are mandatory.

TABLE O-1
COMMON BONDING ALLOYS

Solder Type	Flow Point °C	Brinell Hardness
Sn63 (63Sn, 37Pb)	183	30
Sn60 (60Sn, 40Pb)	189	28
Sn62 (62Sn, 36Pb, 2Ag)	189	33
Sn50 (50Sn, 50Pb)	212	24
95Sn, 5Ag	240	22
80Au, 20Sn	280	115
Sn5 (95Pb, 5Sn)	312	15
88Au, 12Ge	356	107
95Pb, 5Ag	360	12

CHIP TERMINATIONS

Capacitor terminations consist of metal-frit (glass) compounds which are fused to the capacitor body, to effect an electrical connection between the internal capacitor electrodes and the circuit pads. Terminations can be classified into two general categories: older thick film silver or silver-palladium (80Ag-20Pd) metallizations, and the more popular barrier type termination used for surface mount components.

The silver-palladium termination has adequate resistance to solder leach, and less tendency to tarnish than pure silver terminations. Silver finds application mostly on units destined for axial or radial leading, or on specialty items, such as high voltage capacitors, which require the use of more ductile silver metal to reduce thermal shock hazards to these units when leaded.

Silver bearing terminations can tarnish. Usually packed with a tarnish retardant paper, capacitors will store indefinitely and solder properly with the appropriate fluxes. Severely tarnished units can be restored to a clean metal finish by refiring of the product to approximately 700°C to 800°C. Note that product supplied in reeled format cannot be effectively protected by tarnish retardant paper, as units stored in bulk, hence inventory planning or the use of barrier termination is recommended.

Barrier layer terminations are based on plating technology to provide 100 to 150 microinches of nickel thickness over a fired silver termination. As nickel readily oxidizes, a second tin/solder or tin layer 200 to 250 micro inches thick is plated over the nickel, to protect it and provide a readily solderable surface with good shelf life.

The electrolytic process is perhaps the preferred method of nickel deposition. A current is utilized to deposit nickel from nickel sulfamate and nickel chloride in a boric acid solution onto the silver termination of the capacitor. This termination differs from conventional materials in that the frit which bonds the termination to the capacitor must be chemically resistant to the plating solutions, and thus is bismuth free. (Such frits do not promote solderability, hence units with this termination are unsolderable unless properly plated with nickel and solder). Immediately after the nickel process, units must undergo the solder process before the onset of any oxidation of the base metal layer. Units are electroplated using tin and lead concentrates in a deionized water solution.

An electroless method of nickel deposition, based on chemical reduction of nickel boron solutions and catalytic activators, can also provide a continuous nickel barrier layer, but is not as suitable for tin lead plating. Alternate application of a solder coat by wave soldering methods creates dimensional tolerance difficulties, not desirable for components to be taped and reeled for use in surface mount technology

The distinct advantage of the nickel barrier termination is evident in its name; it serves not only as a guard against solder leach, by virtue of the relatively insoluble nature of nickel in solder alloys, but also forms a barrier to the formation of intermetallic compounds in the solder joint which can adversely affect the long term reliability of the bond. Non barrier terminations can be affected by a time dependent diffusion phenomenon of Ag, Pd and Sn atoms, which accelerate with thermal cycling, and can eventually lead to alteration of the physical properties of the bond, and result in stress cracks separating the component from the assembly. Capacitors with nickel barrier terminations have been shown to arrest the diffusion process and the formation of intermetallic compounds, hence maintaining the integrity of the bond.

The quality of capacitors with barrier terminations is largely dependent on the properties of the ceramic dielectric and the process parameters used for plating. Not all dielectric materials, terminations and plating solutions are entirely compatible, and great care must be exercised by the manufacturer to produce product with suitable electrical and mechanical properties. The plating processes, for example, may alter the dielectric surface, and affect the insulation resistance of the product. Also, the rate of nickel deposition and plating bath chemistry and temperature can establish a certain intrinsic stress in the nickel layer. Despite the thin dimension of this layer, the nickel may impart a significant tensile stress on the unit at the termination which can lead to mechanical failure, usually occurring shortly after soldering of the unit to the substrate. This phenomenon has manifested itself

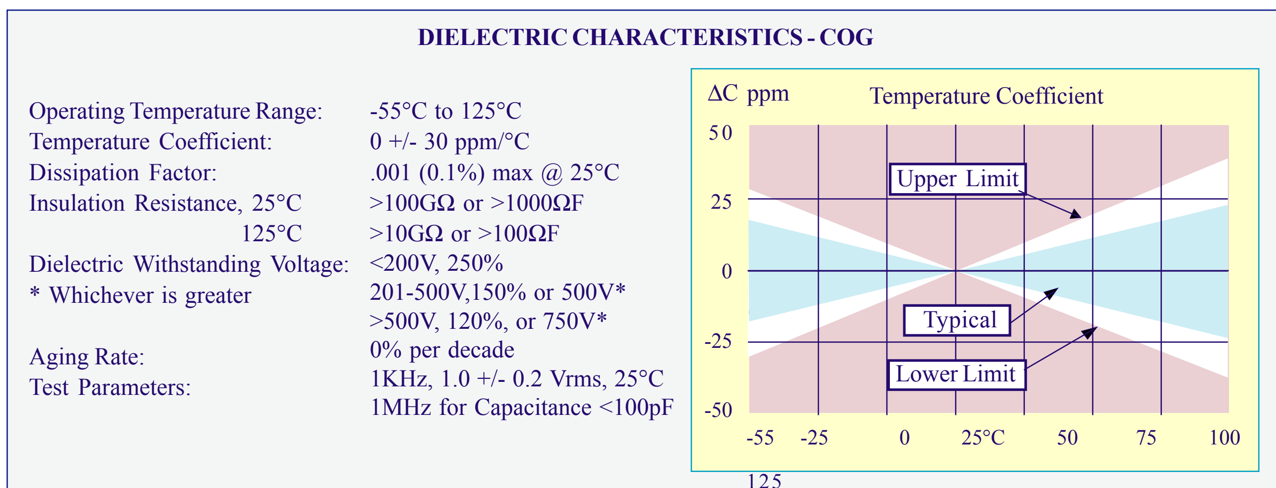
primarily with the more susceptible X7R and Z5U formulations. Although it is a characteristic of all nickel deposition to retain a contractile or tensile condition, the industry has developed the methods to plate the material with controlled metallographic structure and ductility, to produce physical and mechanical properties suitable for all the dielectric types of multilayer capacitors.

Ion Migration

Chip terminations and bonding alloys contain metals, notably silver and tin, which can hydrolyze in the presence of water moisture. Under the influence of an electric field, the hydroxide can dissociate to form metal cations, which have a net positive charge, and can migrate to the cathode. This phenomenon occurs with AC voltage as well as with a dc bias, the severity of which is directly proportional to the voltage gradient. Given enough time, a bridge of silver or tin will form between chip terminations, reducing the insulation resistance and eventually forming an electrical short. Avoidance of this problem can be accomplished with the use of very expensive gold terminations and substrate conductors, or with the elimination of water moisture from the circuit, which precludes the formation of mobile cations. The latter is accomplished by hermetic sealing of circuits, or the use of water proof encapsulants, such as epoxies.

PERFORMANCE SPECIFICATIONS

Choice of capacitor type, other than size, value and termination, is based on dielectric performance characteristics. Following are tables and illustrations describing the dielectric characteristics of the popular Class I (NPO-COG) and Class II formulations (X7R, Z5U, Y5V).

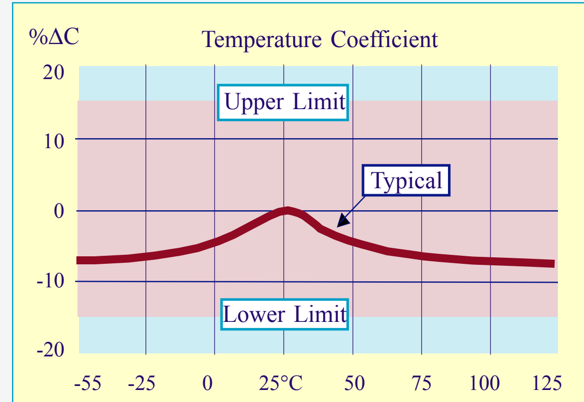


DIELECTRIC CHARACTERISTICS - COG

Operating Temperature Range:	-55°C to 125°C
Temperature Coefficient:	0 +/- 30 ppm/°C
Dissipation Factor:	.001 (0.1%) max @ 25°C
Insulation Resistance, 25°C	>100GΩ or >1000ΩF
125°C	>10GΩ or >100ΩF
Dielectric Withstanding Voltage:	<200V, 250%
* Whichever is greater	201-500V,150% or 500V*
	>500V, 120%, or 750V*
Aging Rate:	0% per decade
Test Parameters:	1KHz, 1.0 +/- 0.2 Vrms, 25°C
	1MHz for Capacitance <100pF

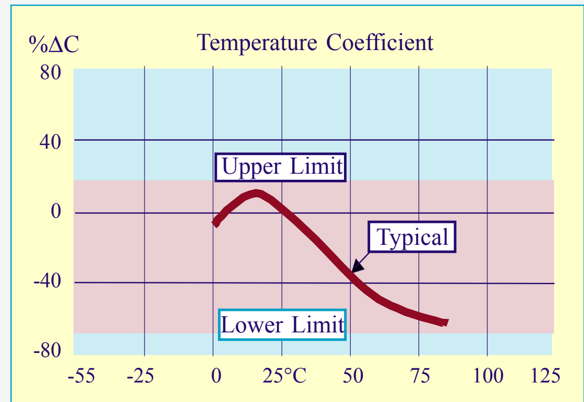
DIELECTRIC CHARACTERISTICS - X7R

Operating Temperature Range:	-55°C to 125°C
Temperature Coefficient:	+/-15% ΔC Max.
Dissipation Factor:	.025 (2.5%) max @ 25°C
Insulation Resistance, 25°C	>100GΩ or >1000Ω F
125°C	>10GΩ or >100Ω F
Dielectric Withstanding Voltage:	<200V, 250%
* Whichever is greater	201-500V,150% or 500V*
	>500V, 120%, or 750V*
Aging Rate:	< 2.0% per decade
Test Parameters:	1KHz, 1.0 +/- 0.2 Vrms, 25°C



DIELECTRIC CHARACTERISTICS - Z5U

Operating Temperature Range:	+10°C to 85°C
Temperature Coefficient:	+22%-56% ΔC Max.
Dissipation Factor:	.030 (3.0%) Max @ 25°C
Insulation Resistance, 25°C	>10GΩ or >100ΩF
Dielectric Withstanding Voltage:	<200V, 250%
	250V, 150%
Aging Rate:	~ 2.0% per decade
Test Parameters:	1KHz, 0.5 +/- 0.2 Vrms, 25°C



DIELECTRIC CHARACTERISTICS - Y5V

Operating Temperature Range:	-30°C to 85°C
Temperature Coefficient:	+22%-82% ΔC Max.
Dissipation Factor:	.050 (5.0%) max @ 25°C
Insulation Resistance, 25°C	>10GΩ or >100ΩF
Dielectric Withstanding Voltage:	<200V, 250%
	250V, 150%
Aging Rate:	~ 2.0% per decade
Test Parameters:	1KHz, 0.5 +/- 0.2 Vrms, 25°C